PD77718 and PD77010 Evaluation Board User Guide

EV99F34A

Introduction

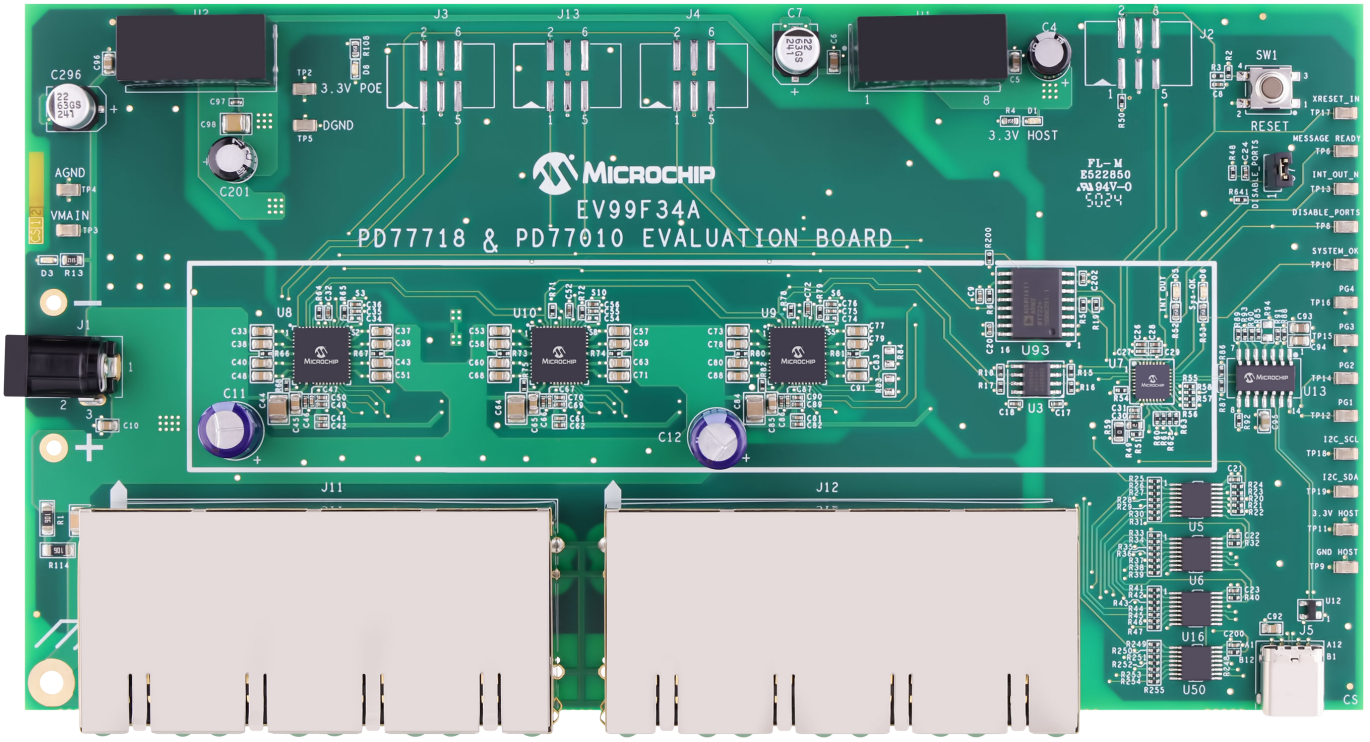
The EV99F34A evaluation board (EVB) is based on Microchip's PD77718 PoE manager and the PD77010 PoE controller. The EV99F34A operates in Controller mode using the PD77010 and demonstrates eight IEEE® 802.3bt 2-pair ports using the PD77718T3 and eight IEEE 802.3bt 4-pair ports using two PD77718T4 devices.

The PD77718 device is a part of the seventh generation IEEE 802.3bt compliant Power over Ethernet (PoE) Power Sourcing Equipment (PSE) family from Microchip. This device is a fully integrated eight port PoE manager, with integrated Field Effect Transistor (FET) switches and current sense resistors. The PD77718 chipset supports IEEE 802.3af/at/bt standards, as well as legacy/pre-standard PD detection. The device is available in a 56-pin, 8 mm × 8 mm Quad flat no-lead (QFN) package.

The EVB includes two green LEDs per port. These LEDs provide the visual status of each port.

The following figure shows the top view of the evaluation board.

Figure 1. Evaluation Board - Top View



Features

The EVB has the following features.

- RJ45 Gang (Contains Eight RJ45 Connectors)
- Eight 2-pair and Eight 4-pair Ports Structured by Three PD77718 Devices and Controlled by the PD77010.
- Switch Domain USB-C® Interface to be Connected to a PC with the Microchip GUI
- Manual Reset and Disable Port Jumpers
- Two Green LED Status Indication for all Sixteen Ports
- Requires only a Single Power Source
- 0 °C to 40 °C Operating Temperature
- RoHS Compliant

The following images show the system block diagram and the dimensions of the evaluation board.

Figure 2. EV99F34A Evaluation Board Block Diagram

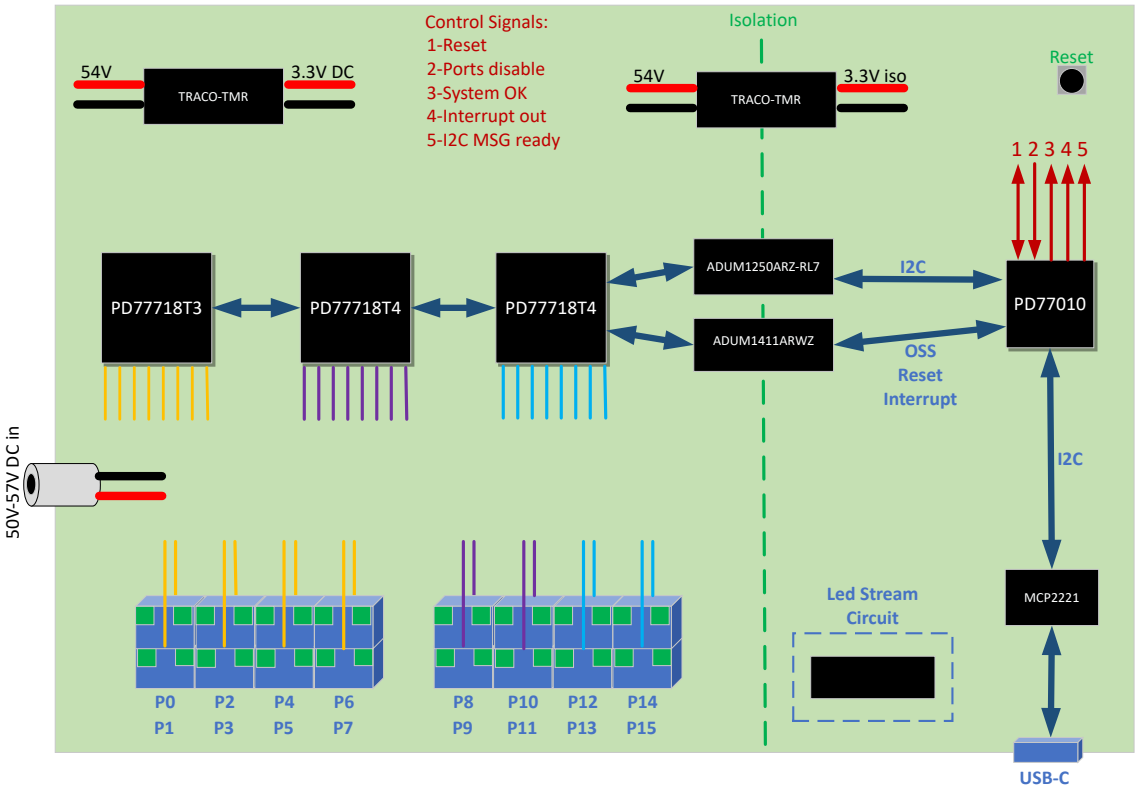
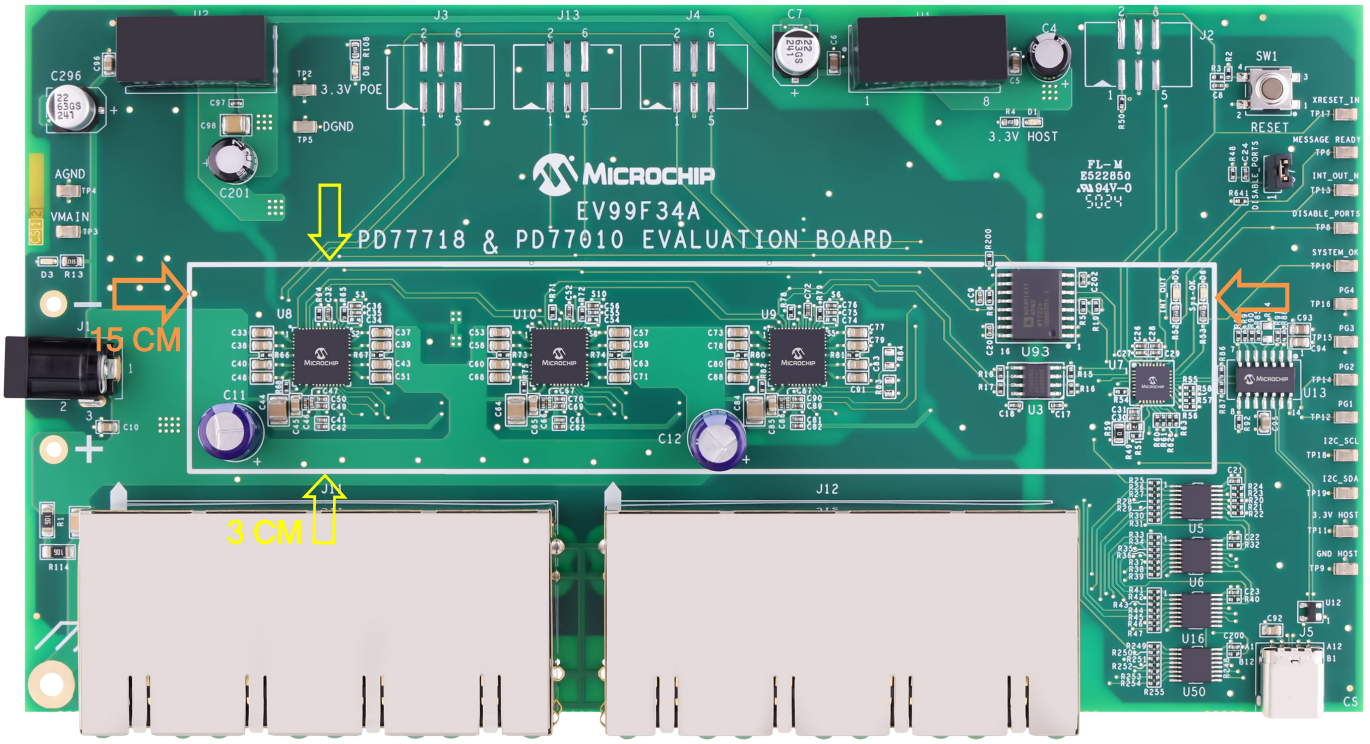


Figure 3. EV99F34A Dimension



Note: Actual PoE application size is 15 cm × 3 cm

Table of Contents

1. Overview

This section provides the basic overview of the EV99F34A evaluation board.

1.1 Power

The EVB is powered by a single source through the DC connector J1. The input voltage level can be selected according to the following IEEE 802.3 PoE standards:

1. IEEE 802.3af: 44 V_{DC} to 57 V_{DC}
2. IEEE 802.3at: 50 V_{DC} to 57 V_{DC}
3. IEEE 802.3bt:
   a. 50 V_{DC} to 57 V_{DC} for Type 3
   b. 52 V_{DC} to 57 V_{DC} for Type 4

The recommended voltage level is 53 V_{DC} to 55 V_{DC}, which covers all the PoE standards. The EVB has three power domains as follows:

1. PoE domain, which is fed directly by the main supply and is the power domain provided by the RJ45
2. 3.3 V_{DC} which feeds the PD77718 and serial communication peripherals, same ground as the PoE domain. This 3.3 V_{DC} is generated by U2 (a DC/DC module).
3. Isolated 3.3 V_{DC} for the PD77010, LED stream, and for the USB port; this power is provided by U1.

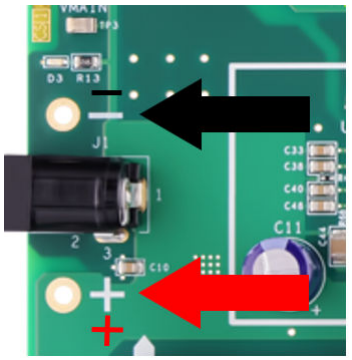
Note: The EVB is polarity sensitive. The correct polarity is shown in the following figure.

Figure 1-1. DC Connector J1 Polarity

Important: DC input connector J1 is limited to current level up to 4A. If higher current is needed, the 2 via holes next to J1 can be used by soldering a cable to it. The two via holes support up to 8A to feed the whole EVB at full power.

The via holes are marked in the following figure: hole marked red is the V_{main} (+), and the hole marked black is the AGND (−).

Figure 1-2. Power via Holes



1.2 Interface and Control

This section describes the set-up procedures for serial communication, reset push-button, Over Supply Shutdown (OSS), PoE ports disable, power good input (PGD1–PGD4), and additional test points.

1.2.1 Serial Communication

The EVB supports serial communication with the PD77010 by I²C. The serial communication is converted to USB by the MCP2221A (U13) from Microchip through a dedicated GUI that allows a user-friendly experience.

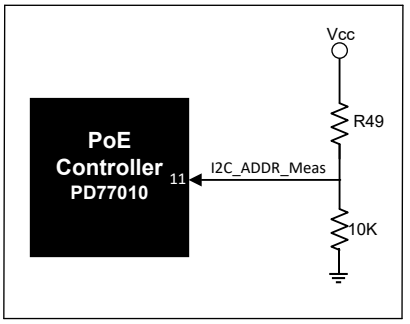
To use the USB port, install the MCP2221A driver on your PC. You can download the driver from the Microchip website at www.microchip.com/wwwproducts/en/MCP2221A

If R94 is installed as 0Ω, the USB converter (U13) is disabled, which allows the user to connect directly to the I²C bus through the I²C pins of U13, and control the EVB through I²C. The DGND test-point is the GND for the I²C bus. For test points location, see Figure 1-7. The EVB is set to I²C address 0x4 (R49=147K). In order to select the I²C address, R49 should be installed according to the following table.

I2C Address	Address (Hex)	R49 (kΩ)
#1	0x4	147
#2	0x8	86.6
#3	0xC	57.6
#4	0x10	43.2
#5	0x14	34
#6	0x18	26.7
#7	0x1C	22.1
#8	0x20	18.2
#9	0x24	15.4
#10	0x28	13
#11	0x2C	11
#12	0x30	9.31
#13	0x34	7.87
#14	0x38	6.49
#15	0x3C	5.49

The following diagram shows the I²C address setting for the PD77010 controller.

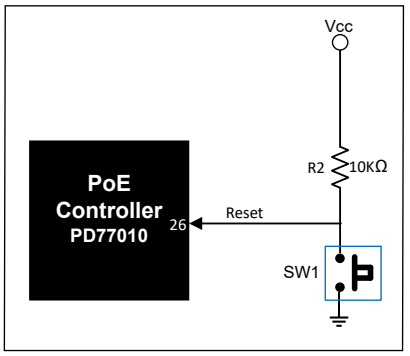
Figure 1-3. I²C Address Setting Diagram



1.2.2 Reset Pushbutton

The pushbutton is connected to the Reset pin of the PD77010 (pin 26), as shown in the following figure. To connect the Reset pin to GND, press the SW1 switch. This resets the PoE system.

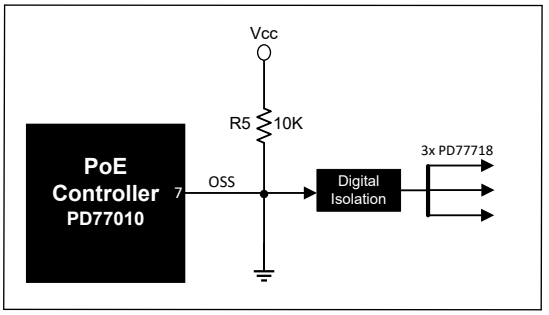
Figure 1-4. Reset Control Diagram



1.2.3 Over Supply Shutdown (OSS)

OSS is used to shut down ports based on the priority settings. The following figure shows the OSS control diagram.

Figure 1-5. OSS Control Diagram

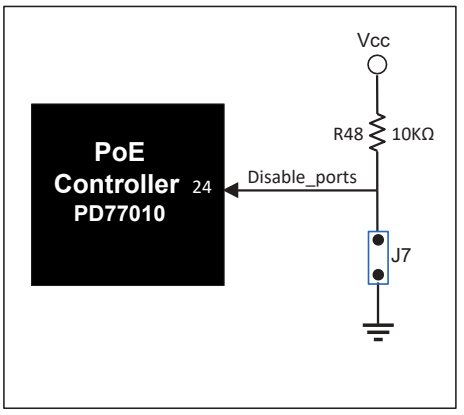


1.2.4 PoE Ports Disable Settings

The jumper J7 is connected to the Disable pin of the PD77010 (Pin 24). When the jumper J7 is installed, the Disable pin is connected to GND.

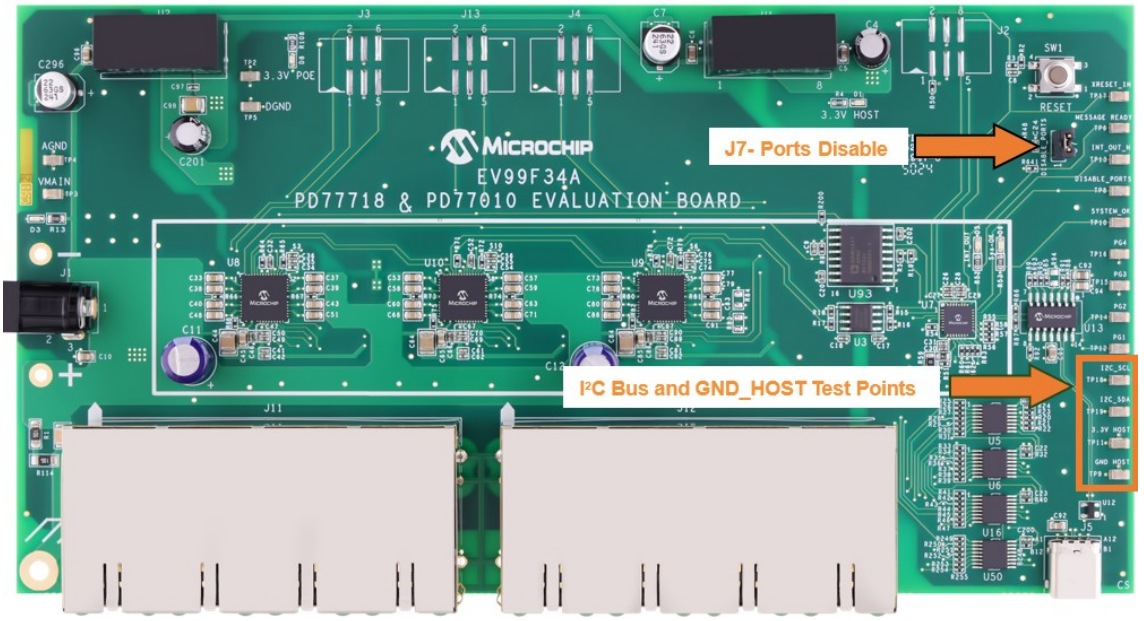
In normal operations, the host can disable all ports by setting this pin to '0'. The following figure shows the J7 jumper settings.

Figure 1-6. Ports Disable Control Jumper Diagram



The following figure shows the J7 Ports Disable jumper and the I²C bus and GND_HOST test points on the evaluation board.

Figure 1-7. I²C Bus and GND_HOST Test Points



Important: These I²C test points are connected to the I²C bus, which connects to the PD77010.

1.2.5 Power Good Input (PGD) Settings

The EVB supports feeding from up to four power supplies, which includes four power banks (bank 1 to bank 4). Each power supply must generate a digital signal (0-3.3 V_{DC}), which indicates the power supply is active. The generated digital signal must be connected to one of the PG pins of PD77010 (pins 17, 18, 19, and 20). This is defined in the following table. See the *PD77010 BT Serial Communication Protocol User Guide* for more detail.

Table 1-1. Power Banks

Power Bank	PG1 Pin 17	PG2 Pin 18	PG3 Pin 19	PG4 Pin 20
PB0*	0	0	0	0
PB1	1	0	0	0
PB1	0	1	0	0
PB1	0	0	1	0
PB1	0	0	0	1
PB2	1	1	0	0
PB2	1	0	1	0
PB2	1	0	0	1
PB2	0	1	1	0
PB2	0	1	0	1
PB2	0	0	1	1
PB3	1	1	1	0
PB3	0	1	1	1

Table 1-1. Power Banks (continued)

Power Bank	PG1 Pin 17	PG2 Pin 18	PG3 Pin 19	PG4 Pin 20
PB3	1	1	0	1
PB3	1	0	1	1
PB4	1	1	1	1

*If a single power supply with no power good signaling is used, PG1-PG4 are connected to GND.

On the EVB, four PG pins are pulled down with a 10K resistor to GND_HOST, which sets the default power bank to 0x00. To set a different bank than 0x00, the user can use the PG1–PG4 test points, located next to U13.

The four PG signals are referenced to the PD77010 domain (GND_HOST), see the following figures

Figure 1-8. PG1–PG4 Test Points Diagram

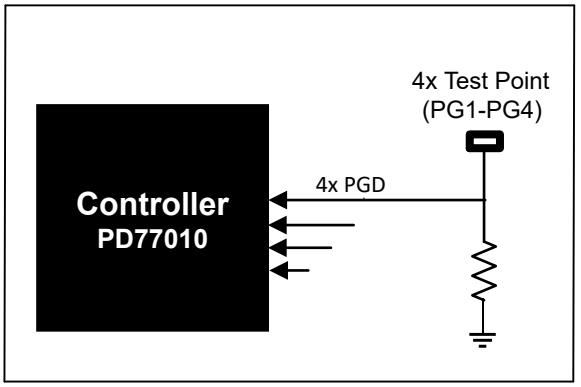
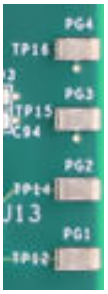


Figure 1-9. PG1–PG4 Test Points



1.2.6 Additional Test Points

The additional test points and their uses are as follows:

1. xI2C_Message_Ready (TP6): I^2C message ready for reading by the host. The Controller asserts this line low when it has an answer to the host. Therefore, the host can poll this line and initiate I^2C read cycle only when the message is ready. After the host reads the data from the controller, this pin is asserted to high. (Active Low).
2. xINT_OUT (TP13): Interrupt output indication. This line is asserted Low when a pre-configured event is in progress. (Active Low).
3. xReset_IN (TP17): Host reset input. (Active Low).
4. Disable ports (TP8): When this pin is pulled down, the PSE activity is off (Active Low). This TP is shorted to jumper J7.
5. xSys_ok (TP10): System validity indication. The behavior of this output is controlled by individual software mask. (Active Low).

Note: All the TPs in the preceding list are referenced to the PD77010 domain (GND_HOST).

The placement of the test points on the evaluation board is as shown in the following figure.

Figure 1-10. Test Points

1.3 LED Indication

The evaluation board contains status indication LED. These LEDs and their corresponding functions are listed in the following table.

Table 1-2. LED List

Designation	Function
D1	Isolated 3.3 V_{DC} ON (powers the PD77010, reset, LED stream, USB comm)
D3	VMAIN ON
D5	Interrupt out (active low)
D6	System OK (active low)
D8	3.3 V_{DC} ON (powers the three PD77718)
Port (0–15)	Two green LED per port: • LED OFF= Port is OFF • Right green LED on= 4-pair port is on • Left green LED on= 2-pair port is on • Right LED blinking= Port is OFF due to error/under load/ power management

1.4 RJ45 Connectors Polarity

The eight ports of J11 are 2-pair up to 30W and eight ports of J12 are 4-pair up to 90W each. The polarity of the port is listed in the following tables.

Table 1-3. J11/RJ45 Connector 2-Pair Port (Ports 0-7)

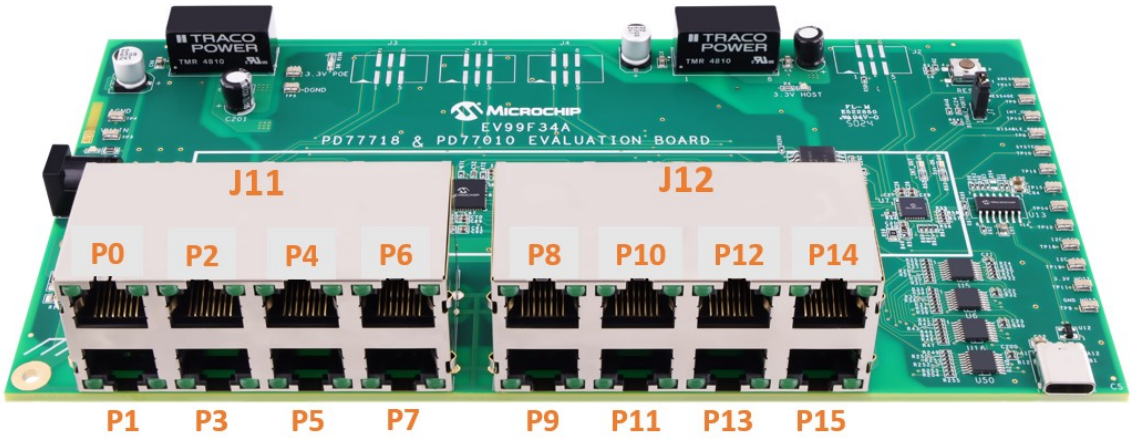
Pin Number (Each RJ45 Port)	Polarity
1, 2	Negative Alt A
3, 6	Positive Alt A
4, 5	N.A.
7, 8	N.A.

Table 1-4. J12/RJ45Connector 4-Pair Port (Ports 8-15)

Pin Number (Each RJ45 Port)	Polarity
1, 2	Negative Alt A
3, 6	Positive Alt A
4, 5	Positive Alt B
7, 8	Negative Alt B

See the following figure for port numbering.

Figure 1-11. Port Numbering



2. Installation and Setting

This section describes the steps required to install and operate the EVB. Take the following precautions before starting the installation:

- Ensure that the 52 V_{DC}– 57V_{DC} power supply of the board is turned off before plugging in the DC connector.
- Turn the main power supply on only after the DC connector is plugged in.
- Ensure the correct polarity of the power supply cable. The polarity of the power supply cable is as shown in Figure 1-1.

2.1 Port Matrix

Ensure that the ports matrix is configured according to the following table

Table 2-1. Port Matrix Configuration

Logical Port	Physical Port A	Physical Port B
0	0	255 (0xFF)
1	1	255 (0xFF)
2	2	255 (0xFF)
3	3	255 (0xFF)
4	4	255 (0xFF)
5	5	255 (0xFF)
6	6	255 (0xFF)
7	7	255 (0xFF)
8	8	9
9	10	11
10	12	13
11	14	15
12	16	17
13	18	19
14	20	21
15	22	23

2.2 Schematics

Contact Microchip for the full-board schematics.

3. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 3-1. Revision History

Revision	Date	Description
A	03/2025	Initial Revision

Microchip Information

Trademarks

The “Microchip” name and logo, the “M” logo, and other names, logos, and brands are registered and unregistered trademarks of Microchip Technology Incorporated or its affiliates and/or subsidiaries in the United States and/or other countries (“Microchip Trademarks”). Information regarding Microchip Trademarks can be found at https://www.microchip.com/en-us/about/legal-information/microchip-trademarks.

ISBN: 979-8-3371-0840-7

Legal Notice

This publication and the information herein may be used only with Microchip products, including to design, test, and integrate Microchip products with your application. Use of this information in any other manner violates these terms. Information regarding device applications is provided only for your convenience and may be superseded by updates. It is your responsibility to ensure that your application meets with your specifications. Contact your local Microchip sales office for additional support or, obtain additional support at www.microchip.com/en-us/support/design-help/client-support-services.

THIS INFORMATION IS PROVIDED BY MICROCHIP “AS IS”. MICROCHIP MAKES NO REPRESENTATIONS OR WARRANTIES OF ANY KIND WHETHER EXPRESS OR IMPLIED, WRITTEN OR ORAL, STATUTORY OR OTHERWISE, RELATED TO THE INFORMATION INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF NON-INFRINGEMENT, MERCHANTABILITY, AND FITNESS FOR A PARTICULAR PURPOSE, OR WARRANTIES RELATED TO ITS CONDITION, QUALITY, OR PERFORMANCE.

IN NO EVENT WILL MICROCHIP BE LIABLE FOR ANY INDIRECT, SPECIAL, PUNITIVE, INCIDENTAL, OR CONSEQUENTIAL LOSS, DAMAGE, COST, OR EXPENSE OF ANY KIND WHATSOEVER RELATED TO THE INFORMATION OR ITS USE, HOWEVER CAUSED, EVEN IF MICROCHIP HAS BEEN ADVISED OF THE POSSIBILITY OR THE DAMAGES ARE FORESEEABLE. TO THE FULLEST EXTENT ALLOWED BY LAW, MICROCHIP’S TOTAL LIABILITY ON ALL CLAIMS IN ANY WAY RELATED TO THE INFORMATION OR ITS USE WILL NOT EXCEED THE AMOUNT OF FEES, IF ANY, THAT YOU HAVE PAID DIRECTLY TO MICROCHIP FOR THE INFORMATION.

Use of Microchip devices in life support and/or safety applications is entirely at the buyer’s risk, and the buyer agrees to defend, indemnify and hold harmless Microchip from any and all damages, claims, suits, or expenses resulting from such use. No licenses are conveyed, implicitly or otherwise, under any Microchip intellectual property rights unless otherwise stated.

Microchip Devices Code Protection Feature

Note the following details of the code protection feature on Microchip products:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner, within operating specifications, and under normal conditions.
- Microchip values and aggressively protects its intellectual property rights. Attempts to breach the code protection features of Microchip products are strictly prohibited and may violate the Digital Millennium Copyright Act.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is “unbreakable”. Code protection is constantly evolving. Microchip is committed to continuously improving the code protection features of our products.