nRF54L15 DK Hardware

v1.0.0

User Guide

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NORDIC® SEMICONDUCTOR

Contents

Revision history

Date	Description
August 2025	Updated for nRF54L15 DK v1.0.0: • Hardware description on page 7 • Power supply on page 8 • nRF54L15 SoC external power with DK functionality on page 9 • GPIO interface on page 10 • External memory on page 12 • Buttons and LEDs on page 13 • 32.768 kHz crystal on page 14 • NFC antenna interface on page 14 • Solder bridge configuration on page 15 • Board control on page 16 • RESET button on page 17 • Virtual serial ports on page 17 • Debug input and trace on page 19 • Debug out for programming external boards on page 19 • Current measurements on page 22 • Set up the DK on page 22 Added: • nRF54L15 SoC external power with DK functionality on page 9 • Regulatory information on page 26
December 2024	Editorial update
November 2024	First release

Previous versions

nRF54L15 DK Hardware v0.9.1 User Guide

Environmental and safety notices

Power supply

The nRF54L15 DK must be powered by a PS1 class (IEC 62368-1) power supply with maximum power less than 15 W.

Skilled persons

The nRF54L15 DK is intended for use only by skilled persons.

A skilled person is someone with relevant education or experience that enables them to identify potential hazards and takes appropriate action to reduce the risk of injury to themselves and others.

Hot surface

In the event of a fault, touchable surfaces can heat up significantly.

Electrostatic discharge

The nRF54L15 DK is susceptible to *Electrostatic Discharge (ESD)*.

To avoid damage to your device, it should be used in an electrostatic free environment, such as a laboratory.

Environmental Protection

Waste electrical products should not be disposed of with household waste.

Please recycle where facilities exist. Check with your local authority or retailer for recycling advice.

1 Introduction

The nRF54L15 DK is a hardware development platform used to design and develop application firmware on the nRF54L15 SoC.

Key features

- nRF54L15 SoC in QFN48 package
- Support for the following wireless protocols:
  - *Bluetooth*® Low Energy
  - NFC
  - 802.15.4
  - Thread®
  - 2.4 GHz proprietary
  - Zigbee®
- 2.4 GHz and NFC antennas
- *Microwave coaxial connector with switch (SWF)* RF connector for direct RF measurements
- Four user-programmable LEDs
- Four user-programmable buttons
- SEGGER J-Link OB programmer/debugger
- Two *Universal Asynchronous Receiver/Transmitter (UART)* interfaces through virtual serial ports
- USB connection to debugger for debugging, programming, and power
- Header for measuring power consumption
- nPM1300 *Power Management Integrated Circuit (PMIC)* providing a 1.8 V to 3.3 V user-programmable power supply from USB
- 64 Mb flash memory
- Programmatic connection and disconnection of extended DK functionality including external memory, UART interfaces, debug interface, and LED power

Kit content

The nRF54L15 DK includes hardware, preprogrammed firmware, documentation, hardware schematics, and layout files.

The nRF54L15 DK (PCA10156) comes with an NFC antenna (PCA64110).

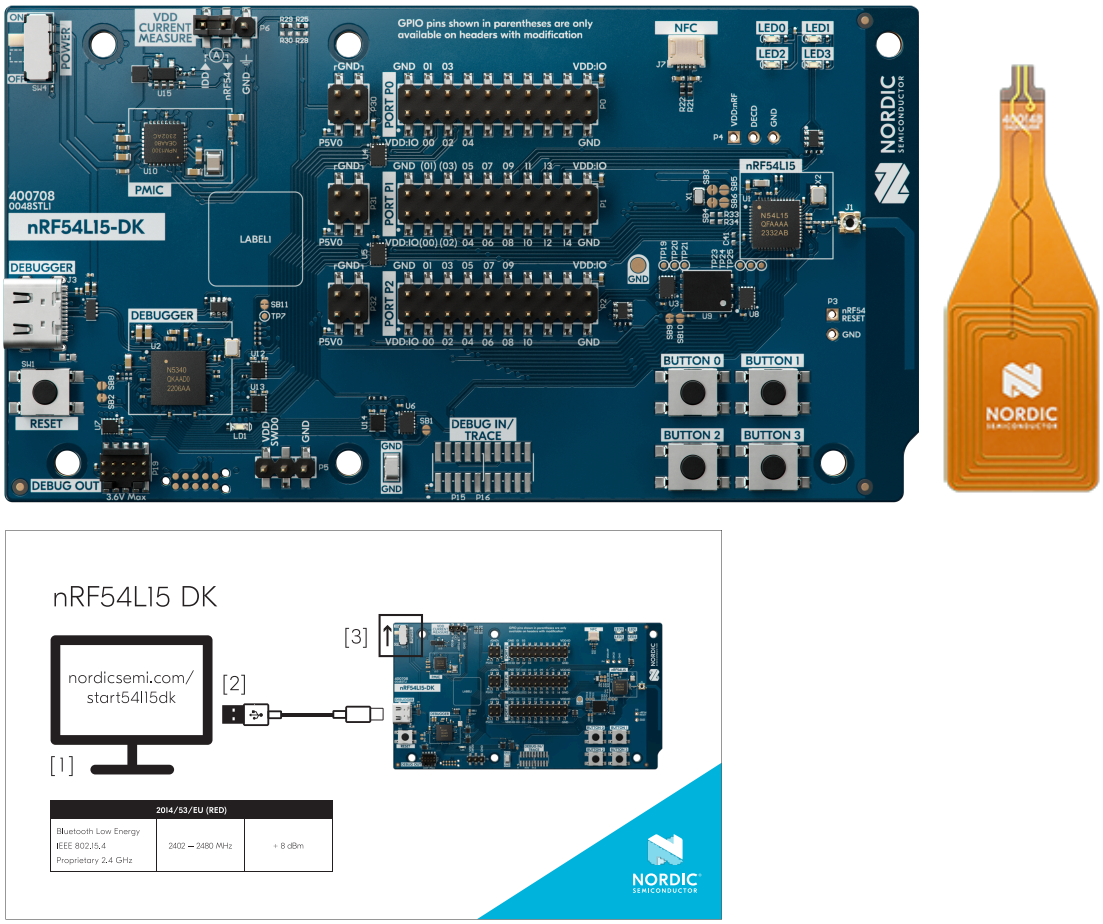

Figure 1: nRF54L15 DK kit content

The hardware design files for the nRF54L15 DK are available on the nRF54L15 DK product page. They include the following resources:

- Schematics
- *Printed Circuit Board (PCB)* layout files
- Bill of materials
- Gerber files

2 Hardware description

The main components of the nRF54L15 DK include the nRF54L15 SoC and hardware peripherals that add functionality and configuration options.

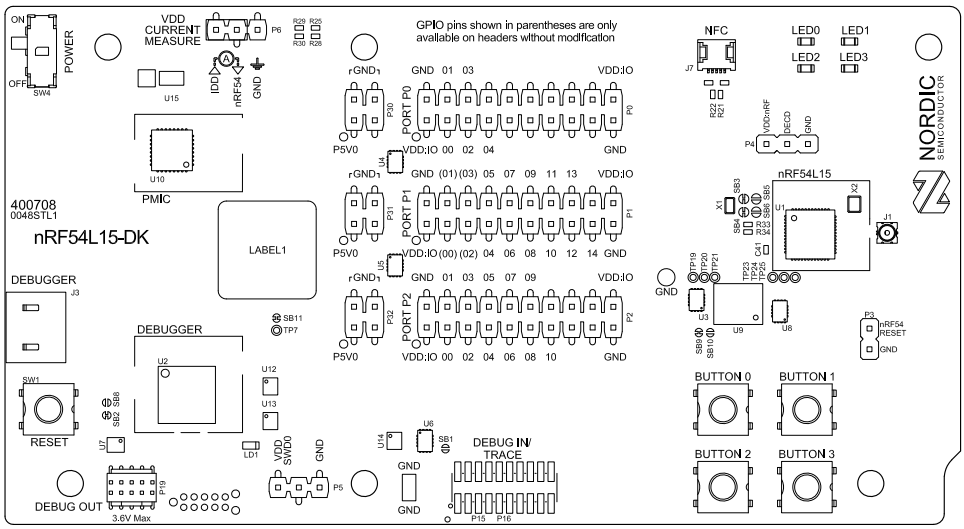

Figure 2: nRF54L15 DK front view

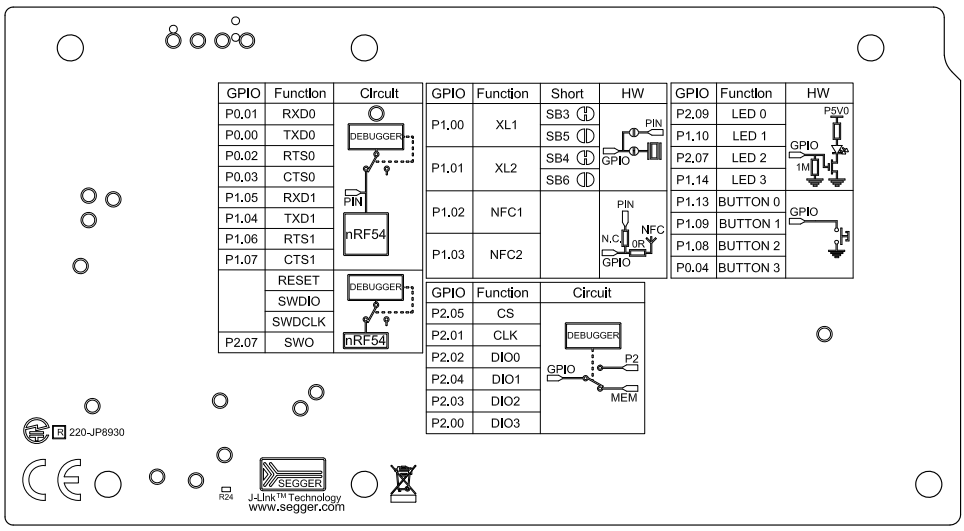

Figure 3: nRF54L15 DK back view

The following figure shows the dimensions of the nRF54L15 DK and the positions of the mounting holes in mm.

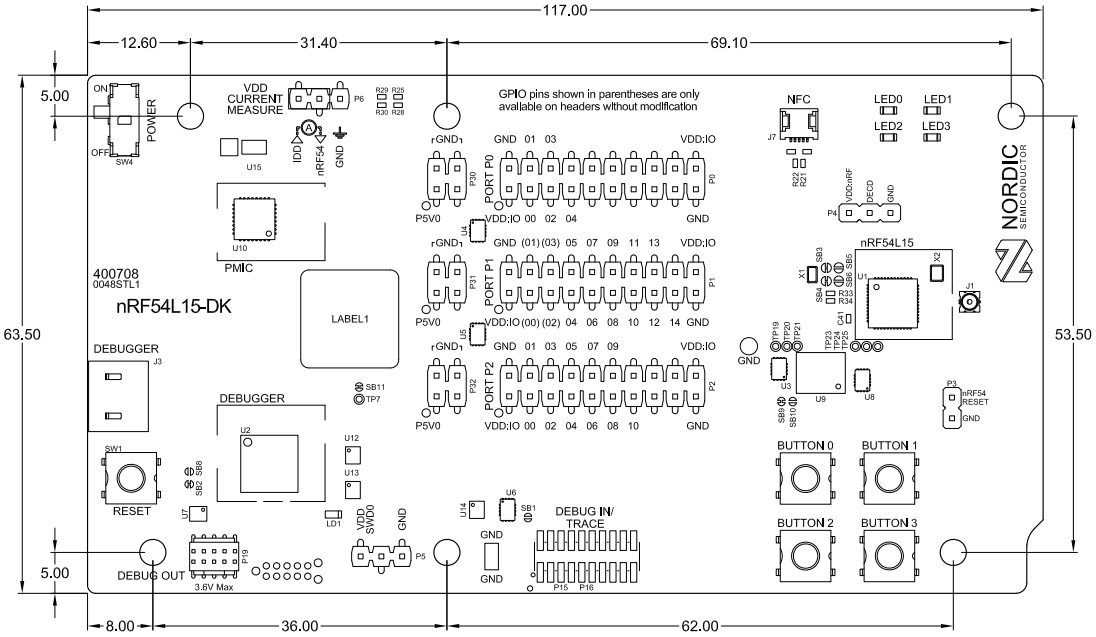

Figure 4: nRF54L15 DK dimensions in mm

2.1 Block diagram

The block diagram illustrates the nRF54L15 DK functional architecture.

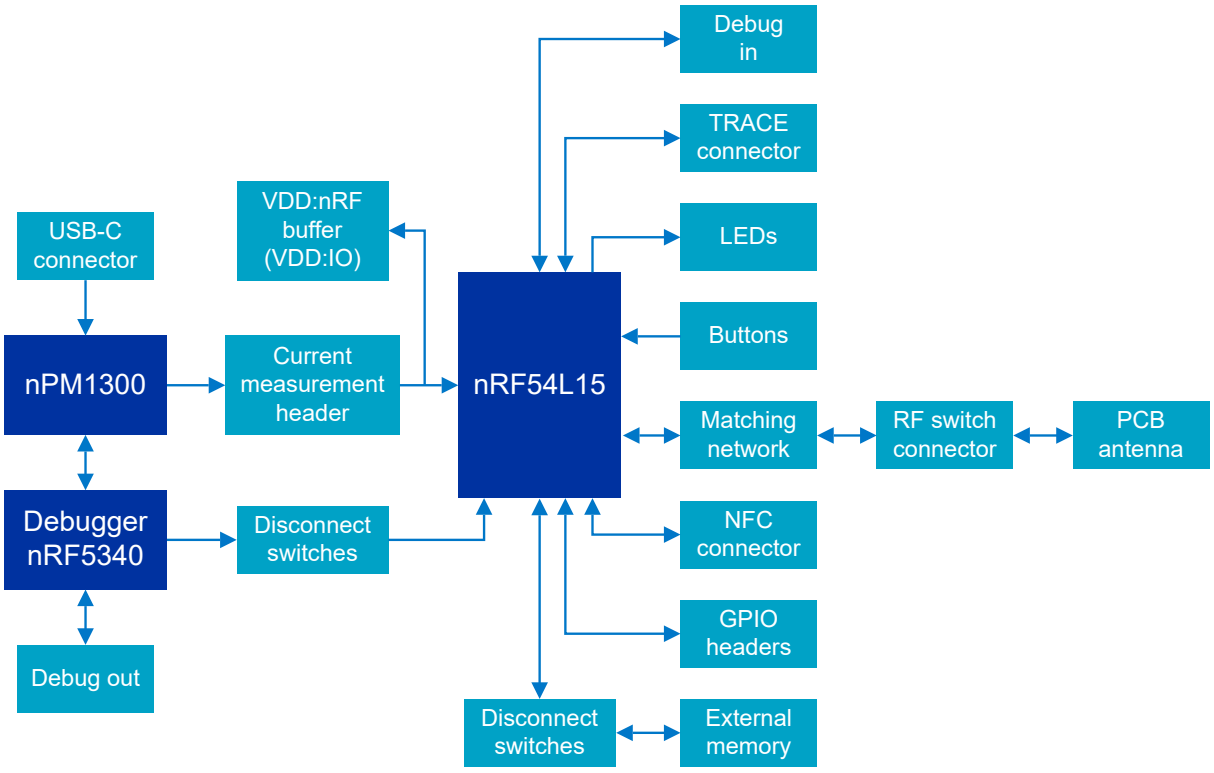

Figure 5: Block diagram

2.2 Power supply

The nRF54L15 DK is fully powered through the **J3** USB connector for the debugger (5 V).

The 5 V domain powers the main supply voltage (P5V0). The 5 V is supplied to the nRF54L15 DK from the **J3** USB connector.

The main power domains on the nRF54L15 DK are the following.

- nRF:VDD programmable voltage from 1.8 V to 3.3 V
- VDD:IO buffered nRF:VDD voltage

The nPM1300 PMIC supplies the nRF54L15 SoC VDD:nRF input with a default voltage of 1.8 V. To change the VDD:nRF voltage, use nRF Connect for Desktop's Board Configurator application.

The buffered VDD:nRF is called VDD:IO. The nRF54L15 DK uses the VDD:nRF voltage follower to make sure that leakage currents are not drawn from the nRF54L15 SoC device during low current measurements.

For more information about power sources, see nRF54L15 SoC external power with DK functionality on page 9.

2.2.1 nRF54L15 SoC external power with DK functionality

The nRF54L15 SoC can be powered directly from an external power source with the rest of the nRF54L15 DK being powered through the **J3** USB connector. This enables external supply for the nRF54L15 SoC while serial interfaces, LEDs, and buttons remain functional.

Remove the jumper from **P6** and connect an external power source to it. The allowed voltage range is from 1.8 V to 3.6 V.

Ensure that the nRF54L15 DK is powered through **J3** before powering on the nRF54L15 SoC through the **P6** external supply header to avoid damaging the onboard circuitry.

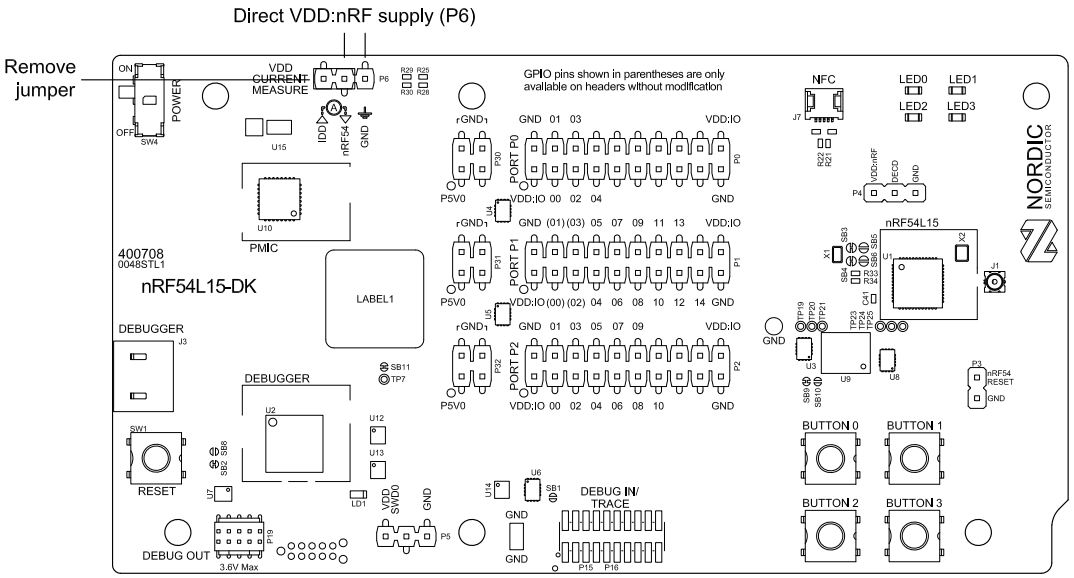

Figure 6: Direct VDD:nRF supply

2.2.2 nRF54L15 DK stand-alone external supply

The nRF54L15 DK can be manually configured to be supplied through the **P6** header without the need to supply power through the **J3** USB connector. In this configuration, the debugger, virtual serial ports, external flash, and LEDs are unavailable.

Remove the jumper from **P6** and connect an external power source to it. The allowed voltage range is from 1.8 V to 3.6 V.

The analog switches on the nRF54L15 DK must be reconfigured to disconnect the nRF54L15 SoC from the onboard debugger. Move the 0 Ω 0402 resistors from **R25** and **R29** to **R28** and **R30**.

2.3 GPIO interface

Access to the nRF54L15 SoC GPIOs is available from headers **P0**, **P1**, and **P2**.

The **P6** header and **P4** test points provide access to ground and power on the nRF54L15 DK.

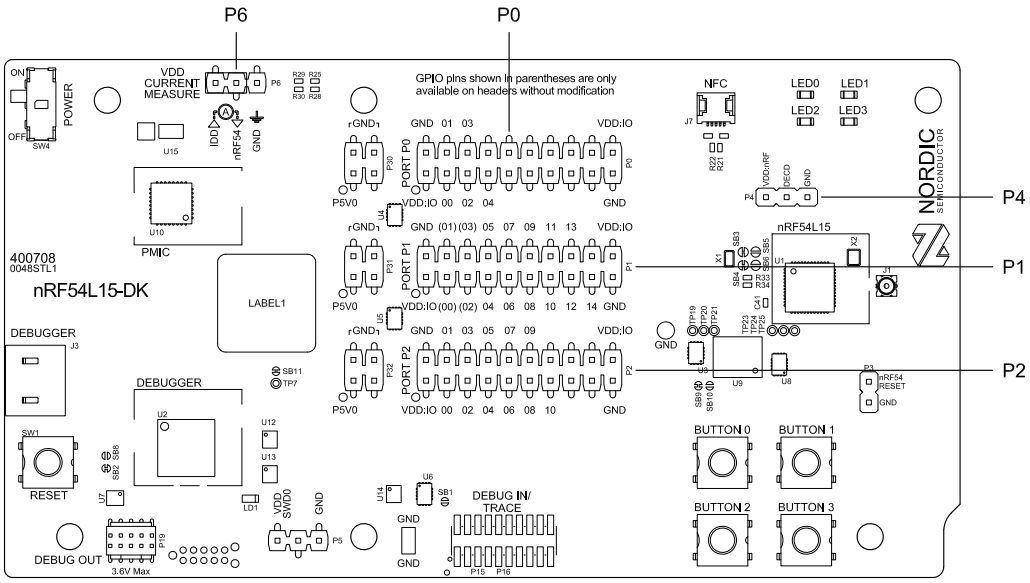

Figure 7: nRF54L15 DK GPIO headers

Pin maps

P0 signal	Function	Default connected on P0
P0.00	UART0_TXD	Yes
P0.01	UART0_RXD	Yes
P0.02	UART0_RST	Yes
P0.03	UART0_CST	Yes
P0.04	Button 3	Yes

Table 1: P0 pin map

P1 signal	Function	Default connected on P1
P1.00	32.768 kHz, XL1	No. Solder bridges must be configured.
P1.01	32.768 kHz, XL2	No. Solder bridges must be configured.
P1.02	NFC1	No. 0R resistors must be configured.
P1.03	NFC2	No. 0R resistors must be configured.
P1.04	UART1_TXD	Yes.
P1.05	UART1_RXD	Yes.
P1.06	UART1_RST	Yes.
P1.07	UART1_CTS	Yes.
P1.08	Button 2	Yes.
P1.09	Button 1	Yes.
P1.10	LED 1	Yes.
P1.11		Yes.
P1.12		Yes.
P1.13	Button 0	Yes.
P1.14	LED 3	Yes.

Table 2: P1 pin map

P2 signal	Function	Default connected on P2
P2.00	SPI_IO3/External flash	No. Board Configurator must be used.
P2.01	SPI_CLK/External flash	No. Board Configurator must be used.
P2.02	SPI_IO0/External flash	No. Board Configurator must be used.
P2.03	SPI_IO2/External flash	No. Board Configurator must be used.
P2.04	SPI_IO1/External flash	No. Board Configurator must be used.
P2.05	SPI_CS/External flash	No. Board Configurator must be used.
P2.06	Trace CLK	Yes.
P2.07	Trace [0]/LED 2	Yes.
P2.08	Trace [1]	Yes.
P2.09	Trace [2]/LED 0	Yes.
P2.10	Trace [3]	Yes.

Table 3: P2 pin map

Headers **P30**, **P31**, and **P32** are power supply pins that each provide 5.0 V for expansion boards connected to GPIO ports.

P30, P31, P32 signal	Function
1	P5V0 from PMIC
2	Ground
3	Do not connect
4	Ground

Table 4: P30, P31, and P32 signal map

2.4 External memory

The nRF54L15 DK has a 64 Mb external flash memory that can be connected to the nRF54L15 SoC. The memory is a multi-I/O memory supporting both *Serial Peripheral Interface (SPI)* and *Quad Serial Peripheral Interface (QSPI)*.

nRF Connect for Desktop's Board Configurator application can be used to select if the nRF54L15 SoC interfaces with the external memory or if the pins are available on the **P2** header. See the following figure for more information.

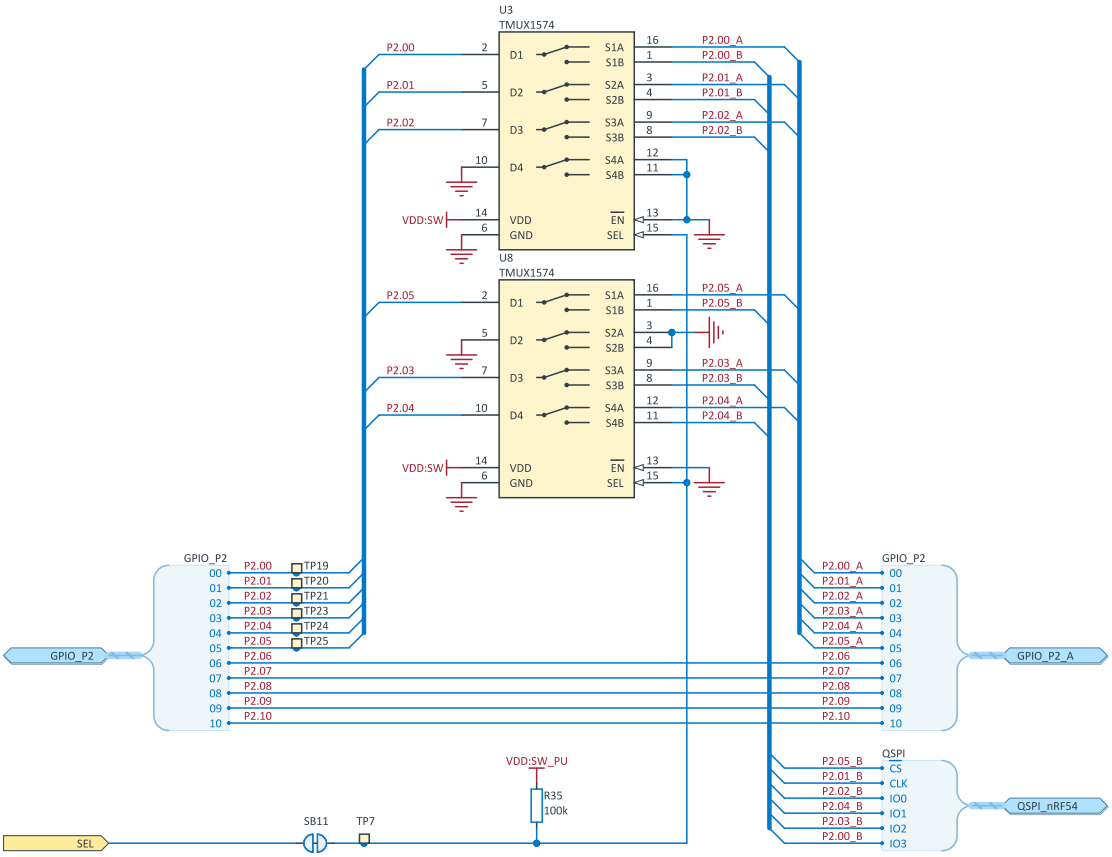

Figure 8: QSPI for external memory

Note: If debugging the QSPI communication is needed, use test points **TP19**, **TP20**, **TP21**, **TP23**, **TP24**, and **TP25**.

By default, the VDD:IO domain powers external memory. The power to the external memory can be configured to come from the VDD:nRF domain instead by cutting **SB9** and shorting **SB10**. If VDD:nRF is selected, the power consumption of the external memory is added to the nRF54L15 SoC current measured on **P6**.

2.5 Buttons and LEDs

The four buttons and four LEDs on the nRF54L15 DK are connected to dedicated GPIOs on the nRF54L15 SoC.

GPIO	Part
P1.13	Button 0
P1.09	Button 1
P1.08	Button 2
P0.04	Button 3
P2.09	LED 0
P1.10	LED 1
P2.07	LED 2
P1.14	LED 3

Table 5: Button and LED connections

The buttons are active low, which means that input is connected to ground when the button is pressed. The buttons do not have an external pull-up resistor. Pins **P0.04**, **P1.08**, **P1.09**, and **P1.13** must be configured as input with an internal pull-up resistor to register that a button is pressed.

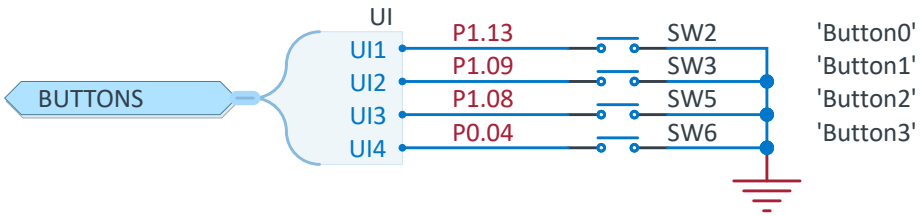

Figure 9: Button configuration

The LEDs are active high which means that writing a logical 1 to the output pin turns on the LED. For the implementation, see Figure 10: LED configuration on page 13.

The LEDs are powered by the nPM1300 PMIC. The power can be disabled using nRF Connect for Desktop's Board Configurator application. Activating the LEDs does not impact power measured on **P6**. Changing the nRF54L15 DK's operating voltage does not impact the intensity of the LEDs.

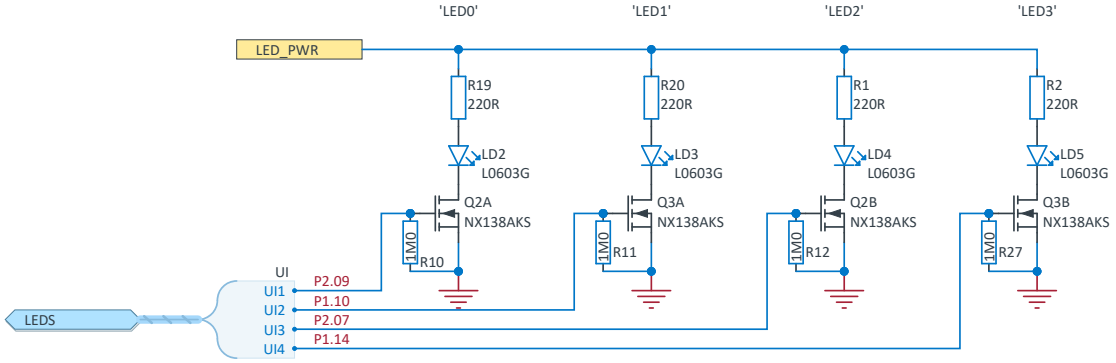

Figure 10: LED configuration

2.6 32.768 kHz crystal

The nRF54L15 SoC can use the optional 32.768 kHz crystal **X1** for lower average power consumption.

On the nRF54L15 DK, **P1.00** and **P1.01** are used for the 32.768 kHz crystal by default and are not available as GPIO on the headers.

By cutting solder bridges **SB3** and **SB4** and soldering **SB5** and **SB6** crystal **X1** is disconnected and GPIOs **P1.00** and **P1.01** are connected to the header for general use.

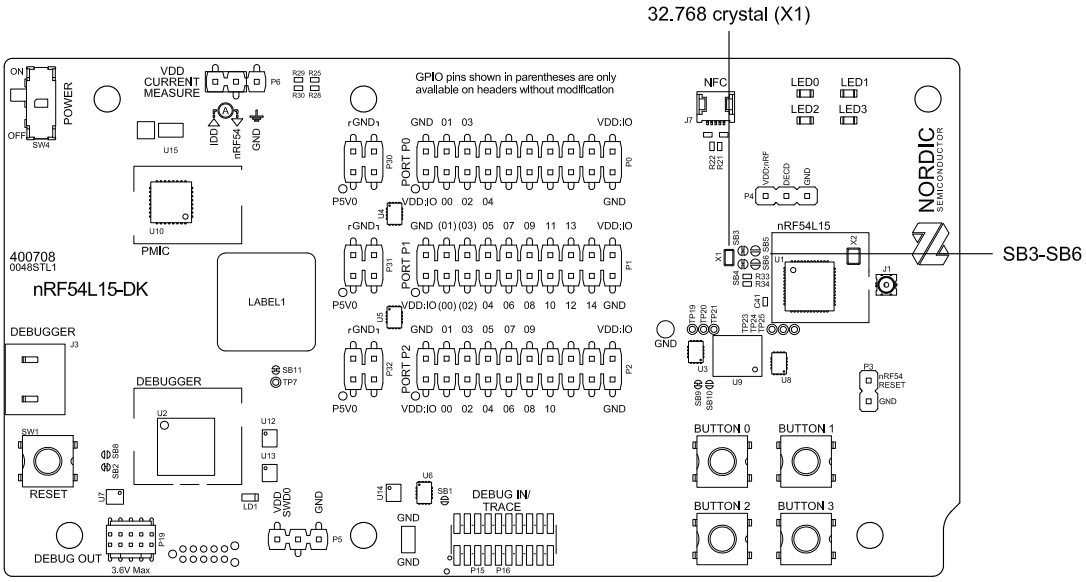

Figure 11: 32.768 kHz crystal X1 and SB3–SB6

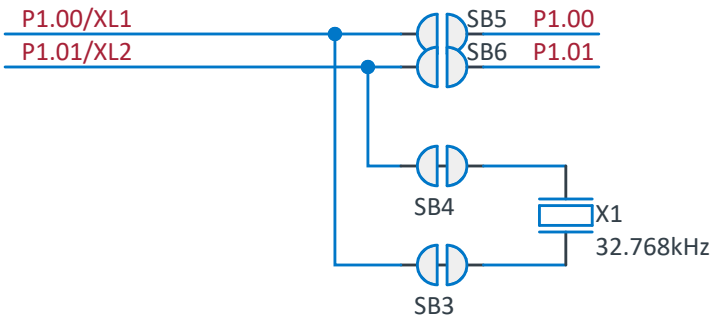

*Figure 12: 32.768 kHz crystal and **SB3–SB6***

2.7 NFC antenna interface

The nRF54L15 DK supports an NFC tag.

NFC-A Listen Mode operation is supported on the nRF54L15 SoC. The NFC antenna input is available on connector **J7** on the nRF54L15 DK.

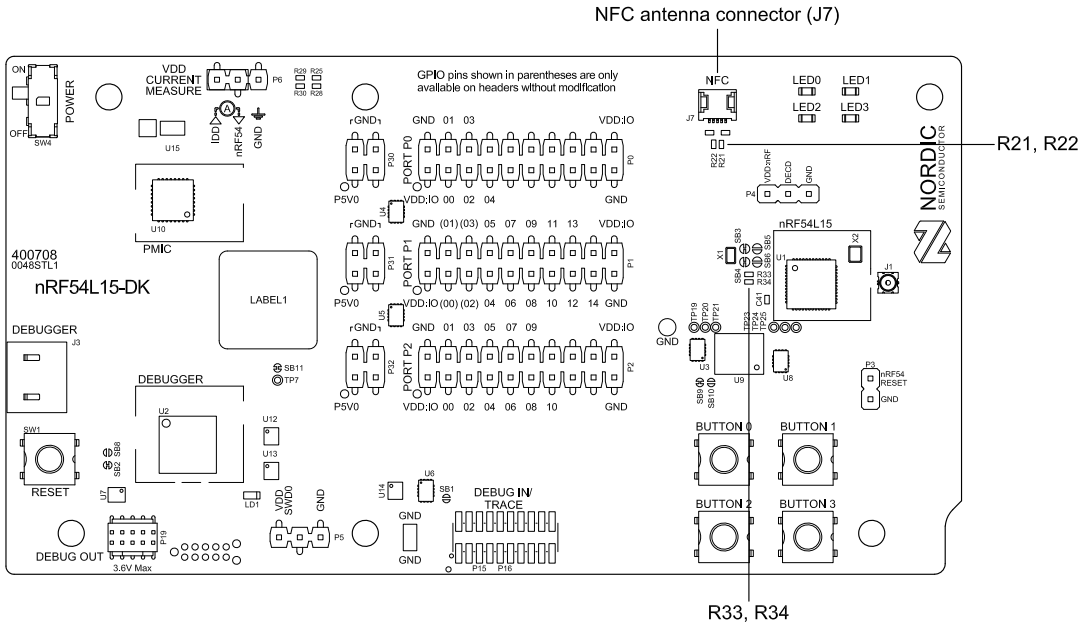

Figure 13: NFC antenna connector

Pins **P1.02** (**NFC1**) and **P1.03** (**NFC2**) are by default configured to use the NFC antenna. The PROTECT field of the NFCPINS register in *User Information Configuration Registers (UICR)* defines the usage of these pins and their protection level against abnormal voltages. The content of the NFCPINS register is reloaded at every reset.

Configuring NFC pins as GPIOs

To use pins **P1.02** (**NFC1**) and **P1.03** (**NFC2**) as GPIOs, move the 0 Ω 0402 resistors from **R21** and **R22** to **R33** and **R34**. Disable the NFC peripheral by setting CONFIG_NFCT_PINS_AS_GPIOS to `y`. See Configuring and building for instructions.

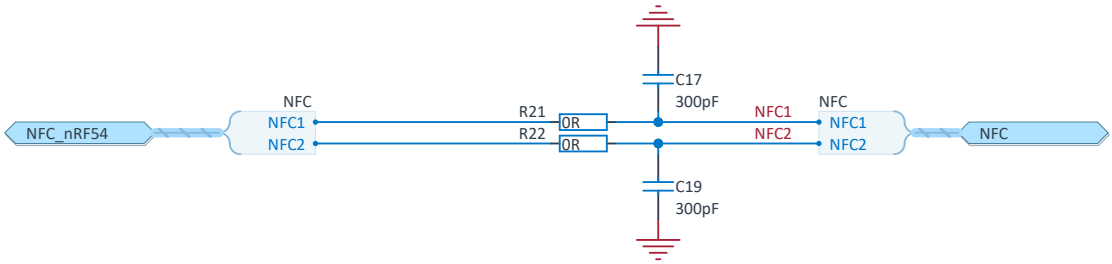

Figure 14: NFC network

2.8 Solder bridge configuration

The nRF54L15 DK has a range of solder bridges for enabling or disabling functionality on the nRF54L15 DK.

When cutting a closed solder bridge to make it open, be careful not to damage other parts of the nRF54L15 DK.

The following table is an overview of the solder bridges on the nRF54L15 DK.

Solder bridge	Default	Function
SB1	Open	Short to connect RESET button line to nRF54L15.

Solder bridge	Default	Function
SB2	Closed	Cut to disconnect debugger from the RESET button line.
SB3	Closed	Cut to disconnect the 32.768 kHz from **P1.00**.
SB4	Closed	Cut to disconnect the 32.768 kHz from **P1.01**.
SB5	Open	Short to enable **P1.00** as GPIO.
SB6	Open	Short to enable **P1.01** as GPIO.
SB8	Open	Short **R23**, 100 k pull-up resistor to the RESET button line.
SB9	Closed	Cut to disconnect VDD:IO from **U9** external flash power.
SB10	Open	Short to connect **U9** external flash to VDD:nRF domain.
SB11	Closed	Cut to connect **U9** permanently to the nRF54L15 SoC.

Table 6: Solder bridge configuration

2.9 Board control

The debugger contains a board controller that controls the power supply voltage and signals which enable and disable features on the nRF54L15 DK.

All features on the nRF54L15 DK have a default factory setting when they are dispatched from Nordic. The default setting is applied at the first boot. The configuration of the board controller can be changed through nRF Connect for Desktop's Board Configurator application. If the configuration is modified from the default factory setting, the board controller loads the modified configuration every time the nRF54L15 DK is restarted.

For more information, see Board Configurator app.

3 Program and debug

The debugger on the nRF54L15 DK programs and debugs the nRF54L15 SoC application firmware.

3.1 Debugger

The debugger on the nRF54L15 DK runs SEGGER J-Link *Onboard (OB)* interface firmware.

3.1.1 RESET button

The nRF54L15 DK is equipped with a RESET button **SW1** connected to the debugger. The debugger reads the status of the RESET_BUTTON signal and resets the nRF54L15 SoC through the *Serial Wire Debug (SWD)*. Devices directly connected to the RESET_BUTTON signals through programming connectors are reset directly.

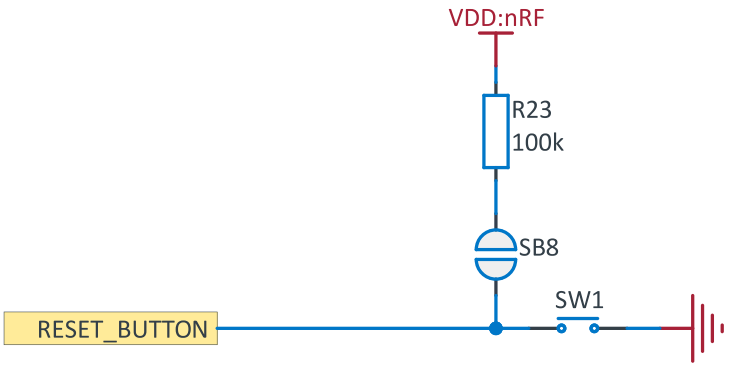

Figure 15: nRF54L15 DK RESET button

The RESET button can be connected directly to the nRF54L15 SoC by cutting the **SB2** solder bridge and then soldering the **SB1** solder bridge.

> **Note:** Pull-up resistor **R23** is for internal use only. Do not short solder bridge **SB8**.

3.1.2 Virtual serial ports

The debugger has two virtual serial ports. Each of them has a *UART* interface.

The serial ports have the following features:

- Flexible baud rate setting up to 1 Mbps (baud rate 921,600 bps is not supported)
- Optional *Hardware Flow Control (HWFC)* pins
- Automatic detection of HWFC if flow control pins are connected
- Tri-stated UART lines when no terminal is connected

The following table lists the nRF54L15 SoC's UART GPIO pins and their signals.

Signal	nRF54L15 SoC UART_0 - Serial Port 0	nRF54L15 SoC UART_1 - Serial Port 1
TXD	P0.00	P1.04
RXD	P0.01	P1.05
RTS	P0.02	P1.06
CTS	P0.03	P1.07

Table 7: nRF54L15 SoC GPIOs mapped to serial port/UART signals

The UART pins connected to the debugger are tri-stated when no terminal is connected to the virtual serial port on the computer. The terminal software must send a *Data Terminal Ready (DTR)* signal to configure the debugger UART pins.

P0.02/P1.06 *Request to Send (RTS)* and **P0.03/P1.07** *Clear to Send (CTS)* can be used for other purposes when HWFC is disabled on the nRF54L15 SoC.

The UART signals are routed to the debugger through analog switches **U4** and **U5**.

UART pins for other tasks

For each UART instance, the TXD/RXD signals can be disconnected from the debugger as a group. For the UARTs in use, the RTS/CTS signals can be connected and disconnected from the debugger as a group depending on the HWFC usage. This can be done through nRF Connect for Desktop's Board Configurator application.

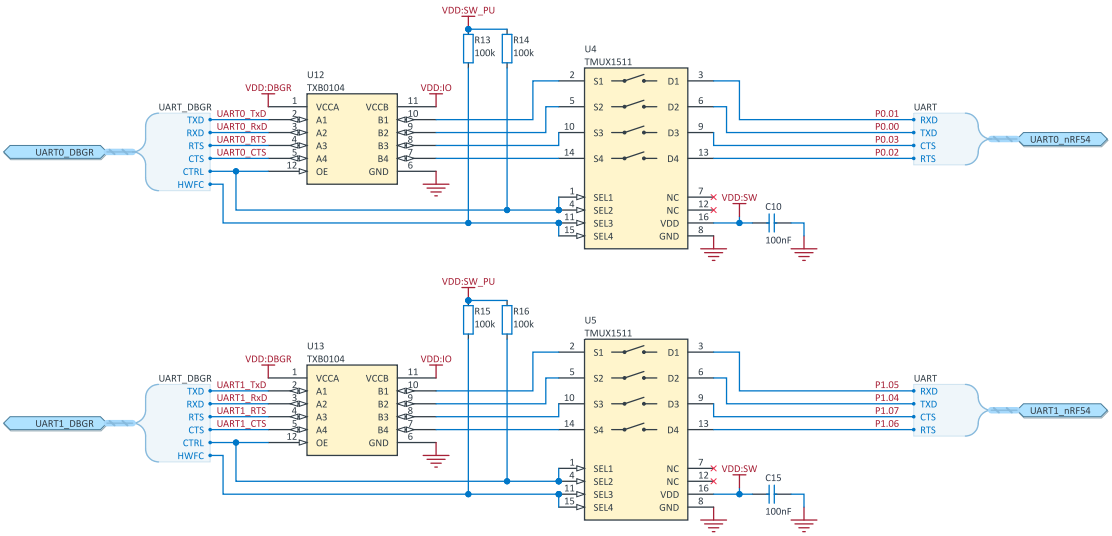

Figure 16: Analog switches between debugger and nRF54L15 DK

3.1.3 Dynamic hardware flow control

When the debugger receives a *DTR* signal from a terminal, it performs automatic *HWFC* detection.

HWFC detection

Automatic HWFC detection is done by driving *CTS* from the debugger and evaluating the state of *RTS* when data is first sent or received. If the state of RTS is high, it is assumed HWFC is not in use. If HWFC is not detected, pins **P0.03/P1.07** (CTS) and **P0.02/P1.06** (RTS) are free for the nRF application to use.

After a power-on reset of the debugger, all UART lines are tri-stated when no terminal is connected to the virtual serial port. If HWFC has been used and detected, **P0.03/P1.07** (CTS) is driven by the debugger

until a power-on reset has been performed or until a new DTR signal is received and the detection is redone.

The debugger has a pull-down 100 kΩ resistor connected from CTS to ground.

3.2 Debug input and trace

Use the Debug In header **P15** to connect external debuggers.

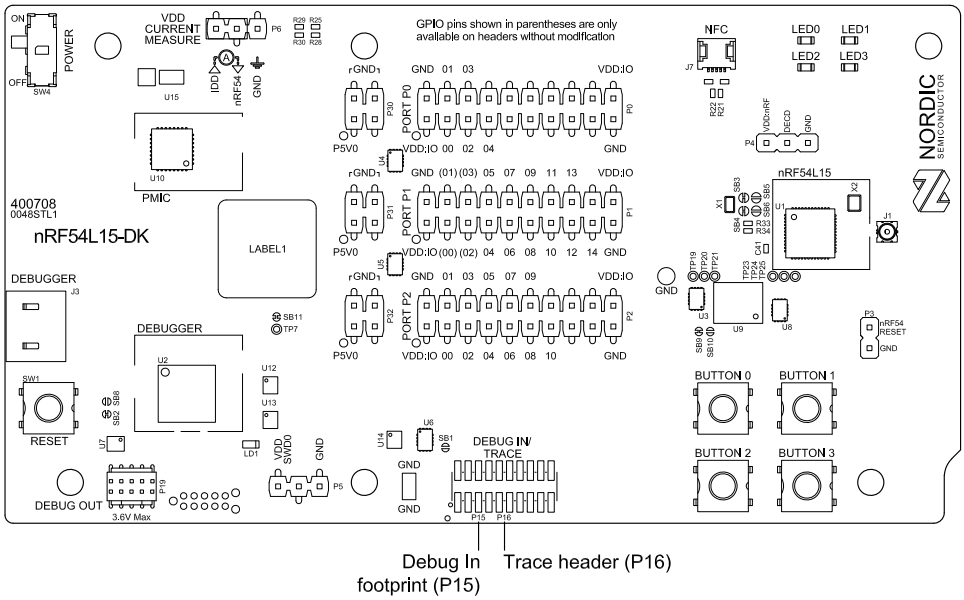

Figure 17: Debug input and trace headers

For trace, a 20-pin header footprint **P16** is available. If trace functionality is required, it is possible to mount a 1.27 mm 2x10 pin pitch surface-mount pin header.

GPIO	Trace	Default use
P2.06	TRACECLK	
P2.07	TRACEDATA[0]	LED2
P2.08	TRACEDATA[1]	
P2.09	TRACEDATA[2]	LED0
P2.10	TRACEDATA[3]	

Table 8: Default and Trace GPIOs

The reference voltage for the debug input and trace is connected to **VDD:IO**.

3.3 Debug out for programming external boards

The nRF54L15 DK supports the programming and debugging of external boards with the nRF51 Series, nRF52 Series, nRF53 Series, and nRF54 Series SoCs and nRF91 Series SiPs.

To program or debug an external board, connect it to the **P19** Debug out header with a 10-pin cable. The external board can be powered by supplying power to the **P5** pin 3 labeled **VDD SWD0**.

Note: The programming cable used to connect the external board must be no longer than 10 cm. To prevent damaging the nRF54L15 DK or the external board, ensure that the external board is powered from only one source: either **P5** or an external power source. The VDD of the external board voltage must be within the range of 1.8 V and 3.6 V.

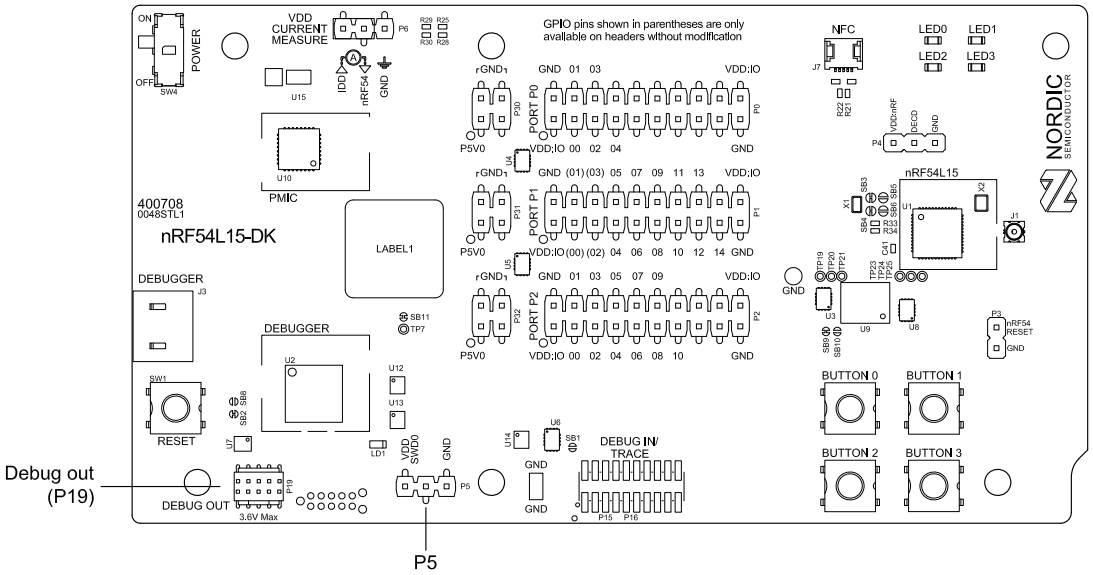

Figure 18: Debug output header

The following table describes the pinout of the **P19** header.

Pin number	Signal	Description
1	SWD0_VTG	I/O voltage reference input for SWD0 signals or power supply to external board.
2	SWD0_SWDIO	SWD data I/O.
3	SWD0_SELECT	Debug out select signal. Connect to ground on the external board.
4	SWD0_SWDCLK	Serial Wire Clock line.
5	GND	Ground.
6	SWD0_SW0	*Serial Wire Output (SWO)* line is not used for programming and debugging over SWD.
7	N.C.	Not used.
8	N.C.	Not used.
9	N.C.	Not used.
10	SWD0_RESET	Reset line.

*Table 9: Header **P19** pinout for programming external targets*

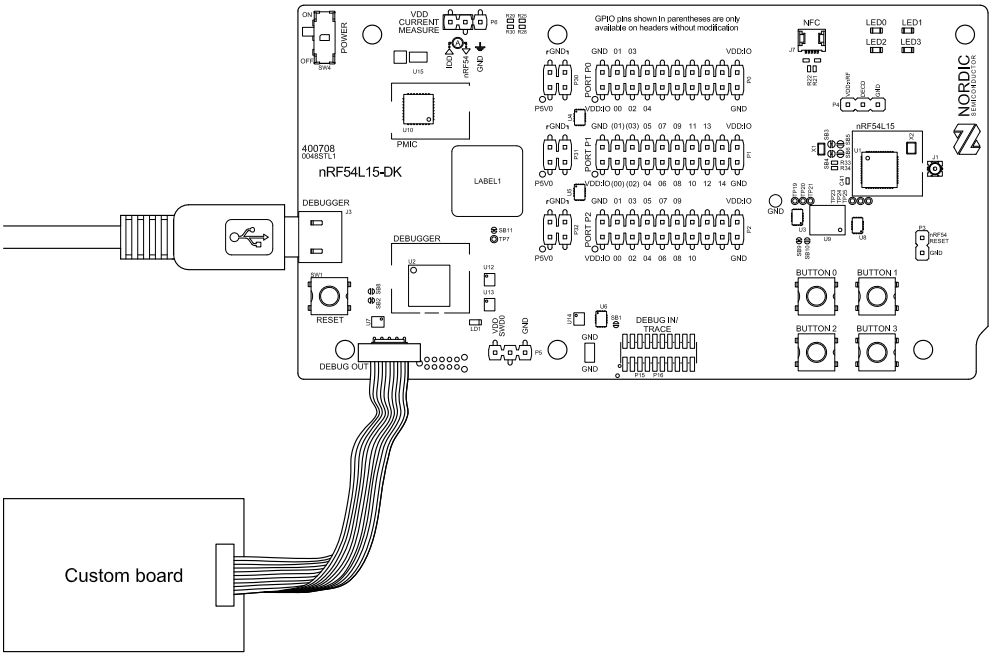

Figure 19: Connecting an external board to P19

4 Measurements

Current and RF signal can be measured on the nRF54L15 DK.

4.1 Current measurements

The current drawn by the application nRF54L15 SoC can be monitored on the nRF54L15 DK.

Current can be measured using any of the following test instruments:

- Power Profiler Kit II (PPK2)
- Oscilloscope
- Ampere meter
- Power analyzer

The following sections provide information on the nRF54L15 DK measurement setup. If the PPK2 is used for measuring current, see Power Profiler Kit II for more information. Power analyzer measurements are not described in this document.

The nRF54L15 DK can measure current on VDD:nRF using **P6**.

> **Note:** The measurement readings might introduce noise if the virtual serial port is open.

For more information on current measurement, see Current measurement guide: Introduction.

4.1.1 Set up the DK

Perform the following tasks to set up the nRF54L15 DK for minimal current consumption.

- Disconnect the virtual serial ports as described in Virtual serial ports on page 17.
- If a circuitry is connected to the **P19** Debug out header, disconnect it.
- Remove the jumper from the **P6** header.

To reprogram the nRF54L15 SoC while the nRF54L15 DK is prepared for current measurements, replace the measurement devices on **P6** with the jumper.

4.1.2 Measure current profile with an oscilloscope

An oscilloscope can be used to measure the average current over a given time interval and capture the current profile.

1. Prepare the nRF54L15 DK as described in Set up the DK.
2. Mount a 10 Ω ±0.1% 0402 resistor to **R24** which is located at the back of the nRF54L15 DK.
3. Set the oscilloscope to differential mode or a mode that is similar.
4. Connect the oscilloscope using two probes on the pins of the **P6** header, as shown in the following figure.
5. Calculate or plot the instantaneous current from the voltage drop across the **R24** resistor by taking the difference of the voltages measured on the two probes.

   The voltage drop is proportional to the current. The 10 Ω resistor causes a 10 mV drop for each 1 mA drawn by the circuit being measured.

The plotted voltage drop can be used to calculate the current at a given point in time. The current can then be averaged or integrated to analyze current and energy consumption over a period.

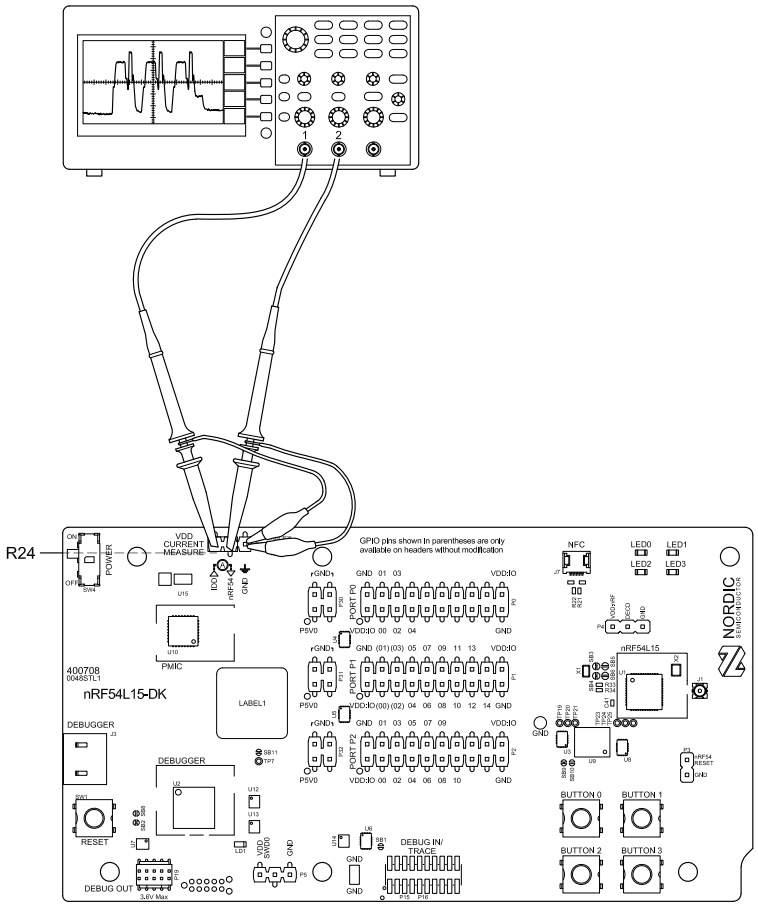

Figure 20: Current measurement with an oscilloscope

To reduce noise, do the following:

- Use GND leads that are as short as possible.
- Use probes with 1x attenuation.
- Enable averaging mode to reduce random noise.
- Enable high-resolution function if it is available.

Use a minimum of 200 kSa/s (one sample every 5 µs) to get the correct average current measurement.

4.1.3 Measure average current with an ampere meter

The average current drawn by the application nRF54L15 SoC can be measured using an ampere meter. This method monitors the current in series with the nRF device. A true *Root Mean Square (RMS)* ampere meter is recommended.

1. Prepare the nRF54L15 DK as described in Set up the DK.
2. Connect an ampere meter between the pins of header **P6** as shown in the following figure.
3. Set the average timing of the ampere meter to a long interval, such as 1 s or longer.
4. Set the dynamic range of the ampere meter between 1 µA and 15 mA, so that it is wide enough to provide accurate measurements.

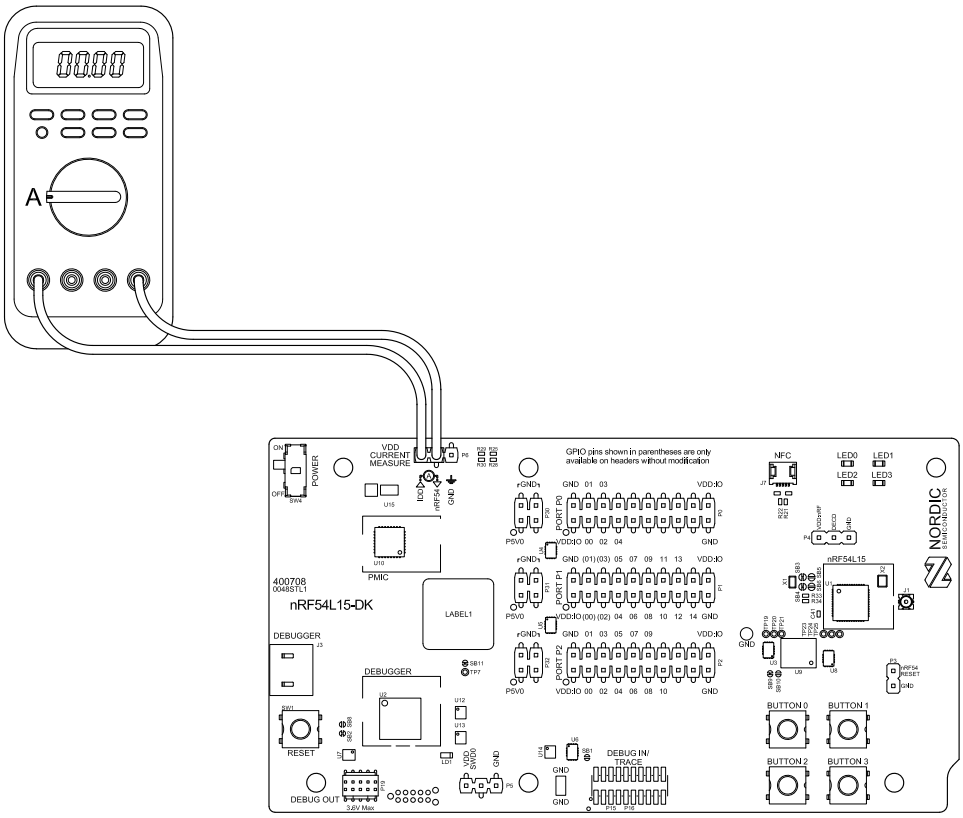

Figure 21: Current measurement with an ampere meter

4.2 RF measurements

The nRF54L15 DK is equipped with a small coaxial connector (**J1**) to measure the RF signal with a spectrum analyzer.

The connector is an SWF type (Murata part no. MM8130-2600) with an internal switch. By default, when a cable is not attached, the RF signal is routed to the onboard trace antenna.

In this example, a test probe (Murata part no. MXHS83QE3000) is used with a standard *SubMiniature Version A (SMA)* connection on the other end for connecting instruments. The test probe is not included in the kit. When connecting the test probe, the internal switch in the SWF connector disconnects the onboard antenna and connects the RF signal from the nRF54L15 SoC to the test probe.

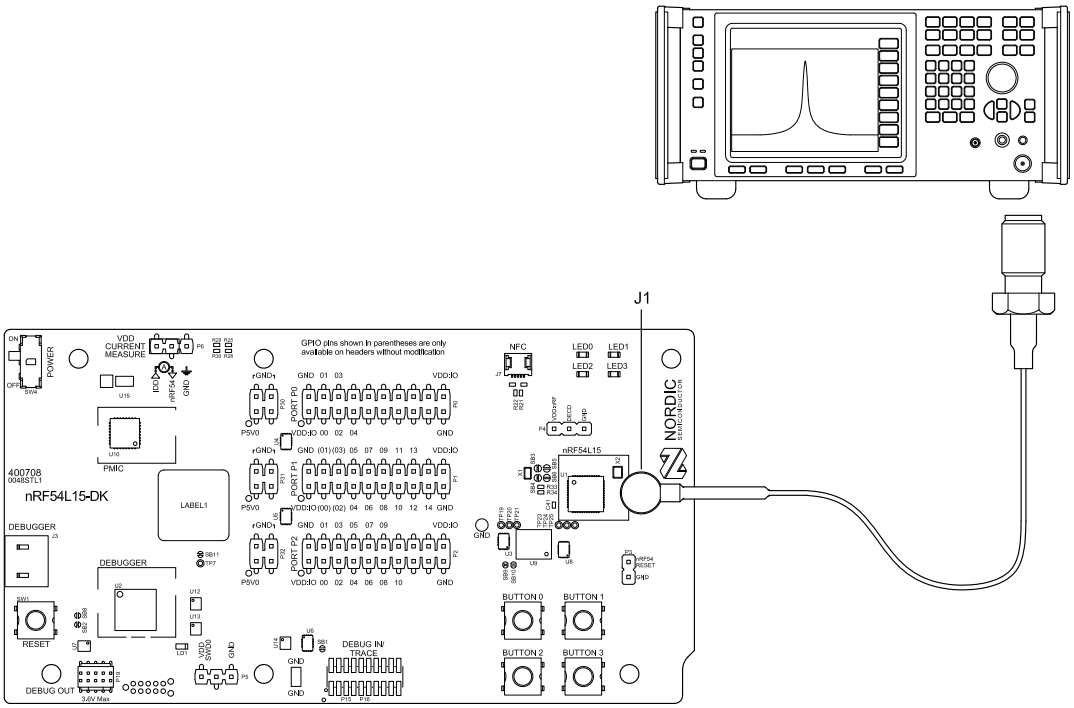

Figure 22: Connecting a spectrum analyzer

The connector and test probe add loss to the RF signal. See the following table for more information or consult the test probe user guide if you are using another model.

Frequency (MHz)	Loss (dB)
2440	1.0
4880	1.7
7320	2.6

Table 10: Typical loss in connector and test probe, using Murata part no. MXHS83QE3000

5 Regulatory information

The nRF54L15 DK is CE certified to operate in the EU and the UK.

The nRF54L15 DK is MIC certified to operate in Japan. Its MIC ID is 220-JP8930.

当該機器には電波法に基づく、技術基準適合証明等を受けた特定無線設備を装着している。

Translation: "This equipment contains specified radio equipment that has been certified to the Technical Regulation Conformity Certification under the Radio Law."

Glossary

Clear to Send (CTS)

In flow control, the receiving end is ready and telling the far end to start sending.

Data Terminal Ready (DTR)

A control signal in RS-232 serial communications transmitted from data terminal equipment, such as a computer, to data communications equipment.

Development Kit (DK)

A hardware development platform used for application development.

Electrostatic Discharge (ESD)

A sudden discharge of electric current between two electrically charged objects.

Hardware Flow Control (HWFC)

A handshaking mechanism used to prevent an overflow of bytes in modems. It uses two dedicated pins on the RS-232 connector, Request to Send and Clear to Send.

Integrated Circuit (IC)

A semiconductor chip consisting of fabricated transistors, resistors, and capacitors.

Lithium-polymer (Li-Poly)

A rechargeable battery of lithium-ion technology using a polymer electrolyte instead of a liquid electrolyte.

Mass Storage Device (MSD)

Any storage device that makes it possible to store and port large amounts of data in a permanent and machine-readable fashion.

Microwave coaxial connector with switch (SWF)

A small, RF surface-mount switch connector series for wireless applications.

NFC-A Listen Mode

Initial mode of an NFC Forum Device when it does not generate a carrier. The device listens for the remote field of another device. See Near Field Communication (NFC).

Onboard (OB)

A function that is delivered on the chip microcontroller.

Operational Amplifier (op-amp)

A high-gain voltage amplifier that has a differential input and, usually, a single output.

Power Management Integrated Circuit (PMIC)

A chip used for various functions related to power management.

Printed Circuit Board (PCB)

A board that connects electronic components.

Quad Serial Peripheral Interface (QSPI)

A Serial Peripheral Interface (SPI) controller that allows the use of multiple data lines.

Receive Data (RXD)

A signal line in a serial interface that receives data from another device.

Request to Send (RTS)

In flow control, the transmitting end is ready and requesting the far end for a permission to transfer data.

Root Mean Square (RMS)

An RMS meter calculates the equivalent Direct Current (DC) value of an Alternating Current (AC) waveform. A true RMS meter can accurately measure both pure waves and the more complex nonsinusoidal waves.

Serial Peripheral Interface (SPI)

Synchronous serial communication interface specification used for short-distance communication.

Serial Wire Debug (SWD)

A standard two-wire interface for programming and debugging Arm® CPUs.

Serial Wire Output (SWO)

A data line for tracing and logging.

SubMiniature Version A (SMA)

A semi-precision coaxial RF connector for coaxial cables with a screw-type coupling mechanism.

System in Package (SiP)

Several integrated circuits, often from different technologies, enclosed in a single module that performs as a system or subsystem.

System on Chip (SoC)

A microchip that integrates all the necessary electronic circuits and components of a computer or other electronic systems on a single integrated circuit.

Transmit Data (TXD)

A signal line in a serial interface that transmits data to another device.

Universal Asynchronous Receiver/Transmitter (UART)

A hardware device for asynchronous serial communication between devices.

Universal Serial Bus (USB)

An industry standard that establishes specifications for cables and connectors and protocols for connection, communication, and power supply between computers, peripheral devices, and other computers.

User Information Configuration Registers (UICR)

Non-volatile memory registers used to configure user-specific settings.

Recommended reading

In addition to the information in this document, you may need to consult other documents.

Nordic documentation

- nRF54L15 | nRF54L10 | nRF54L05 Preliminary Datasheet
- nRF54L15 Errata

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