RVP001 Transformer Driver for Micro-power Isolated Supplies

3-6VIN/0.5A Power Switch

FEATURES

- Full Bridge Topology
- Highly Integrated, Simple Solution
- Built-in 0.13Ω NMOS
- Built-in 0.25Ω PMOS
- 0.9A Current Clamp Limit
- 3-6V Input Voltage Range
- Surge Voltage up to 10V
- Input Overvoltage Protection
- Continuous Short-circuit Protection, Over-temperature Protection, Self-recovery
- Ambient: -40°C~+125°C

APPLICATIONS

- Low-power Isolated Power Supply for CAN/RS-485/RS-232/SPI/I2C
- Process Control
- Precision/Medical Equipment
- Distributed/Radio/Telecom Power Supplies
- Low Noise Isolated USB Power Supplies
- Low Noise Filament Power Supplies
- IGBT Gate-Drive Power Supplies

DESCRIPTION

RVP001 is a transformer driver specifically designed for compact, micropower isolated power supplies requiring low standby power consumption. It requires only simple input/output filter capacitors, an isolation transformer, and rectifier circuitry to form a complete isolated power supply with a 3-6V input range, multiple output voltage options, and output power of up to 2W.

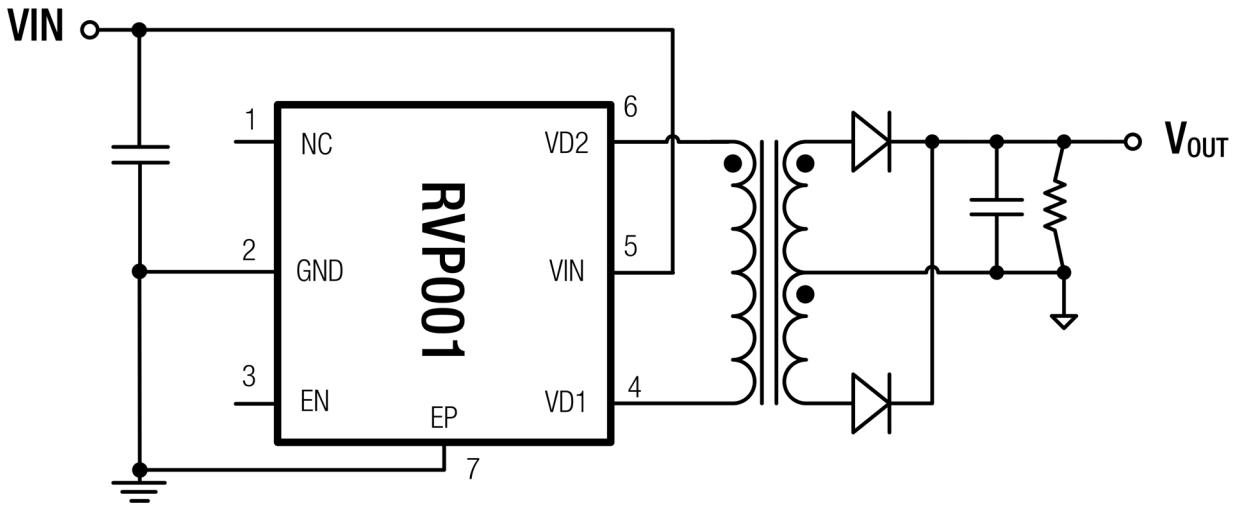
RVP001 integrates two N-channel and two P-channel MOSFETs in a full-bridge configuration. An internal oscillator generates a pair of high-precision complementary signals that ensure symmetrical switching, thereby minimizing magnetic bias during operation.

To enhance system reliability, the RVP001 incorporates multiple protection features. A high-precision dead-time control circuit ensures break-before-make switching to prevent cross-conduction under varying operating conditions. The device also includes overcurrent detection and overtemperature protection, safeguarding against abnormal events such as output short circuits in the switching power supply.

Device Information

Part Number	Packaging	Weight(mg)	Size	SPQ
RVP001	DFN2x2-6	10.38	2.0mm x 2.0mm	3000

SIMPLIFIED SCHEMATIC



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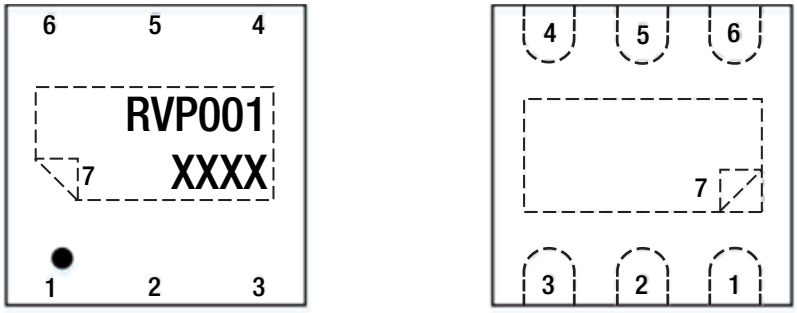
PIN CONFIGURATION AND FUNCTIONS



Name	No.	Type	Description
NC	1	-	Not connected pin.
GND	2	P	Logic circuit ground and analog circuit ground.
EN	3	I	Enable pin. The chip stops operating when the pin voltage is at low potential and operates normally when it is not connected or at high potential.
VD1	4	O	Transformer drive output 1.
VIN	5	I	Power input, VIN to GND with a 1uF capacitor; place the capacitor as close to the device as possible.
VD2	6	O	Transformer drive output 2.
EP	7	P	Exposed pad, connected to EP and GND to enhance heat dissipation. Multi-layer boards are recommended to add through holes. Exposed pads are not used as electrical connection points.

SPECIFICATIONS

Absolute Maximum Ratings

		MIN	MAX	UNIT
VIN Input Voltage	V_{IN}	-0.3	10	V
LDMOS Drain Voltage	VD1, VD2	-0.3	V_{IN} +0.3	
EN/CLK Pin Voltage	EN, CLK	-0.3	6.6	V
Peak Junction Temperature	T_{JMAX}		150	°C
Storage Temperature Range	T_{STG}	-55	150	°C

Stress exceeding the absolute maximum rated value may cause permanent damage to the device. These are only stress ratings and do not imply that the device operates beyond the recommended operating conditions under these or any other conditions. Long term exposure to absolute maximum rated conditions may affect the reliability of the device. All voltages are related to grounding. The current is positive input and negative output.

ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostactic discharge	Human body model HBM, per ESDA/JEDEC JS-001-2017; (Zap 1 pulse, Interval :>=0.1S)	±4000	V
		Charged device model CDM, per ESDA/JEDEC JS-002-2014	±1000	V

Thermal Resistance

Packaging	θ_{JA}	Ψ_{JT}	UNIT
DFN2x2-6	90	5.2	°C/W

Note: Measured on a test board with 1oz copper (7.62cm × 11.43cm).

Recommended Operatings Conditions

		MIN	TYP	MAX	UNIT
VIN Input Voltage	V_{IN}	3		6	V
Output Switch Current	I_{VD1}, I_{VD2}			0.5	A
Ambient Temperature	T_A	-40		125	°C

Electrical Characteristics

If not specified, the following parameters are measured at VIN=5V and temperature T=25°C.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input Pin VIN						
V_{IN}	Input voltage range		3.0		6.0	V
$V_{IN(ON)}$	Start up voltage	EN unconnected, V_{IN} rising	2.6	2.8	3.0	V
$V_{IN(HYS)}$	Hysteresis voltage	EN unconnected, V_{IN} falling		0.17		V
I_Q	VIN quiescent current	VD1, VD2, CLK, EN unconnected	0.6	1.0	1.6	mA
$I_{VIN\ (EN)}$	VIN current for EN=0	EN=0, V_{IN}=5V		5	10	µA
$V_{IN(OVP)}$	Overvoltage protection threshold	V_{IN} rises to VD1 and VD2 stops driving	7.0	7.8	8.2	V
$V_{INHYS(OVP)}$	Input overvoltage protection hysteresis voltage	V_{IN} drops to VD1 and VD2 starts driving		0.5		V
Enable Pin EN						
$V_{EN(ON)}$	EN pin logic high threshold	V_{EN} rising	1.6	2.24	2.8	V
$V_{EN(HYS)}$	EN Pin logic low threshold	V_{EN} falling		1.14		V
$R_{EN(ON)}$	Pull-up resistor after opening	$V_{EN} > V_{EN\ (ON)}$	70	100	130	kΩ
$R_{EN(OFF)}$	Pull-up resistor after shutdown	V_{EN}=0V	700	1000	1300	kΩ
Output stage VD1/VD2						
DMM	VD1/VD2			0%		
$R_{DSN(ON)}$	NMOS switch-on resistance	T=25°C, I_{DS}=0.2A		0.13		Ω
		T=100°C, I_{DS}=0.2A		0.17		
$R_{DSP(ON)}$	PMOS switch-on resistance	T=25°C, I_{DS}=0.2A		0.25		
		T=100°C, I_{DS}=0.2A		0.30		
F_{SW0}	Operating frequency	VD1/VD2 connects 51Ω resistors to GND respective	306	340	374	kHz
V_{SLEW}	Slew rate	VD1/VD2 connects 51Ω resistors to GND respective		72		V/us
t_{BBM}	VD1/VD2 break-before-make time	VD1/VD2 connects 51Ω resistors to GND respective		65		ns
I_{LIM0}	Current clamp limit initial value	Short circuit VD1 and VD2, test current of VIN	350	500	650	mA
I_{LIM1}	Current clamp limit steady-state values		650	900	1150	mA
t_{ss}	Rise time when I_{LIM0} rises to I_{LIM1}			1		ms
Over Temperature Protection						
T_{SHDN}	Thermal shutdown		145	163	175	°C
$T_{SHDN\ (HYS)}$	Thermal shutdown hysteresis			17		°C
$T_{OFFMIN(OTP)}$	Delayed recovery time			2^{18}		Tsw

Typical Characteristics

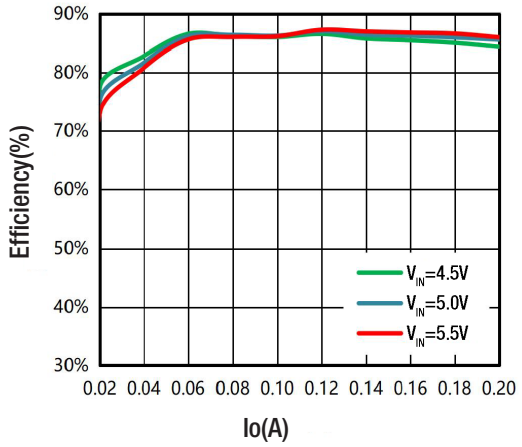


Fig. 1 Efficiency vs Output Current (5V to 5V/1W)

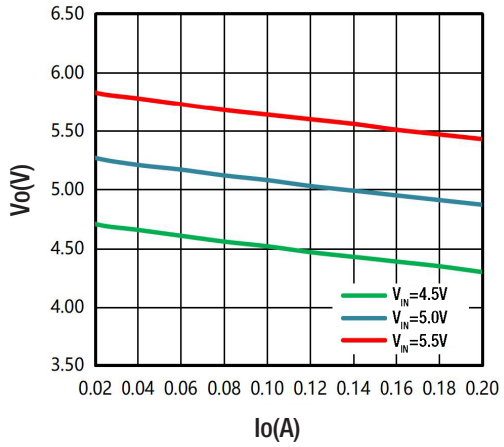


Fig. 2 Output Voltage vs Output Current (5V to 5V/1W)

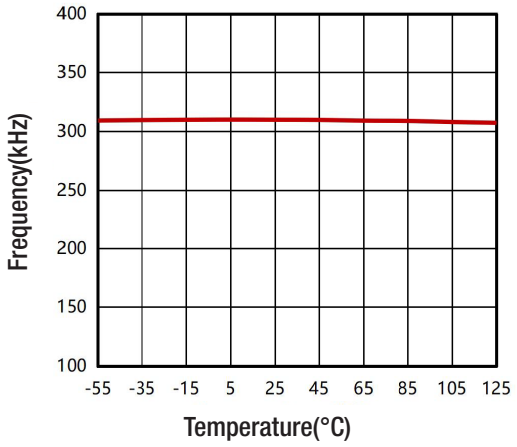


Fig. 3 Frequency vs Temperature

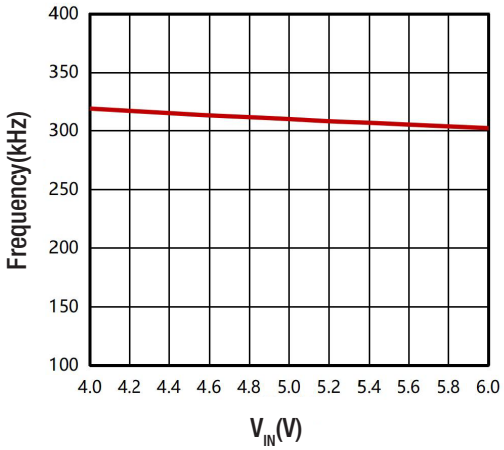


Fig. 4 Frequency vs Input Voltage

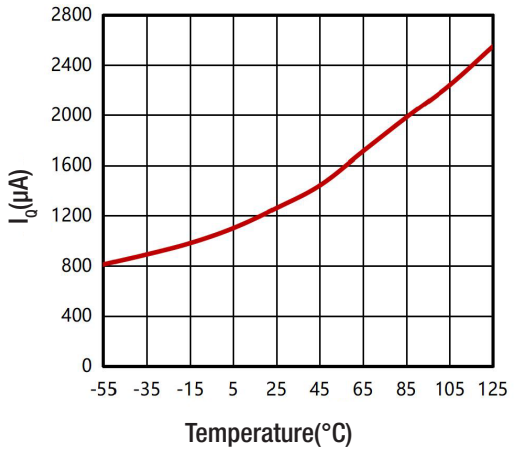


Fig. 5 I_Q vs Temperature

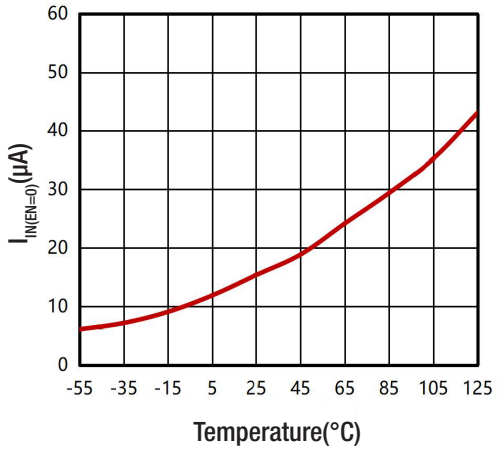


Fig. 6 $I_{in(EN=0)}$ vs Temperature

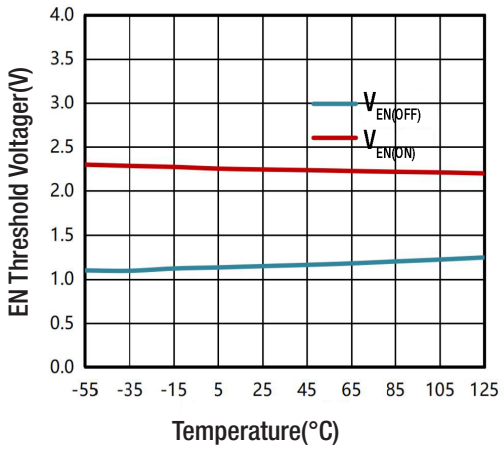


Fig. 7 EN Threshold Voltage vs Temperature

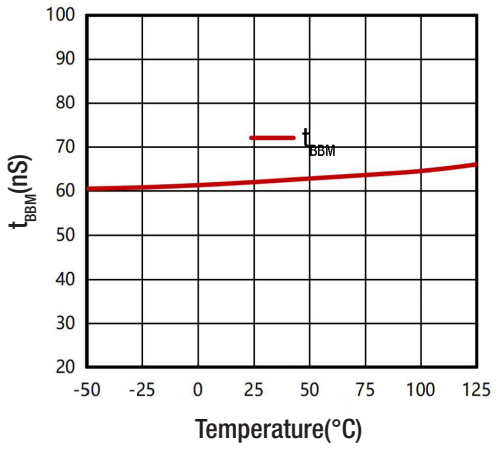


Fig. 8 t_{BBM} vs Temperature

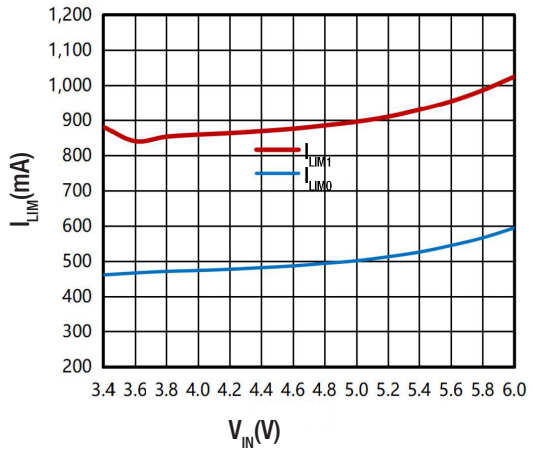


Fig. 9 I_{LIM} vs Input Voltage

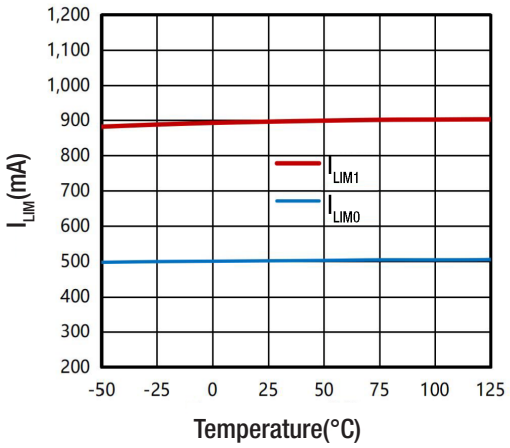


Fig. 10 I_{LIM} vs Temperature

PARAMETER MEASUREMENT INFORMATION

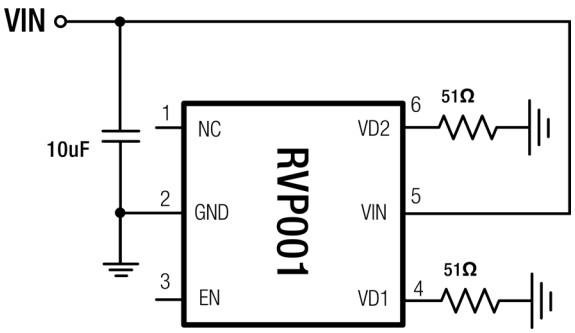


Fig. 11 f_{SW0}/ V_{SLEW}/ t_{BBM} Test Circuit

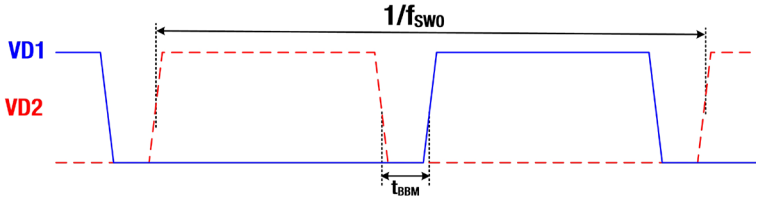


Fig. 12 VD1 and VD2 Timing Diagram

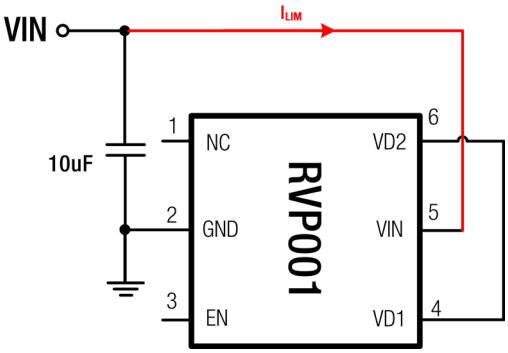


Fig. 13 I_{LIM} Test Circuit

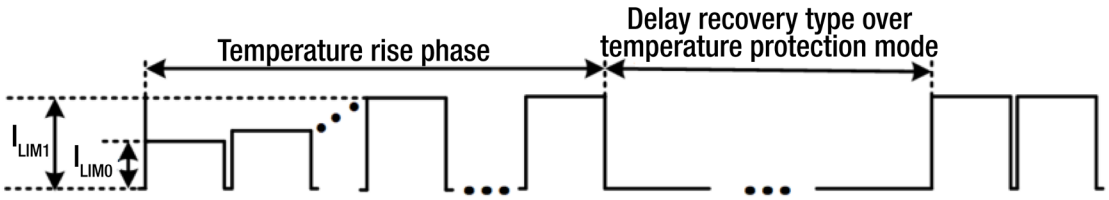


Fig. 14 I_{LIM} Test Timing Diagram

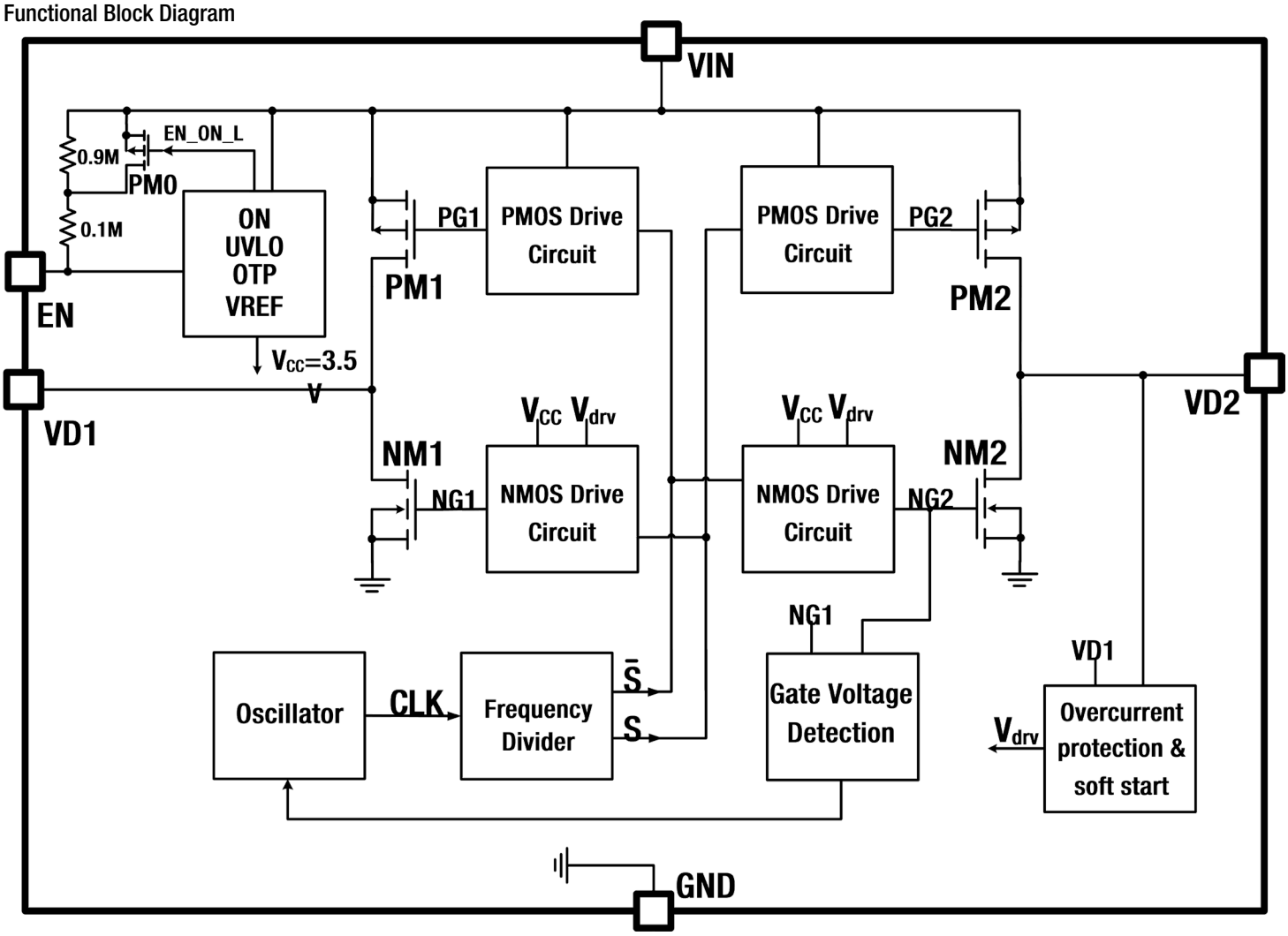
DETAILED DESCRIPTION

Overview

RVP001 is a transformer driver designed for isolated DC/DC converters using a full-bridge topology. This topology minimizes the number of transformer windings, helping to reduce overall cost. It supports applications with input voltages ranging from 3V to 6V and offers strong compatibility. The device features clamp-limiting on the power switch current, providing protection when current levels become too high. This not only keeps the chip operating within its safe zone but also shields peripheral components from large current surges. Additionally, the RVP001 incorporates a dead time t_{BBM} between the two drive signals. This design prevents simultaneous switching of the power switches, reducing the risk of short circuits. It also lowers the drain-source voltage during turn-on, minimizing switching losses.

The chip is controlled via the EN pin, which enables or disables its operation. When the EN pin is pulled high-or left unconnected, as it defaults to a high level-the chip functions normally. When the EN pin is pulled low, the chip stops operating and enters an ultra-low power standby mode.

Functional Block Diagram



Operation Mode

Full Bridge Waveform

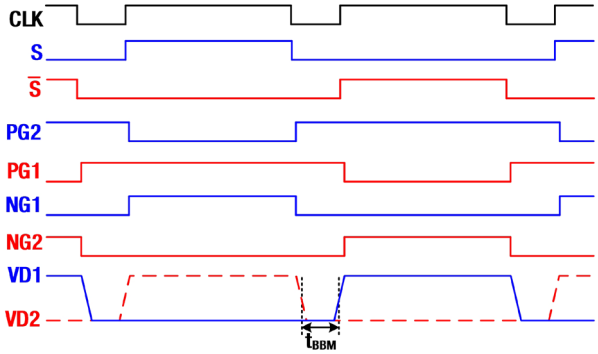


Fig. 15 Output Signal Waveforms

In Figure 15, NG1 and NG2 represent the gate logic levels of the power switches NM1 and NM2, respectively. These signals share the same high-level pulse widths, but there is a brief interval between the high states during which both signals are low. This interval is referred to as the dead time t_{BBM}, which prevents both power switches from being on simultaneously during transitions. This not only avoids short-circuit conditions but also ensures that the switches turn on at a lower drain-source voltage, thereby reducing switching losses. The dead time t_{BBM} is primarily determined by the low-level duration of the oscillator clock (CLK) and is inversely related to the chip's operating frequency: the lower the frequency, the longer the dead time, and vice versa. After NM1 and NM2 are turned off, their gate voltages are monitored, and t_{BBM} is generated only once the switches have fully turned off. This method minimizes the impact of driver delay and its temperature dependence, ensuring consistent dead time performance across the full input voltage range.

Current Clamp Mode

During the startup of the converter, if the output is short-circuited or the transformer becomes magnetically saturated, the current flowing through the power switches NM1 and NM2 may become excessively high. The RVP001 detects this condition and responds by reducing the gate drive voltage to the power switches, thereby limiting the current to a safe level defined by the internal clamp threshold, I_{LIM}. This mechanism not only ensures safe operation of the switches within their specified current range but also protects external components, such as the transformer and output rectifier diode from the harmful effects of high surge currents. As a result, the current clamp mode significantly enhances the overall reliability and fault tolerance of the converter.

Delay recovery overtemperature protection mode

When the internal temperature of the chip exceeds the specified threshold, it enters a protection state in which all power switches remain disabled. To return to normal operation, two conditions must be met: (1) the temperature must fall below the recovery threshold, and (2) the mandatory cooldown period must elapse. In this protection mode, the chip's internal temperature more closely aligns with the ambient temperature when restarting after an over-temperature event. As the temperature rises again to the over-temperature trigger point, the chip benefits from a wider thermal margin. This allows for a longer maximum drive time of the power switches, providing greater capacitive load capability and preventing abnormal startup behavior in systems with large output capacitance following thermal shutdown.

Principle of Output Short Circuit Protection

The output short-circuit protection of the full-bridge converter is achieved through the combined operation of the current clamp mode and the delayed-recovery over-temperature protection mode. In the event of an output short circuit, the primary winding N_P of the transformer is clamped with a minimal voltage drop, while most of the input voltage VIN drops across the N-channel MOSFETs. When a high current is detected, the chip enters current clamp mode. As the power switches heat up, the chip temperature gradually increases, eventually triggering the over-temperature protection mode with delayed recovery. The rate at which the temperature rises depends on the ambient temperature and input voltage. Lower ambient temperatures or lower input voltages result in a slower temperature increase, thereby delaying the activation of over-temperature protection. This adaptive behavior enhances the converter's ability to handle large capacitive loads. Furthermore, the delayed recovery mode ensures stable operation even under high-temperature conditions, optimizing performance with capacitive loads.

General Operating Mode

During startup, the output capacitor initially holds a low voltage, resulting in a relatively high inrush current through the power switches. Under these conditions, the converter begins operation in current clamp mode to protect the power stage. As the output voltage rises and approaches its rated value, the current through the power switches decreases. In response, the RVP001 gradually increases the gate drive voltage, fully enhancing the switches and thereby minimizing their on-resistance ($R_{DS(ON)}$). This transition ensures efficient operation under normal load conditions, with reduced conduction losses and improved overall system performance.

EN Shutdown Mode

To achieve ultra-low standby power consumption, the RVP001 includes an enable control pin (EN). The device shuts down when the EN voltage falls below 1.14V and resumes normal operation when the voltage rises above 2.24V. Internally, the EN pin is connected to two series pull-up resistors: a 0.9MΩ resistor and a 0.1MΩ resistor. During normal operation (when EN is high), the 0.9MΩ resistor is bypassed by a P-channel MOSFET (PM0), leaving only the 0.1MΩ resistor active. This configuration results in a low pull-up resistance, providing strong noise immunity. When the EN voltage is pulled low to disable the device, PM0 is turned off, and the full 1MΩ resistance (0.9MΩ+0.1MΩ) is restored. This high pull-up resistance significantly reduces shutdown current, contributing to the device's ultra-low power standby performance.

Full Bridge Converter

Operating Principle of Full Bridge Converter

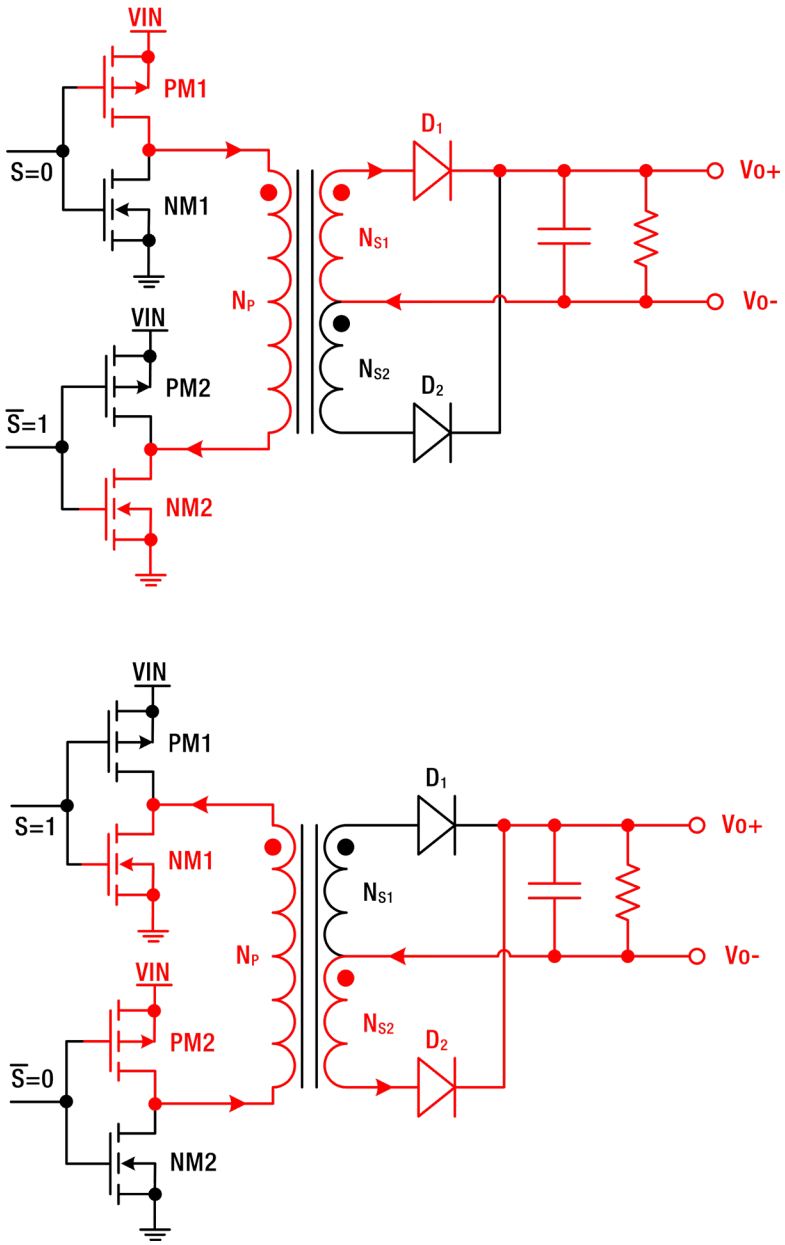


Fig. 16 Full Bridge Transformer Schematic

When S=0, the P-channel MOSFET PM1 and the N-channel MOSFET NM2 are turned on, while PM2 and NM1 are turned off, enabling isolated power transmission in the first direction. On the primary side of the transformer, current flows from the positive terminal VIN of the input power supply, passes through PM1, enters the dotted terminal of the primary winding N_P, exits through the undotted terminal, and flows to ground GND via NM2. On the secondary side, current flows into the undotted terminal of winding N_{S1}, exits from the dotted terminal, and passes through the forward-conducting rectifier diode D_1 to reach the converter's output. During this phase, no current flows through winding N_{S2}, and diode D_2 remains off.

When S=1, the P-channel MOSFET PM2 and N-channel MOSFET NM1 are turned on, while PM1 and NM2 are turned off, enabling isolated transmission in the second direction. Current on the primary side flows from VIN through PM2, enters the undotted terminal of winding N_P, exits from the dotted terminal, and returns to GND through NM1. On the secondary side, current flows into the dotted terminal of winding N_{S2}, exits from the undotted terminal, and passes through rectifier diode D_2 to the output. In this state, winding N_{S1} carries no current, and diode D_1 is off.

The full-bridge converter operates at an effective duty cycle close to 100%, allowing continuous energy transfer to the secondary side. This high-duty operation contributes to both high conversion efficiency and excellent dynamic response. As a result, only a small output capacitor is needed to maintain a low output voltage ripple under normal operation. However, to prevent shoot-through during switching and to minimize switching losses, a defined dead time is introduced between transitions of the two switching pairs on the primary side. During this dead time, power transfer temporarily halts, and the output is solely maintained by the energy stored in the output capacitor. Consequently, a slight increase in output voltage ripple may occur during these brief intervals.

Core Magnetization

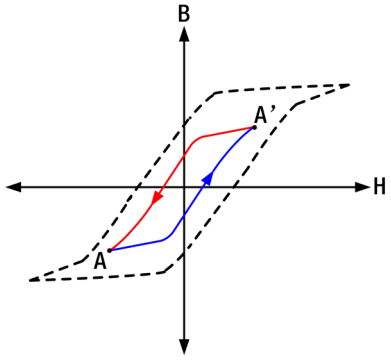


Fig. 17 Full Bridge Transformer Core Magnetization

For a full bridge transformer to operate normally, it must satisfy the condition known as volt-second balance. This principle states that the volt-second product the product of the primary winding voltage (V_P) and the duration of conduction time (T_{ON}) during the magnetization excitation phase must be equal in magnitude and opposite in polarity to that of the demagnetization phase. If this balance is not maintained, core saturation may occur over time.
Figure 17 illustrates the magnetization curve of a transformer core, where B denotes magnetic flux density and H represents magnetic field strength within the core.
When switches PM1 and NM2 are turned on, the transformer enters the excitation phase, and magnetic flux density increases as the flux moves from point A to A'. This causes the core to store magnetic energy, and when these switches are turned off, the flux reaches its maximum positive value at point A'.
Subsequently, when switches PM2 and NM1 are turned on, the transformer enters the demagnetization phase, during which the magnetic flux density decreases as the flux returns from A' to A. When these switches are turned off, the core reaches its maximum negative magnetic flux density at point A.
The magnitude of the magnetic flux density B in each cycle is primarily governed by the volt-second product, expressed as $V_P \times T_{ON}$. For balanced operation, the volt-second product in the excitation phase must match that of the demagnetization phase. If an imbalance occurs, it introduces a magnetic bias-a gradual shift in the core's operating point along the B-H curve. Over time, this bias accumulates and pushes the core toward magnetic saturation, exceeding its designed flux density limit. Once saturation is reached, the core can no longer support proper energy transfer, resulting in loss of transformer function and potential failure of the converter.

TYPICAL APPLICATION

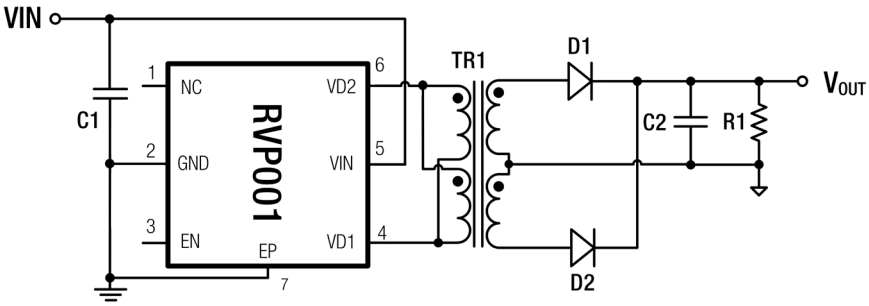


Fig. 18 Typical Application Schematic

Design Requirements

The following are typical application examples using a 5V ±10% input, an isolated unregulated 5V output, and up to 1W output power. Key power supply specifications are provided below:

Input and Output Parameters

Specification	MIN	TYP	MAX	UNIT
Input Voltage	4.5	5.0	5.5	V
Output Voltage	---	5.0	---	V
Output Current	---	0.2	---	A
Output Ripple and Noise	---	50	100	mV
Voltage Regulation	---	---	1.5	%
Load Regulation	---	---	10	%
Conversion Efficiency	---	85	---	%
Reliability Requirements				
Output Short Circuit Protection	Continuous, self-recovery			
Operating Temperature	-40	---	85	°C
Isolation	1500	---	---	VDC

Input Capacitor Selection

As shown in Figure 18, the input capacitor C1 serves multiple purposes, including energy storage, input filtering, and decoupling. Enhancing high-frequency noise suppression, an additional 0.1µF ceramic capacitor may be connected in parallel between VIN and GND. This decoupling capacitor should be placed as close to the chip as possible.

During operation, C1 supplies transient current to the converter. A capacitance value in the range of 1µF to 10µF is recommended to minimize input voltage ripple. The capacitor's voltage rating must exceed the maximum input voltage, with appropriate derating applied.

For optimal performance, use ceramic chip capacitors with low ESR and stable temperature characteristics. To further reduce voltage spikes caused by parasitic PCB inductance, place C1 close to the VIN and GND pins, and ensure that power loop traces are short and wide.

Output Rectifier Diode Selection

For optimal performance, it is recommended to use Schottky diodes in the output rectification circuit due to their low forward voltage drop and short reverse recovery time, which contribute to improved load regulation and higher conversion efficiency. This design adopts a full-wave rectification topology, where the reverse voltage stress on each diode is approximately twice the output voltage. Therefore, the selected diode must have a reverse voltage rating of at least 2x the maximum output voltage, with appropriate derating applied for reliability.

The selected rectifier diode must also be capable of operating reliably across the expected ambient temperature range. Special attention should be given to reverse leakage current, which increases significantly at high temperatures. Derating based on the diode's temperature-leakage characteristics (as illustrated in the diode's temperature derating curve) is necessary to maintain performance and reliability.

To ensure the full-bridge converter operates reliably under all conditions, the diode selection must also account for abnormal operating scenarios, such as output short circuits. In such cases, the RVP001 enters output short-circuit protection mode, during which it switches to current clamp mode. The internal clamp limits the current through the power switches to I_{LIM} (typically 900mA, up to 1150mA maximum). As a result, the maximum current through the output rectifier diode must be calculated based on the transformer turns ratio and this clamped primary current.

The peak current requirement for the rectifier diode can be estimated using the following formula:

$$I_{D-MAX} = \frac{N_P}{N_S} \times I_{\mathrm{LIM-MAX}}$$

In the equation, N_P refers to the number of turns of the primary winding of the full-bridge transformer, N_S is the number of turns of the secondary winding, and $I_{LIM-MAX}$ represents the maximum current clamp limit of the chip.

During protection mode, the converter operates in over-temperature protection (OTP) with delayed recovery. When the chip enters self-recovery and subsequently re-triggers OTP, it shuts down again to prevent thermal damage. During this interval, the output rectifier diode conducts continuously at its maximum operating current. Therefore, when selecting the rectifier diode, it is highly important to ensure that its peak forward surge current (I_{FSM}) rating is sufficient to handle this stress reliably.

The RB160M-30 Schottky diode is suitable for this application. At 75°C, it exhibits a forward voltage drop of approximately 280mV at 0.2A, and a reverse leakage current of around 90µA at 15V. Its peak forward surge current rating is I_{FSM} = 30A. For applications requiring higher operating temperatures, it is advisable to select a Schottky diode with lower reverse leakage current under elevated thermal conditions to maintain efficiency and reliability.

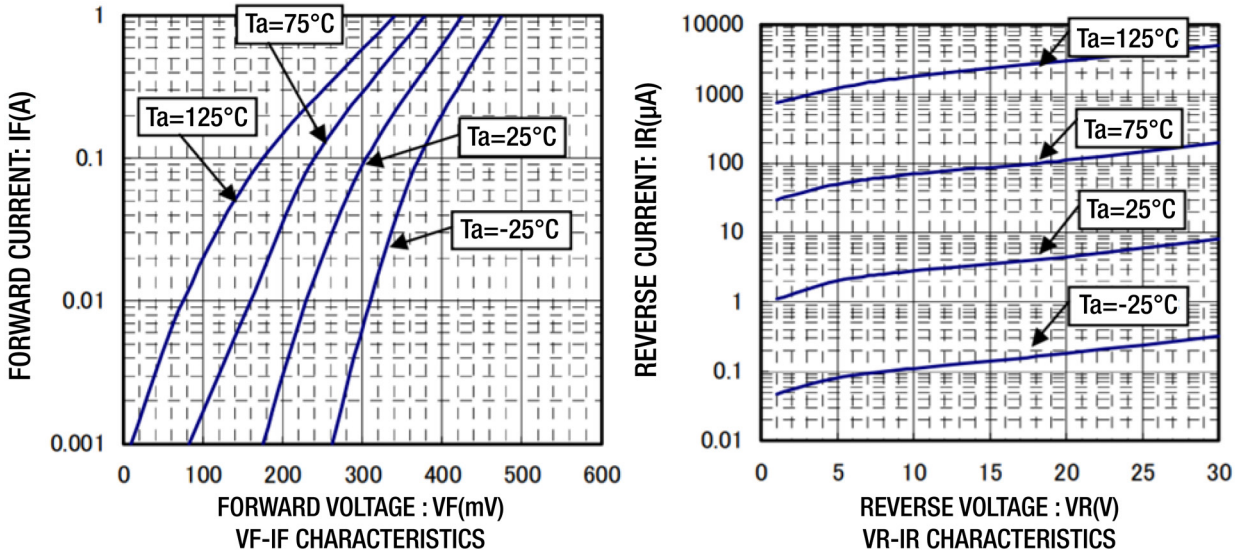


Fig. 19 Schottky Diode RB160M-30 Characteristics

Output Capacitor Selection

While a full bridge converter can theoretically deliver power to the secondary side with nearly a 100% duty cycle, in practice, a short dead time is required between switching transitions to prevent cross conduction. During this dead time, the output filter capacitor C2 temporarily supplies energy to the load, resulting in some level of output voltage ripple.
To ensure stable operation and effective filtering, it is recommended to use a ceramic capacitor with a capacitance value between 4.7µF and 10µF for C2. The capacitor should have low ESR and good temperature stability to minimize ripple and maintain performance across varying load and environmental conditions.

Full Bridge Transformer Selection

Primary to Secondary turns ratio estimation once the output rectifier diode has been selected, its forward voltage drop (V_F) at maximum output current can be determined. This value, along with the target output voltage, helps define the required minimum secondary voltage. The turns ratio of the full bridge transformer primary winding (N_P) to secondary winding (N_S) can then be estimated based on the input voltage on the primary side and the minimum required output voltage on the secondary side. Using this information, the transformer can be designed to ensure that the required output voltage is delivered while maintaining efficient power transfer, proper volt-second balance, and sufficient headroom for rectification losses and regulation margin.
Under nominal input and full-load conditions, the input voltage across the transformer's primary winding is:

$$V_p = V_{IN} - \frac{P_{O-MAX}}{\eta \times V_{IN}} (R_{DSP(ON)} + R_{DSN(ON)})$$

P_{O-MAX} is the maximum output power of the full bridge converter, η is the nominal input, estimated conversion efficiency of a full bridge converter at full load, and $R_{DSP(ON)}$ and $R_{DSN(ON)}$ are ON-resistance of the PMOS and NMOS respectively.
At full output load, the minimum output voltage of the secondary winding is:

$$V_S = V_{O-MIN} + V_F$$

V_{O-MIN} is the minimum output voltage allowed by the full-bridge converter under full-load conditions. To ensure the output remains within specification, V_{O-MIN} is typically calculated as 97% of the nominal output voltage, reflecting a -3% regulation margin. V_F represents the forward voltage drop of the selected output rectifier diode at full load.
According to the above equation, the primary to secondary turns ratio can be determined through:

$$N_{PS} = \frac{V_{IN} - \frac{P_{O-MAX}}{\eta \times V_{IN}} \times (R_{DSP(ON)} + R_{DSN(ON)})}{V_{O-MIN} + V_F}$$

Based on the input and output requirements of this application, the primary and secondary turns ratio is approximated as:

$$N_{PS} = \frac{5V - \frac{1W}{0.85 \times 5V} \times (0.25\Omega + 0.13\Omega)}{5V \times 0.97 + 0.34V} \approx 0.876$$

Volt-second Product Calculation

To avoid transformer core saturation, the transformer's volt-second capacity must exceed the maximum volt-second product generated by the RVP001 under all normal operating conditions. In applications with a narrow input range, the input voltage is typically specified as ±10% of the nominal value, and the volt-second calculation should be based on the maximum input voltage.
Additionally, the switching frequency and its tolerance must be considered to ensure the transformer does not saturate when the chip operates at its minimum switching frequency. The worst case scenario for transformer excitation occurs when the highest input voltage coincides with the lowest switching frequency, corresponding to half of the switching cycle time.
Therefore, the minimum required volt-second product applied to the primary winding can be calculated as:

$$Vt_{MIN} \geq V_{IN-MAX} \times \frac{T_{MAX}}{2} = \frac{V_{IN-MAX}}{2 \times f_{MIN}}$$

Based on the design requirements of this application, the operating frequency of RVP001 is typically 340kHz and the minimum operating frequency is 306kHz. When the input voltage is at the highest, the volt-second product should be:

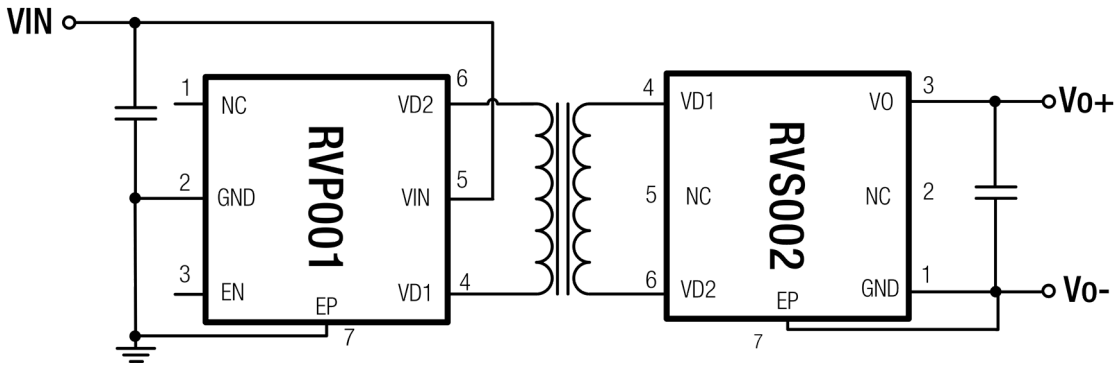
$$Vt_{MIN} \geq \frac{5V \times 110\%}{2 \times 306kHz} \approx 9V\mu s$$

The selection of the full bridge transformer should be based on the specific application requirements, including the required volt-second product and the primary-to-secondary turns ratio. In addition, factors such as maximum output power, isolation voltage rating, and distributed isolation capacitance must also be carefully considered to ensure reliable performance and compliance with system-level requirements.

RVP001 Transformer Driver for Micro-power Isolated Supplies

3-6VIN/0.5A Power Switch

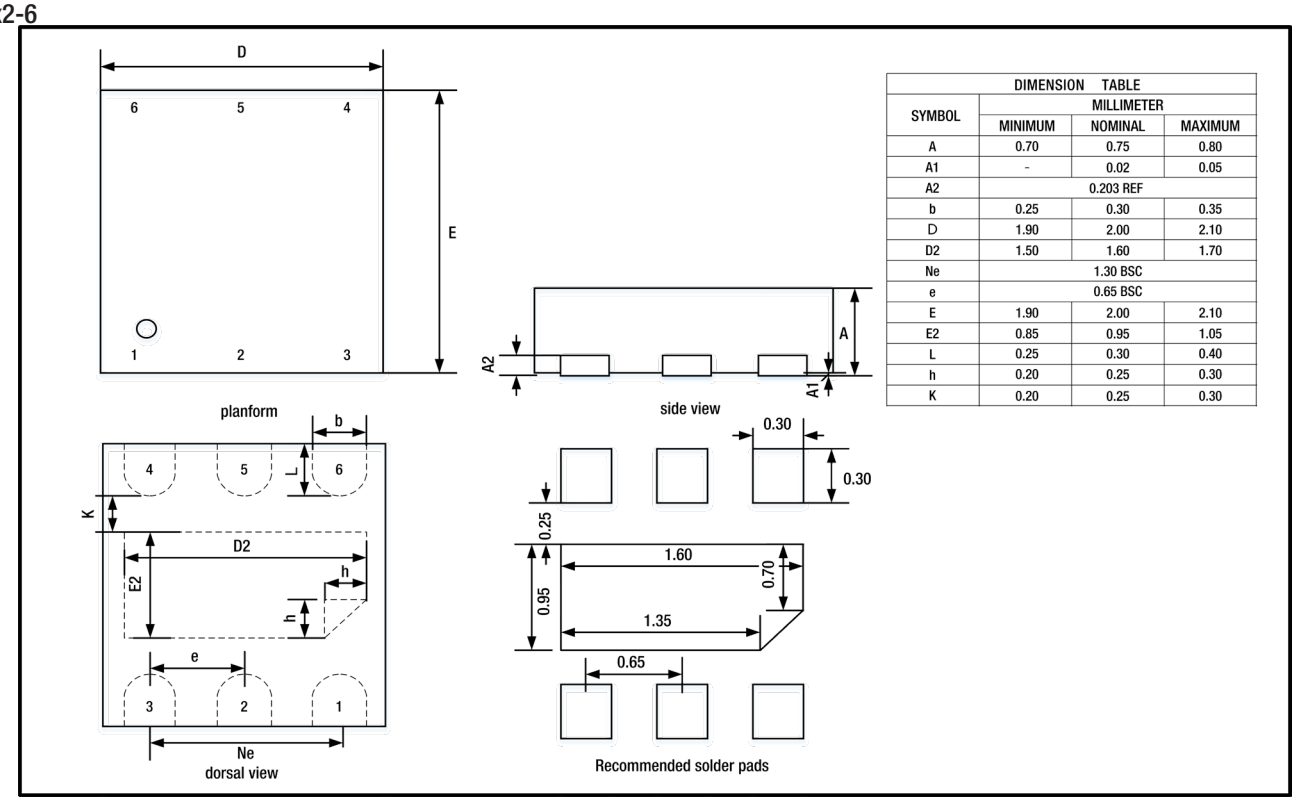
TYPICAL APPLICATION



V_{IN}(V)	V_{OUT}(V)	Power(W)	TR	Isolated Voltage
5	5	1	TMR-001-P55	3000VDC

PACKAGING INFORMATION

DFN2x2-6



DIMENSION TABLE			
SYMBOL	MILLIMETER		
	MINIMUM	NOMINAL	MAXIMUM
A	0.70	0.75	0.80
A1	-	0.02	0.05
A2		0.203 REF	
b	0.25	0.30	0.35
D	1.90	2.00	2.10
D2	1.50	1.60	1.70
Ne		1.30 BSC	
e		0.65 BSC	
E	1.90	2.00	2.10
E2	0.85	0.95	1.05
L	0.25	0.30	0.40
h	0.20	0.25	0.30
K	0.20	0.25	0.30

ORDER INFORMATION

Device	Package Type	PIN	Packaging	QTY	Marking Code*	MSL
RVP001-FBN-2DN6-R	DFN2x2-6	6	Tape and Reel	3000	RVP001 XXXX	MSL-3

*Marking Code :
RVP ——Company Code
001——Product Code
Model XXXX—— Product Traceability ID Number