AIROC™ Wi-Fi & Bluetooth® LE Connected MCU

Low-power, 1 x 1, tri-band, IEEE 802.11ax, Wi-Fi 6/6E, Bluetooth® Low Energy 5.4

Description

The Infineon CYW55913/55912/55911/55903/55902/55901 are a family of ultra-lower power, single-chip, connected MCUs that support 1x1 Wi-Fi 6/6E, Bluetooth® Low Energy 5.4, Matter, IP networking, targeted at Internet-of-Things (IoT) applications for stand-alone operation or to offload a host-processor. An integrated 192 MHz Arm® Cortex®-CM33, runs the Wi-Fi and Networking Stacks, Bluetooth® LE 5.4 and supports a wide array of peripherals.

The CYW5591x Wi-Fi supports single stream, 1x1, Wi-Fi 6/6E (802.11ax), with PHY rates up to 1024 QAM (MCS11) over 20-MHz channels. Included on-chip are 2.4 GHz and 5/6 GHz transmit power amplifiers (PAs), and low-noise amplifiers (LNAs) for best-in-class RF performance. The device is also capable of operating with external power amplifiers and low-noise amplifiers, as well as switched antenna diversity, if improved range is required. The CYW55913 supports tri-band (2.4 GHz, and 5/6 GHz), the CYW55912 supports dual-band (2.4 GHz and 5 GHz) and the CYW55911 supports single-band (2.4 GHz) with all devices support Bluetooth® LE 5.4.

The device supports Bluetooth® LE 5.4 with support for LE 1 Mbps, LE 2 Mbps, LE long range (Coded Phy) with advertising coding selection. The device includes on-chip power amplifiers supporting three different output power paths optimized for best efficiency, +4 dBm, +13 dBm, and +19 dBm path for driving poor antennas in wearable devices or other applications that require longer range for Bluetooth® LE. The device also features a flexible Bluetooth® receiver offering a dedicated Bluetooth® path or a Bluetooth® receive path that can be shared (sLNA) with the 2.4-GHz WLAN receive path. The CYW55903 supports tri-band (2.4 GHz, and 5/6 GHz), the CYW55902 supports dual-band (2.4 GHz and 5 GHz) and the CYW55901 supports single-band (2.4 GHz). The CYW55903/2/1 family does not support Bluetooth® LE.

The device integrates a 192 MHz Arm® Cortex® M33 processor with ThreadX RTOS, NetX Duo TCPI/IP network stack and NetX Secure for TLS 1.3 embedded in the 2048 KB of ROM. The device also embeds 768 KB of SRAM. A Quad SPI interface is available for supporting external Flash and PSRAM, supporting XIP and On-the-Fly encryption/description. Network communication can be enabled through the interface options: SDIO, gSPI, UART and SPI. The device supports three Serial Control Blocks (SCB) with each SCB supporting I2C/SPI/UART, 9x Timing Control and PWM blocks, 12-bit ADC with seven channel mux input for DC sensing. A pair of time-division multiplexing (TDM) interfaces enables a flexible interface for various audio use cases and a PDM interface is available for connecting digital microphones. A UART/SDIO/SPI/I2C/gSPI interface is available for interfacing with the host processor. CYW55913 family does not support Bluetooth® LE Audio. See the CYW55513/2/1 for devices requiring Bluetooth® BR/EDR and Bluetooth® LE Audio support.

The CYW5591x also includes a power management unit (PMU) and requires a 37.4 MHz crystal which provides the system reference clock and can operate from an internal high-accuracy 32.768 kHz low-power oscillator (iLPO) or external 32.76 kHz crystal (eLPO) for higher accuracy or from an external reference clock. The CYW5591x includes advanced coexistence hardware mechanisms and algorithms which ensure WLAN and Bluetooth® LE simultaneous operation is optimized for maximum performance. In addition, coexistence support is available for external radios such as (LTE, GPS, and ZigBee) via an external interface. The CYW5591x operates over the -40°C to +85°C temperature range and is available in a 0.35 mm pitch WLBGA package.

Features

- Connected MCU
  - Arm® Cortex®-M33 192 MHz with Trustzone Cryptocell 312
  - On-chip memory has
    - 2048-KB ROM
      - ThreadX RTOS
      - NetX Secure TLS 1.3
      - NetX Duo (TCP/IP)
    - 768-KB RAM
  - 1 x Serial memory interface (SMIF)
    - QSPI interface supporting external FLASH and PSRAM up to 16 MB
    - Option to boot from Flash, support Execute-in-place (XIP) with on-the-fly AES encryption/ decryption
  - ModusToolbox™ supports various middleware, Peripheral Driver libraries, Hardware Abstraction Libraries
  - Supports interface with other Host MCUs for Network Offloads and Network communication over AT Commands interface
    - > 40 Mbps throughput with TCP/IP, TLS over SDIO
    - > 20 Mbps throughput with TCP/IP, TLS over gSPI
    - < 7.4 Mbps throughput with TCP/IP, TLS over UART
- Wide selection of peripherals
  - 7 Channel 12-bit Sigma Delta ADC
    - 16 ksps, 7x DC sensing, 1 x analog MIC for noise threshold detection (NTD)
  - 2 x Low Power Comparators (LPCOMP)
    - Programmable thresholds for window comparison
  - 3 x Serial Communication Blocks configurable as SPI, I2C or UART
    - UART (< 7.4 Mbps)
    - I2C (100 kHz, 400 kHz and 1 MHz)
    - SPI (run up to a max clock of 24 MHz)
  - 9 x Timer Counter PWM (TCPWM)
    - 2 x 32-bit + 7 x 16-bit counters, 4 x OUT positive/negative, 8 x IN
  - 1 x PDM (Left and Right Digital microphones)
  - Audio Interfaces
    - TDM1, TDM2 each supporting inter-IC sound (I2S) (2-channels) and PCM (8-channels), 8k to 96k sample rates, and 16- and 24-bit sample widths
    - Bidirectional PCM (TDM and I2S) with 8k, 16k sample rates and 16-bit sample width. Multiplexed with TDM2 through second audio interface
    - Single-direction I2S with 48k sample rates and 16-bit sample width. Multiplexed with TDM2 through second audio interface
  - GPIO
    - 48 pins could be used for GPIO function

  - Timer/Watchdog
    - 2x Timer
    - 1x Watchdog
  - Programming and debug
    - Debug Supported via Arm® DAP JTAG/SWD
    - Programming supported via UART
- WLAN features
  - IEEE 802.11a/b/g/n/ac/ax compliant
  - Tri-band (2.4 GHz/5 GHz/6 GHz)
  - 1x1 with 20 MHz channels supporting PHY data rates up to 802.11ax (MCS11 1024-QAM 5/6)
  - Transmit (TX) power with internal PA
    - 2.4 GHz: +24.0 dBm 1 Mbps DSSS
    - 5 GHz: +22.5 dBm 6 Mbps OFDM
    - 6 GHz:
      - +21.0 dBm MCS0 UNII-5 OFDM
      - +21.0 dBm MCS0 UNII-6 OFDM
      - +20.5 dBm MCS0 UNII-7 OFDM
      - +20.5 dBm MCS0 UNII-8 OFDM
  - Sensitivity with internal LNA
    - 2.4 GHz: -101.5 dBm 1 Mbps DSSS
    - 5 GHz: -94.5 dBm MCS0
    - 6 GHz:
      - -95.0 dBm MCS0 UNII-5
      - -95.0 dBm MCS0 UNII-6
      - -95.0 dBm MCS0 UNII-7
      - -93.5 dBm MCS0 UNII-8
  - Wi-Fi 6/6E release features
    - OFDMA up-link and down-link as STA
    - Down-link multi-user MIMO (MU-MIMO) as STA
    - Individual target-wake-time (TWT), broadcast TWT
    - BSS color
  - Support for switched antenna diversity, and external PAs and LNAs for improved range
  - Mode support:
    - STA
    - SoftAP
    - STA+Soft AP
  - Security
    - WPA2(Personal/Enterprise), WPA3 (Personal/Enterprise with 192 bit security)
- Bluetooth® Low Energy
  - Bluetooth® 5.4 (Bluetooth® Low Energy)
    - Advertising Coding Selection
    - Encrypted Advertising Data
    - LE Generic Attribute Profile (GATT) Security Levels Characteristic

Features

  - Bluetooth® Low Energy 5.0/5.1/5.2/5.3 features
  -
    - Advertisement Data Information (ADI) in Periodic Advertising
    - LE Enhanced Connection Update
    - LE Channel Classification
    - LE Isochronous Channels (non-Audio applications)
    - Enhanced Attribute Protocol
    - LE Power Control
    - GATT caching
    - Periodic Advertising Sync Transfer (PAST)
    - Control Length Extension
    - Advertising Channel Index
    - Slot Availability Mask (SAM)
    - 2M PHY for LE
    - LE Coded PHY
    - High Duty Cycle Non-Connectable Advertising
    - LE Advertising Extensions
    - LE Channel Selection Algorithm #2
  - Bluetooth® LNA can be shared with WLAN LNA for reduced antenna count (sLNA)
  - Dedicated Bluetooth® LNA (dLNA) for improved RF and coexistence performance with dedicated Bluetooth® antenna
  - +4, +13, and +19 dBm Bluetooth® PA paths optimized for best efficiency, output power adjustable in 4 dB steps
  - Receive sensitivity: -111.5 dBm (Bluetooth® LE 125 kbps, LR S=8)
  - Receive sensitivity: -97.5 dBm (Bluetooth® LE 2 Mbps)
  - Bluetooth® UART with max baud rate as 4 Mbps
- General features
  - VBAT: 3.3 V typical, 3.0 V to 4.8 V operating range
  - VDDIO: 1.8 V typical
  - 0.35 mm pitch WLBGA package
  - Temperature range: -40°C to +85°C
  - Internal 32.768 kHz low-power oscillator[1], [2]
  - External 32.768 kHz low-power oscillator (eLPO) with crystal or reference clock input for low-power consumption[3]
- Security
  - Arm® Trustzone Cryptocell 312
  - Life cycle management
  - Crypto key establishment and management
  - Crypto offloads
  - PSA Level 2 certifiable
  - Secure boot
  - Wi-Fi, Bluetooth® and application independent firmware authentication
  - Firmware encryption

1 Internal low-power oscillator accuracy is only adequate for WLAN, and not for Bluetooth® if low power for Bluetooth® Low-Energy required.
2 Improved HW/SW calibration schemes allows to achieve ILPO effective variation of less than 1% across PVT.
3 External LPO is needed for Bluetooth® Low Energy to support low power mode.

Features

  - Attestation
  - Anti-rollback
- Coexistence
  - Advanced coexistence 2-wire BTSIG WCI-2 (LTE) and 3-wire (ZigBee)

Potential applications

- IP Cameras
- Video Doorbell Cameras
- Smart Locks
- Smart Watches
- IoT Gateways
- Sensors
- Wi-Fi Speakers
- Thermostats
- Appliances
- Printers
- Internet of Things (IoT)
- Industrial Internet of Things (IIoT)
- Smart Home
- Boilers
- Garage Door Openers (GDO)

Family block diagram

The block diagrams illustrates the super set of CYW5591x device, which encompasses all the features. For a detailed breakdown of specific features associated with individual parts, see Ordering information.

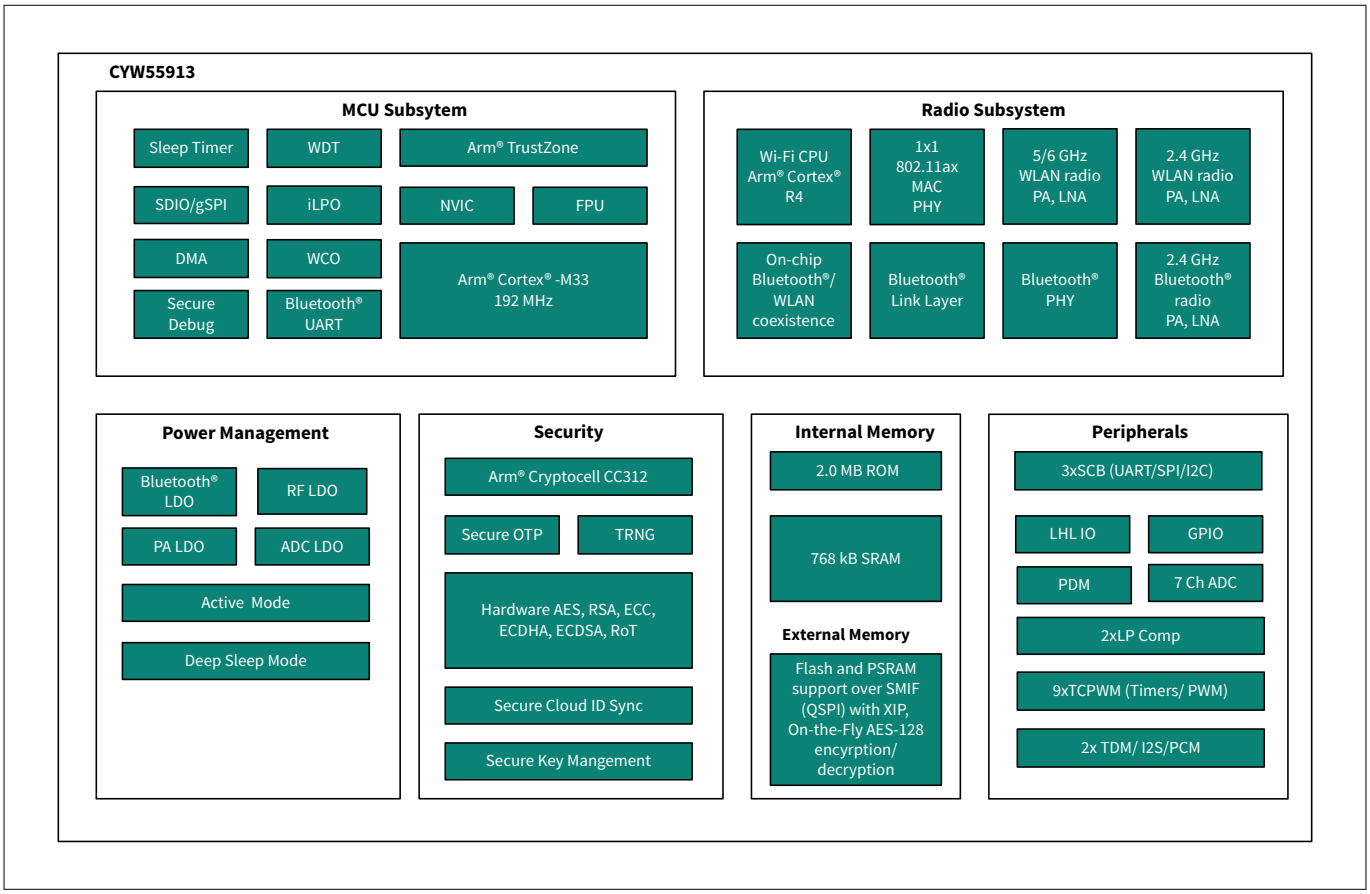

Figure 1 CYW5591x family block diagram

Functional block diagram

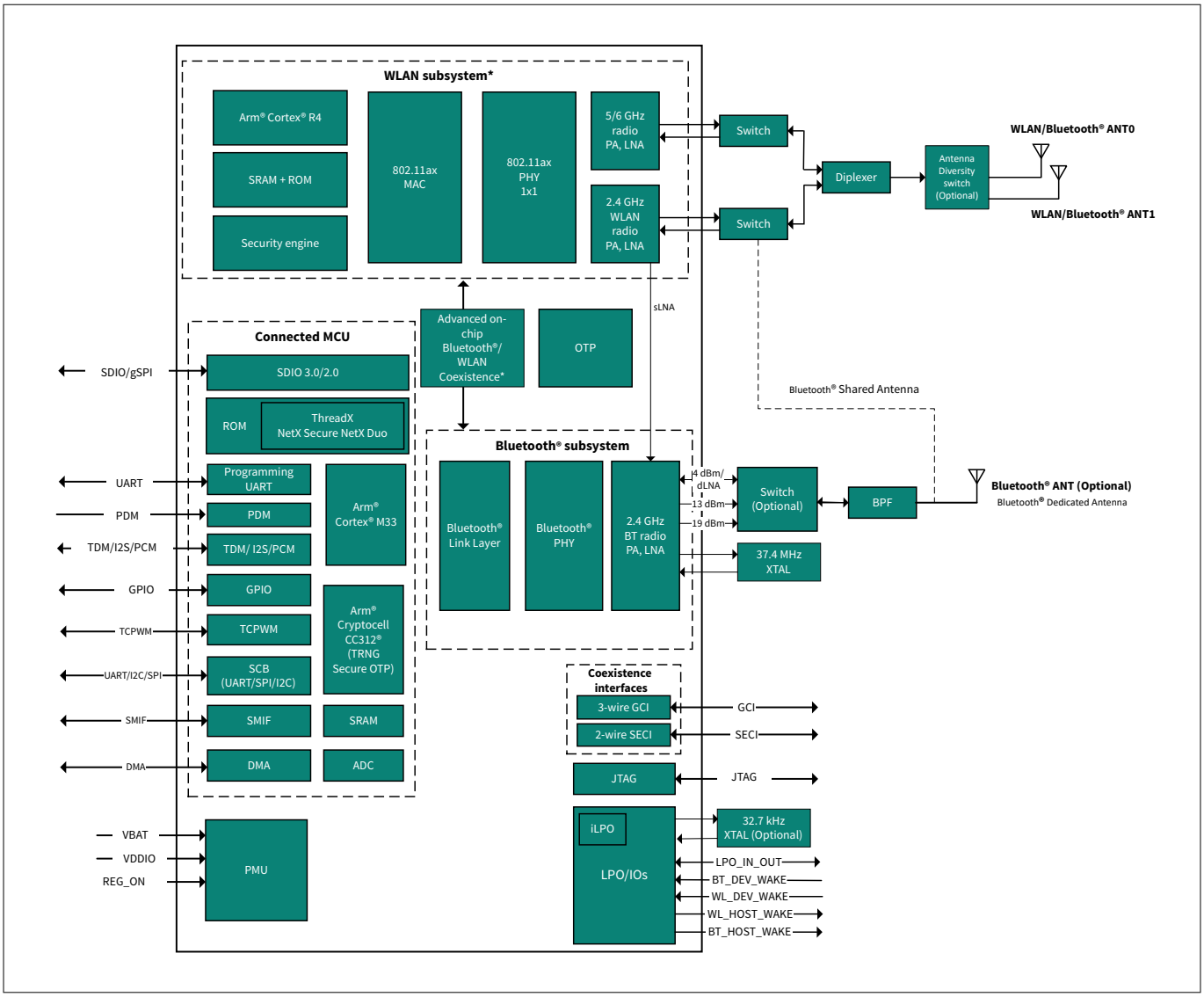

Figure 2 CYW5591x functional block diagram

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1 Overview

The CYW5591x architecture block diagram in Figure 2 shows a simplified view of the interconnection between subsystems and blocks. CYW5591x has two major connectivity subsystems: the Connected MCU + or, the Bluetooth® LE subsystem, and the Wi-Fi subsystem. The other major subsystems are I/O subsystem, peripherals, and I/O.

The user application runs in the Connected MCU and provides an extensive support for programming, testing, debugging, and tracing of the firmware.

CYW5591x provides a high-level of security with various security modes. Programming, debug, and test interfaces are disabled when maximum security is enabled.

1.1 Standards compliance

The AIROC™ CYW5591x family supports the following standards:

- Bluetooth® 4.2, 5.0, 5.1, 5.2, 5.3, 5.4
- IEEE 802.11ax
- IEEE 802.11ac mandatory and optional requirements for 20 MHz
- IEEE 802.11a/b/g/n
- IEEE 802.11d/h
- IEEE 802.11i
- IEEE 802.11k
- IEEE 802.11v
- Security
  - Open, WPA2-AES, WPA3-WPA2, WPA3-SAE, and OWE
  - WPA2/WPA3 Enterprise with 192-bit Encryption, hardware accelerator (AES), EAP-TLS, EAP-TTLS, ECDSA and RSA with TLS 1.2, TLS 1.3, and PEAPV0 with MSChapV2
- Software support (CKIP)
- IEEE 802.11r (Fast Roaming Between APs)
- IEEE 802.11w (Secure Management Frames)
- IEEE 802.11 Extensions
  - IEEE 802.11e Quality of Service (QoS) Enhancements (in accordance with the WMM specification, QoS is already supported)
  - IEEE 802.11h 5/6 GHz Extensions
  - IEEE 802.11i MAC Enhancements

2 Power supplies and power management

2.1 Power supply topology

A buck regulator, multiple LDO regulators, and a power management unit are integrated into CYW5591x. These blocks simplify power supply design for Bluetooth® and WLAN functions in embedded designs. CYW5591x only requires two power supplies, VBAT, and VDDIO, to be provided, with all additional voltages being generated by on-chip regulators.

Control signal REG_ON is used to power-up the regulators and take the device out of reset. The core Buck regulator ABUCK powers up when REG_ON is asserted. All regulators, Buck and LDO, are powered down when REG_ON is deasserted.

CYW5591x allows for an extremely low power-consumption mode by completely shutting down the ABUCK regulator.

2.2 CYW5591x family PMU features

CYW5591x contains the following regulators:

- Analog switching regulator (400 mA)
- BTLDO (400 mA)
- PALDO (400 mA)
- RFLDO (100 mA)
- CLDO (100 mA)

See Internal regulator electrical specifications for more details.

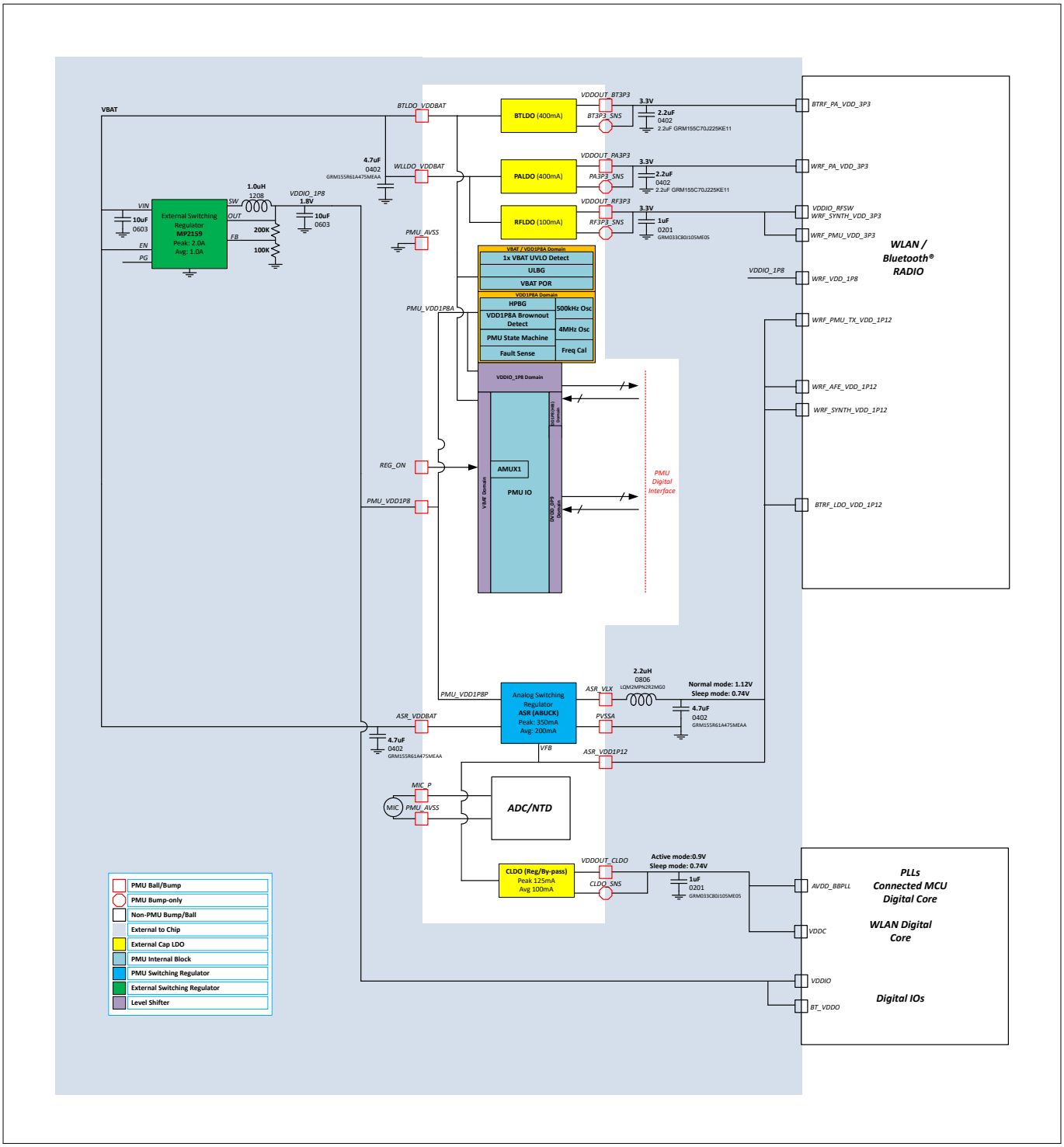


Figure 3 Typical power topology

2.3 WLAN power management

CYW5591x has been designed with the stringent performance requirements of commercial/consumer applications in mind. All areas of the chip design are optimized to minimize power consumption. Silicon processes and cell libraries were chosen to reduce leakage current and supply voltages. Additionally, the CYW5591x integrated RAM is a HIGH Vt memory with dynamic clock control. The dominant supply current consumed by the RAM is leakage current only. CYW5591x includes an advanced WLAN PMU sequencer. The PMU sequencer provides significant power savings by putting CYW5591x into various power management states

appropriate to the current environment and activities that are being performed. The PMU enables and disables internal regulators, switches, and other blocks.

CYW5591x WLAN power states are described as follows:

- **Active mode**: All WLAN blocks in CYW5591x are powered up and fully functional with active carrier sensing and frame transmission and reception. All required regulators are enabled and put in the most efficient mode based on the load current. Clock speeds are dynamically adjusted by the PMU sequencer.
- **Deep Sleep mode**: Most of the chip including both analog and digital domains and most of the regulators are powered off. All main clocks (PLL, crystal oscillator, or TCXO) are shut down to reduce active power to the minimum. In Deep Sleep mode, the primary source of power consumption is leakage current due to retention memory and flops.
- **Power-down mode**: CYW5591x is effectively powered OFF by shutting down all internal regulators. The chip is brought out of this mode by external logic re-enabling the internal regulators.

2.4 PMU sequencing

The PMU sequencer is responsible for minimizing system power consumption. It enables and disables various system resources based on a computation of the required resources and a table that describes the relationship between resources and the time needed to enable and disable them.

Configurable, free-running counters (running at 32.768 kHz LPO clock) in the PMU sequencer are used to turn ON/turn OFF individual regulators and power switches. Clock speeds are dynamically changed (or gated altogether) for the current mode. Slower clock speeds are used wherever possible.

2.5 Power-down mode

CYW5591x provides a low-power shutdown feature that allows the device to be turned OFF while the host, and any other devices in the system, remain operational. When CYW5591x is not needed in the system, VDDIO_RFSW and VDDC are shutdown while VBAT, VDDIO remains powered. This allows CYW5591x to be effectively OFF while keeping the I/O pins powered so that they do not draw extra current from any other devices connected to the I/O.

During a low-power shut-down state, provided VDDIO remains applied to CYW5591x, all outputs are tristated, and most input signals are disabled. The input voltages remain within the limits defined for normal operation. This is done to prevent current paths or create loading on any digital signals in the system and enables CYW5591x to be fully integrated in an embedded device and take full advantage of the lowest power-savings modes.

When CYW5591x is powered ON from this state, it is the same as a normal power-up and the device does not retain any information about its state from before it was powered down.

2.6 Power-up/power-down/reset circuits

CYW5591x has two signals (see Table 1) that enable or disable Bluetooth® and WLAN circuits and internal regulator blocks, allowing the host to control power consumption. For timing diagrams of these signals and the required power-up sequences, see MCU or Bluetooth® start up timing diagram.

Table 1 Power-up/power-down/reset control signals

Signal	Description
REG_ON	This signal is used by the PMU to power up the device and to control the internal CYW5591x regulators. When this pin is HIGH, the regulators are enabled, and the core is out of reset. If REG_ON is LOW, all the regulators are disabled. This pin has an internal 50 kΩ pull-down resistor that is enabled by default and can be disabled up on recognizing high on this pin.

2.7 Brownout (BOR) and UVLO

Post-POR release, the BOR and UVLO circuits monitor the voltages on the 1.8 V and VBAT supplies respectively.

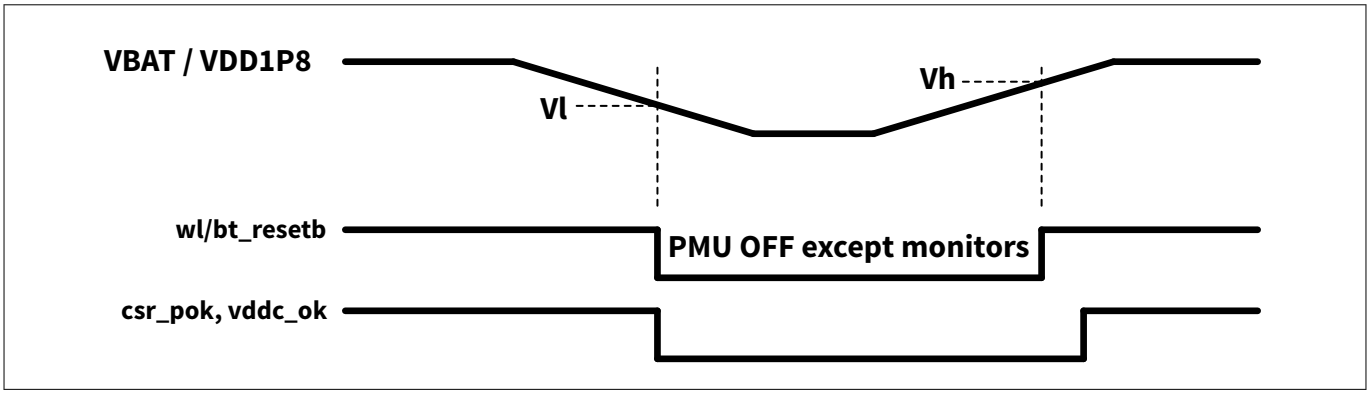


Figure 4 Brownout and UVLO

3 Frequency references

The CYW5591x requires two reference frequencies. One is an external 37.4 MHz crystal for the RF section and a 32.768 kHz reference oscillator for low-power operation.

3.1 Crystal interface and clock generation

CYW5591x can use an external crystal to provide a frequency reference. The recommended configuration for the crystal oscillator including all external components is shown in Figure 5. See the reference schematics for the latest configuration.

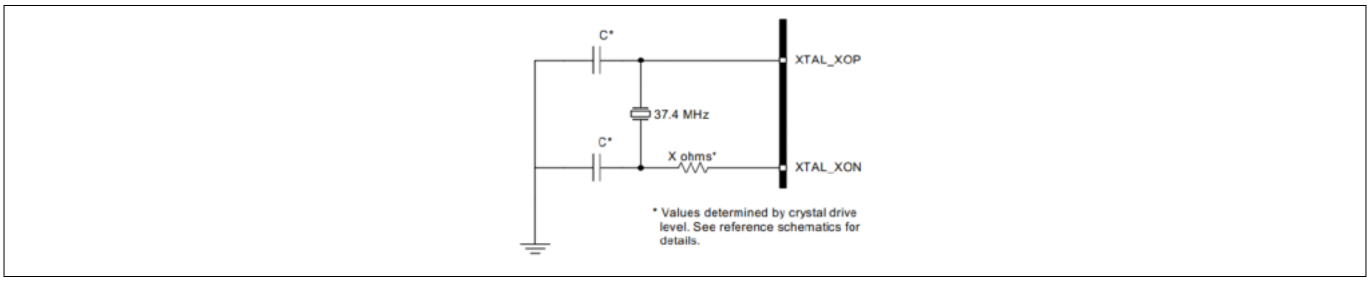


Figure 5 Recommended crystal oscillator configurator

The required default frequency reference is a 37.4 MHz crystal. The signal characteristics for the crystal oscillator interface are listed in Table 2.

Table 2 Crystal oscillator - Requirements and performance

Parameter	Conditions	Crystal [1]			
		Min	Typ	Max	Unit
Frequency	2.4G, 5G, 6G bands: IEEE 802.11ac/ax	–	37.4	–	MHz
Frequency tolerance over the lifetime of the equipment, including temperature[2]	Without trimming	–20.0	–	20.0	ppm
Crystal load capacitance	–	–	12.0	–	pF
ESR			–	60	Ω
Drive level	External crystal must be able to tolerate this drive level		–	200	µW
Input impedance XTAL_XOP	Resistive	–			kΩ
	Capacitive			7.5	pF

1) Use XTAL_XOP and XTAL_XON.
2) It is the responsibility of the equipment designer to select oscillator components that comply with these specifications.

3.2 External frequency reference

As an alternative to a crystal, an external precision frequency reference can be provided. The recommended default frequency is 37.4 MHz, and it must meet the requirements listed in Table 3. The external frequency reference should be connected to the XTAL_XOP pin through an external 1000 pF coupling capacitor, as shown in Figure 6.

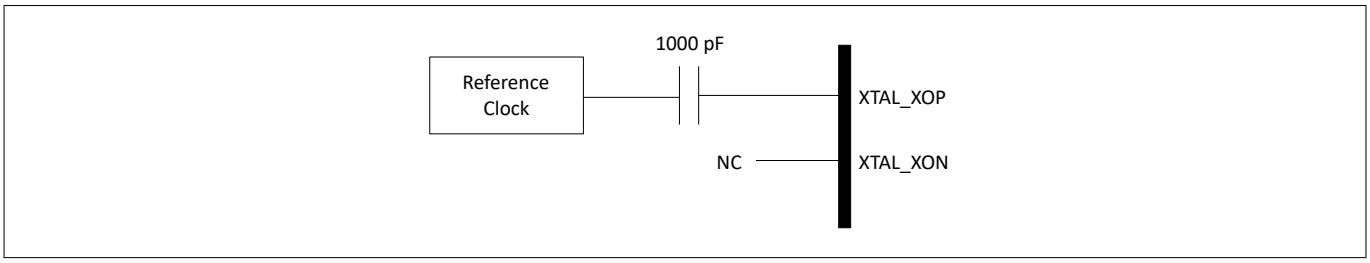


Figure 6 Recommended circuit to use with an external reference clock

The internal clock buffer connected to this pin will be turned OFF when CYW5591x goes into Sleep mode. When the clock buffer turns ON and OFF there will be a small impedance variation. Power must be supplied to the BTRF_LDO_VDD_1P12 pin.

Table 3 External clock - Requirements and performance

Parameter	Conditions	External frequency reference			Unit
Frequency	2.4G, 5G, and 6G: IEEE 802.11ac/ax operation	–	37.4	–	MHz
Frequency tolerance over the lifetime of the equipment, including temperature[1)]	Without trimming	-20.0	–	20	ppm
Input impedance (XTAL_XOP)	Resistive	30	100	–	kΩ
	Capacitive	–		7.5	pF
XTAL_XOP input low level	DC-coupled digital signal	0		0.2	V
XTAL_XOP input high level	DC-coupled digital signal	0.8		1	
XTAL_XOP input voltage	AC-coupled analog signal	400		1000	mVp-p
Duty cycle	37.4 MHz clock	40	50	60	%
Phase noise (IEEE 802.11b/g)	37.4 MHz clock at 10 kHz offset	–	–	–129	dBc/Hz
	37.4 MHz clock at 100 kHz offset			–136	
Phase noise[2)] (IEEE 802.11a)	37.4 MHz clock at 10 kHz offset			–137	
	37.4 MHz clock at 100 kHz offset			–144	
Phase noise[2)] (IEEE 802.11n, 2.4 GHz)	37.4 MHz clock at 10 kHz offset			–134	
	37.4 MHz clock at 100 kHz offset			–141	

(table continues...)

Table 3 (continued) External clock - Requirements and performance

Parameter	Conditions	External frequency reference			Unit
Phase noise[2] (IEEE 802.11n, 5/6 GHz)	37.4 MHz clock at 10 kHz offset			–142	
	37.4 MHz clock at 100 kHz offset			–149	
Phase noise[2] (IEEE 802.11ac, 5/6 GHz)	37.4 MHz clock at 10 kHz offset			–150	
	37.4 MHz clock at 100 kHz offset			–157	
Phase noise[2] (IEEE 802.11ax, 5/6 GHz)	37.4 MHz clock at 10 kHz offset			–152	
	37.4 MHz clock at 100 kHz offset			–159	

1) It is the responsibility of the equipment designer to select oscillator components that comply with these specifications.
2) Assumes that external clock has a flat phase noise response above 100 kHz.

3.3 32.768 kHz low-power oscillator

CYW5591x requires a 32.768 kHz reference oscillator for the sleep clock.

The following are the possible clock configurations (for low power):

- Internal low power oscillator[4], [5]
- External LPO (eLPO) with external crystal connected to LHL_XTALI, LHL_XTALO. In case 32.768 kHz clock source is not from eLPO with external crystal, then LHL_XTALI should be connected to GND
- External LPO clock connected to LPO_IN_OUT, digital 32.768 kHz clock input. In case 32.768 kHz clock source is not from the external LPO clock, then LPO_IN_OUT should be connected to GND. This is a free running clock as long as the device REG_ON is ON

An external 32.768 kHz precision oscillator which meets the requirements listed in Table 4 should be used.

Table 4 External 32.768 kHz sleep clock specifications

Parameter	LPO clock	Unit
Nominal input frequency	32.768	kHz
Frequency accuracy	±250	ppm
Duty cycle	30–70	%
Input signal amplitude	200–1800	mV, p-p
Signal type	Square-wave or sine-wave	–
Input impedance[1]	> 100k	Ω
	< 5	pF
Clock jitter [2] (during initial startup)	< 10,000	ppm

4 Internal LPO accuracy is only adequate for WLAN, and not for Bluetooth® if low power for Bluetooth®Low-Energy required.
5 Improved HW/SW calibration schemes allows to achieve ILPO effective variation of less than 1% across PVT.

1) When power is applied or switched OFF.
2) The LPO_IN input receiver has ac-coupled capacitance on the input with the feedback resistor to maintain the common mode around VDDIO/2 and power supply noise should be maintained less than 100 mV to avoid any false glitches before the time constant (ac-coupled capacitance * feedback resistor, i.e., 100 µs) settles down.

The LPO_OUT feature of which is primarily used to provide clock input to an external chip if required. On POR, LPO_IN_OUT pin functions only as an input for eLPO. Software configuration of the pins is needed to enable it as a clock output or as a GPIO. Please note that clock output or GPIO feature can be used only if eLPO is not connected to CYW5591x and external 32.768 kHz crystal is available.

CYW5591x can drive 32.768 kHz clock out as source for any external chip. It uses LPO_IN_OUT pin to drive out the clock. This feature is disabled by default and LPO_IN_OUT pin is used to provide external reference clock. External crystal (32.768 kHz) availability is prerequisite to enable this feature using software.

Table 5 32 kHz crystal specifications

Parameter	Crystal			
	Min.	**Typ.**	**Max.**	**Unit**
Frequency	_	32.768	_	KHz
Frequency tolerance	–20	_	+20	ppm
Crystal load capacitance	_	6.0	_	pF
Equivalent Series Resistance	_	_	90	kΩ
Driver level	_	0.1	0.5	µW

3.3.1 Watchdog

The watchdog timer is configurable, allowing for adjustable time-out periods ranging from two to five seconds in one-second increments, providing precise control over the maximum time-out duration.

4 Bluetooth® LE Subsystem

CYW5591x contains a Bluetooth® LE subsystem which contains a Bluetooth® LE 5.4, baseband processor and 2.4 GHz transceiver. It features the highest level of integration and eliminates the need for all critical external components, thus minimizing the footprint, power consumption, and system cost of a Bluetooth® solution. CYW55913/55912/55911 incorporates Bluetooth® LE features. CYW5590x do not support Bluetooth® LE.

The Bluetooth® transmitter also features a power amplifier with programmable Class 1 and Class 2 capabilities with three output paths supporting +4 dBm, +13 dBm, or +19 dBm output power. The Bluetooth® receiver has option to be shared with the 2.4 GHz WLAN receive path or dedicated Bluetooth® Rx shared with the Bluetooth® +4 dBm power amplifier.

4.1 Features

- Supports features of Bluetooth® core specification v 5.4:
  - Advertising Coding Selection
  - Encrypted Advertising Data
  - LE Generic Attribute Profile (GATT) Security Levels Characteristic
- Supports features of Bluetooth® core specification v 5.3:
  - LE connection subrating
  - LE Channel Classification
  - Periodic advertising ADI support
  - LE Enhanced Connection Update
- Supports features of Bluetooth® Core Specification v 5.2:
  - LE Isochronous Channels (No LE Audio)
  - Enhanced Attribute Protocol
  - LE Power Control
- Supports features of Bluetooth® Core Specification v 5.1:
  - Periodic Advertising Sync Transfer (PAST)
  - GATT Caching
  - Control Length Extension
  - Advertising Channel Index
- Supports features of Bluetooth® Core Specification v 5.0:
  - LE 2M PHY
  - LE Long Range (LE-LR)
  - LE Coded PHY
  - Stable Modulation Index for LE
  - LE Advertising Extension
  - Slot Availability Masks (SAM)
  - Channel Selection Algorithm #2
  - High Duty Cycle Non-Connectable Advertising
- Supports features of Bluetooth® Core Specification v 4.0:
  - Adaptive frequency hopping (AFH)
  - Quality of service (QoS)
  - Encryption pause resume (EPR)
  - Link supervision timeout (LST)

- UART baud rates < 7.4 Mbps
- Supports all Bluetooth® 4.2, 5.0, 5.1, 5.2, 5.3 and 5.4 packet types
- Maximum BLE connections - eight in central and four in peripheral roles simultaneously
- Narrowband and wideband packet loss concealment
- Standard Bluetooth® LE test mode
- Extended radio and production test mode features
- Full support for power savings modes
  - Bluetooth® clock request
  - Deep-sleep modes and software regulator shutdown
- TCXO input and auto-detection of all standard handset clock frequencies. Also supports a low-power crystal, which can be used during power save mode for better timing accuracy.

5 Bluetooth® baseband core (BBC)

The BBC implements all of the time-critical functions required for high-performance Bluetooth® operation. The BBC manages the buffering, segmentation, and routing of data for all connections. It also buffers data that passes through it, handles data flow control, schedules ACL TX/RX transactions, monitors Bluetooth® slot usage, optimally segments and packages data into baseband packets, manages connection status indicators, and composes and decodes HCI packets. In addition to these functions, it independently handles HCI event types, and HCI command types.

The following TX and RX functions are also implemented in the BBC hardware to increase reliability and security of the TX/RX data before sending over the air:

- Symbol timing recovery, data deframing, forward error correction (FEC), cyclic redundancy check (CRC), data decryption, and data dewhitening in the receiver.
- Data framing, FEC generation, CRC generation, key generation, data encryption, and data whitening in the transmitter.

5.1 Test mode support

CYW5591x fully supports Bluetooth® Test mode as described in Part I:1 of the specification of the Bluetooth® system v5.4. This includes the transmitter tests . In addition to the standard Bluetooth® Test mode, CYW5591x also supports enhanced testing features to simplify RF debugging and qualification and type-approval testing.

These features include:

- Fixed frequency carrier wave (unmodulated) transmission
  - Simplifies some type-approval measurements (Japan)
  - Aids in transmitter performance analysis
- Fixed frequency constant receiver mode
  - Allows for direct PER measurements using standard RF test equipment
  - Facilitates spurious emissions testing for receive mode
- Fixed frequency constant transmission
  - 8-bit fixed pattern or PRBS-9
  - Enables modulated signal measurements with standard RF test equipment

5.2 Bluetooth® PMU

The Bluetooth® PMU provides power management features that can be invoked by either software through power management registers or packet handling in the baseband core. The power management functions provided by CYW5591x are:

- RF power management
- Host controller power management
- BBC power management

5.3 RF power management

The BBC generates power-down control signals for the TX path, RX path, PLL, and PA to the 2.4 GHz transceiver. The transceiver then processes the power-down functions accordingly.

5.4 Host controller power management

Any GPIO could be used as wake-up source for the Connected MCU and similarly any GPIO could be configured to wake an external host controller or MCU.

5.5 Advanced Bluetooth®/WLAN coexistence

CYW5591x includes advanced coexistence technologies that are only possible with a Bluetooth®/WLAN integrated die solution.. The CYW5591x is capable of supporting antenna shared with WLAN for lowest cost or a dedicated Bluetooth® antenna where the highest throughput and lowest latency WLAN and Bluetooth® is required. Advanced Bluetooth®/WLAN coexistence algorithms allow for simultaneous WLAN and Bluetooth® reception and transmit antenna arbitration. CYW5591x integrated solution enables MAC-layer signaling (firmware) and a greater degree of sharing via an enhanced coexistence interface. Information is exchanged between the Bluetooth® and WLAN cores without host processor involvement. CYW5591x also supports TX power control on the WLAN STA together with standard Bluetooth® TPC to limit mutual interference and receiver desensitization. Pre-emption mechanisms are utilized to prevent AP transmissions from colliding with Bluetooth® frames. Improved channel classification techniques have been implemented in Bluetooth® for faster and more accurate detection and elimination of interferers (including non-WLAN 2.4 GHz interference).

6 Connected MCU

6.1 CPU

AIROC™ CYW5591x Connected MCU subsystem contains a 32-bit Arm® Cortex®-M33 CPU with clock speed up to 192 MHz with MPU, single precision FPU, 2048 KB of ROM, SRAM of 704 KB, 64 KB of patch RAM and with no cache.

At power-up, the lower-layer protocol stack is executed from the internal ROM memory. Patches may be applied to the ROM-based firmware to provide flexibility for bug fixes or feature additions.

6.2 ROM

CYW5591x Connected MCU provides 2048 KB of ROM that contains boot and configuration routines. This ROM enables secure boot to guarantee a secure system.

- ThreadX RTOS
- NetX Secure TLS 1.3
- NetX Duo (TCP/IP)

6.3 Security system (Arm® TrustZone CryptoCell 312)

CYW5591x Connected MCU provides security using the Arm® TrustZone CryptoCell 312 which enables the following services:

- Symmetric and asymmetric cryptography
- True random number generator (TRNG)
  - Random number (derived from NIST compliant DRBG)
- Device lifecycle state management
- Root of Trust access policy enforced by hardware means
- Root of Trust ownership model allowing multiple entities to own different trust anchor, removing the need for default trust between entities along the value chain
- Keys and assets provisioning, management, and isolation, across different device operational scenarios, both in-factory and in the field
- Software image validation and optional decryption both at boot time and update time
- Attestation

The following cryptographic (CC312 H/W accelerated) services are provided:

- AES (Symmetric crypto)
  - Block sizes: 128 bits, 192 bits and 256 bits
  - Accelerated operations for CBC, CTR, XCBC, CCM 8
- RSA (Asymmetric crypto)
  - 1 Kb, 2 Kb, 3 Kb, and 4 Kb key-sizes are supported
- Elliptic curve cryptography (ECC) (Asymmetric crypto)
  - SECP curves 192r1/224r1/256r1/384r1/521r1)
    - ECDH
    - ECDSA
- Hashes
  - Accelerated: SHA-1, SHA-224, SHA-256 and MD5

- Non-accelerated: SHA-384 and SHA-512
- Keyed-hash message authentication code (HMAC)

7 Peripherals

7.1 12-bit ΔΣ-ADC and low-power comparator

CYW5591x consists of two low power comparators (LPCOMP) and a 7-channel 12-bit ΔΣ ADC to provide sensing and monitoring of input signals connected to the GPIO and connection of a single-ended analog microphone. The LPCOMPs and ADC each has their own control signals to allow measurement configuration flexibilities and power saving when not in use. The ADC and LPCOMP are powered by a single supply voltage of 1.8 V.

The following are the general features for ADC:

- Third order 1-bit continuous-time ΔΣ
- Output sampling rate 16 ksps
- MIC bias reference at 1.8 V
- MIC PGA gain range 0-18 dB (eight linear steps)

LPCOMP features a programmable noise threshold in 16 linear steps.

The system supports two modes of operations: DC and noise threshold detection (NTD) modes. In DC mode, DC input signals are routed through the 7-GPIO pins, this mode can be used for sampling sensors like thermistor, etc. In NTD mode audio signal is routed from the analog microphone to the microphone input through an AC coupling capacitor.

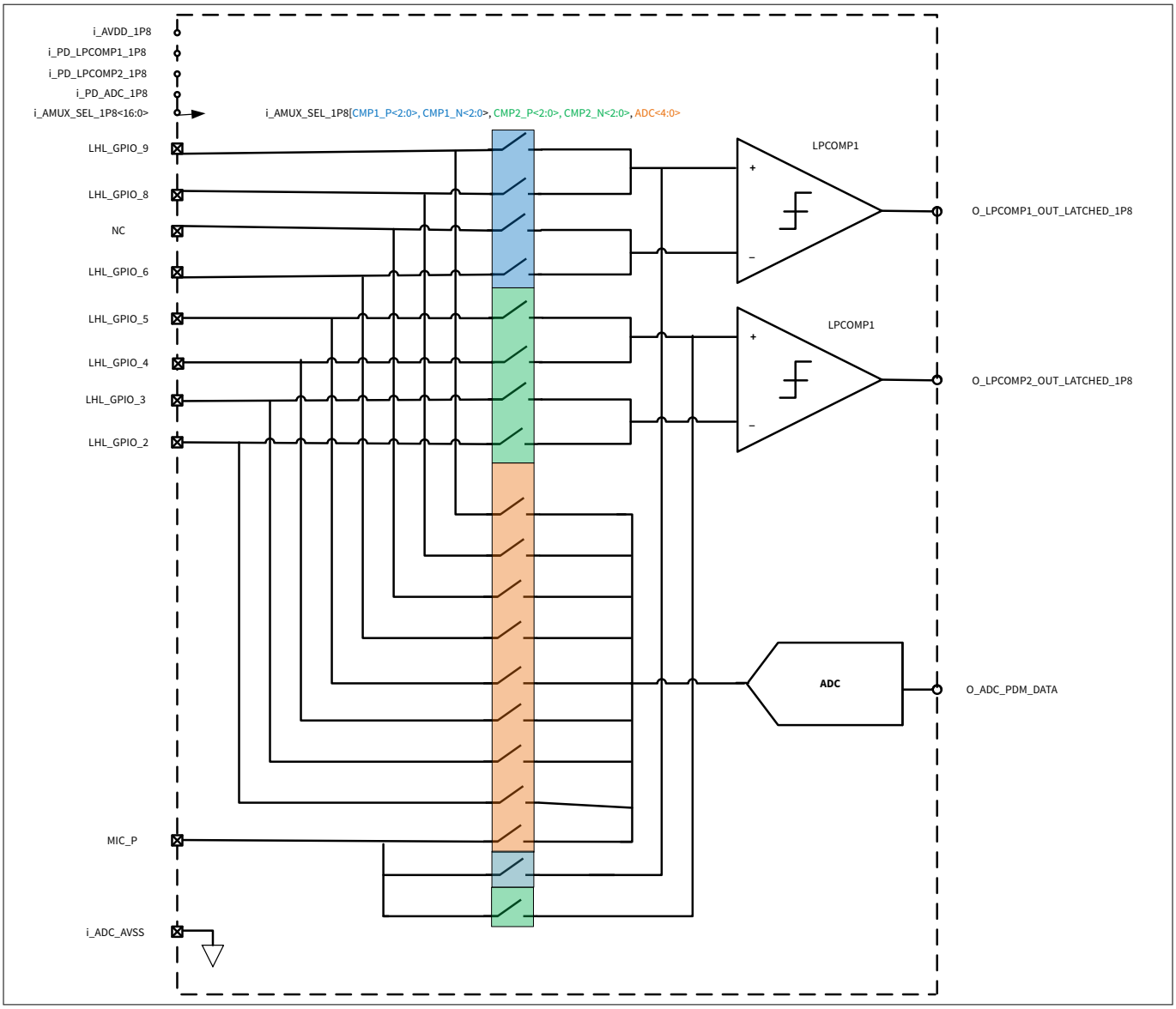


Figure 7 ADC block diagram

Table 6 ADC block diagram pin description

Pin name	I/O	Description
i_AVDD_1P8	I	System 1.8 V supply from an external SR
I_ADC_AVSS	I	Low-impedance direct ground reference to ADC
i_PD_LPCOMP1_1P8	I	Default: 1. LPCOMP1 power up/down controlled by 1.8 V power up/down signal: 0: LPCOMP1 is powered up 1: LPCOMP1 is powered down (default)

(table continues...)

Table 6 (continued) ADC block diagram pin description

Pin name	I/O	Description
i_PD_LPCOMP2_1P8	I	Default: 1. LPCOMP2 power up/down controlled by 1.8 V power up/down signal: 0: LPCOMP2 is powered up 1: LPCOMP2 is powered down (default)
i_PD_ADC_1P8	I	Default: 1. ADC power up/down controlled by 1.8 V power up/down signal: 0: ADC is powered up 1: ADC is powered down (default)
i_AMUX_SEL_1P8<16:0>	I	Multiplexer configuration (see mapping in Table 7)
LHL_GPIO_<9:2>	I	GPIO inputs for ADC input signals
i_MIC	I	AC input signal from analog microphone or AC source, Rin = 375 kΩ
o_LPCOMPn_OUT_LATCHED_1P8 (n = 1,2)	O	Latched LPCOMPn output (1.8 V) when noise above threshold is detected
o_ ADC_PDM_DATA	O	ADC PDM bitstream

Table 7 Multiplexer register configuration mapping

	Value	MUX input	MUX output
i_AMUX_SEL_1P8<16:0>			
CMP1_P<2:0>	000	LHL_GPIO_<8>	LPCOMP1_P
	001	LHL_GPIO_<9>	LPCOMP1_P
	01x	i_MIC	LPCOMP1_P
	1xx	OPEN	LPCOMP1_P
CMP1_N<2:0>	000	LHL_GPIO_<6>	LPCOMP1_N
	001	LHL_GPIO_<7>[1)]	LPCOMP1_N
		OPEN	LPCOMP1_N
	1xx	OPEN	LPCOMP1_N
CMP2_P<2:0>	000	LHL_GPIO_<4>	LPCOMP2_P
	001	LHL_GPIO_<5>	LPCOMP2_P
	01x	PDM_DMIC	LPCOMP2_P
	1xx	OPEN	LPCOMP2_P
CMP2_N<2:0>	000	LHL_GPIO_<2>	LPCOMP2_N

(table continues...)

Table 7 (continued) Multiplexer register configuration mapping

	Value	MUX input	MUX output
	001	LHL_GPIO_<3>	LPCOMP2_N
	01x	OPEN	LPCOMP2_N
	1xx	OPEN	LPCOMP2_N
ADC<4:0>	00000	LHL_GPIO_<2>	ADC
	00001	LHL_GPIO_<3>	ADC
	00010	LHL_GPIO_<4>	ADC
	00011	LHL_GPIO_<5>	ADC
	00100	LHL_GPIO_<6>	ADC
	00101	LHL_GPIO_<7>[1)]	ADC
	00110	LHL_GPIO_<8>	ADC
	00111	LHL_GPIO_<9>	ADC
	01xxx	PDM_DMIC	ADC
	1xxxx	OPEN	ADC

1) LHL_GPIO_7 is reserved as not available for user, making the total available channels to seven.

7.2 Timer

CYW5591x consists of 2x timer instances which are dual timers of which one instance will be used internally by the system software. The user application will have one instance of the dual timer.

The timer has the following programmable features:

- Free-running, periodic, or one-shot timer modes
- 32-bit or 16-bit timer operation
- Prescaler divider of 1, 16, or 256
- Interrupt generation enable and disable
- Interrupt masking

7.3 IOs

7.3.1 GPIO

CYW5591x consists of 48 pins that could be used for GPIO function. These pins which can act as GPIOs have following configuration options available:

- Drive strength: Minimum value of 2 mA and maximum value of 16 mA with steps of 2 mA.
- Pull up/pull down control
- Input hysteresis control
- Slew rate control
- Input disable control

These pins which can act as GPIO are designed for nominal VDDO = 1.80 ± 10% operation but can operate down to VDDO = 1.10 - 10% (0.99 V) at reduced drive strength. If VDDO is unpowered, the pad is failsafe up to 1.98 V.

The HOLD feature keeps the pad in its current state by using a 600k feedback resistor. RF_SW_CTRL6 and RF_SW_CTRL7 are 3.3V GPIOs which are referenced to (VDDIO_RFSW)

7.3.2 Little Hibernate Logic (LHL) GPIO

There are 10 LHL GPIO's having same configuration options available as regular GPIO's. One use case is the use of these pins for providing DC input to the ADC for sensing and monitoring. The LHL_GPIOs can multiplex various peripheral functions (as listed in), with the unique capability of accepting analog inputs. These GPIOs have a maximum operating frequency of 8 MHz.

7.4 Serial Communication Block (SCB)

CYW5591x consists of up to three serial communication blocks, each configurable to support I2C, UART, or SPI.

7.4.1 I2C interface

CYW5591x SCB

- An SCB can be configured to implement a full I2C master (capable of multi-master arbitration) or slave interface. Each SCB configured for I2C can operate at speeds of up to 1 Mbps (Fast-mode Plus[8]) and has flexible buffering options to reduce the interrupt overhead and latency of the CPU. In addition, each SCB supports FIFO buffering for receive and transmit data, which, by increasing the time for the CPU to read the data, reduces the need for clock stretching. The I2C interface is compatible with Standard, Fast-mode, and Fast-mode Plus devices as specified in the NXP I2C-bus specification and user manual (UM10204). The I2C-bus I/O is implemented with GPIO in open-drain modes [6], [7]
- I2C slave EZ (EZI2C[8]) mode with up to 256-B data buffer for multi-byte communication without CPU intervention
- I2C slave externally-clocked operations
- Command/response mode with a 512-B data buffer for multi-byte communication without CPU intervention

7.4.2 SPI interface

CYW5591x SCB

- The SPI configuration supports full Motorola SPI, TI Synchronous Serial Protocol (SSP, essentially adds a start pulse that is used to synchronize SPI-based codecs), and National Microwire (a half-duplex form of SPI). The SPI interface can use the FIFO. The SPI interface can run up to a max clock of 24 MHz (limited by GPIO timing). SCB also supports EZSPI[9] mode. The SCB supports the following additional features:
  - Operable as a slave in DeepSleep mode

6 I/Os drive level does not support the full bus capacitance in Fast-mode Plus speeds.
7 This is not 100 percent compliant with the I2C-bus specification; I/Os are not high-voltage compliant, do not support the 20-mA sink requirement of Fast-mode Plus, and violate the leakage specification when no power is applied.
8 The Easy I2C (EZI2C) protocol is a unique communication scheme built on top of the I2C protocol by Infineon. It uses a meta protocol around the standard I2C protocol to communicate to an I2C slave using indexed memory transfers. This reduces the need for CPU intervention.
9 The Easy SPI (EZSPI) protocol is based on the Motorola SPI operating in any mode (0, 1, 2, or 3). It allows communication between master and slave, and reduces the need for CPU intervention.

7.4.3 UART interface

CYW5591x SCB when configured as a UART, each SCB provides a full-featured UART with maximum signaling rate determined by the configured peripheral-clock frequency and over-sampling rate. It supports infrared interface (IrDA) and SmartCard (ISO 7816) protocols, which are minor variants of the UART protocol. It also supports the 9-bit multiprocessor mode that allows the addressing of peripherals connected over common Rx and Tx lines. Common UART functions such as parity, number of stop bits, break detect, and frame error are supported. FIFO buffering of transmit and receive data allows greater CPU service latencies to be tolerated. The LIN protocol is supported by the UART. LIN is based on a single-master multi-slave topology. There is one master node and multiple slave nodes on the LIN bus. The SCB UART supports only LIN slave functionality. Compared to the dedicated LIN blocks, an SCB/UART used for LIN requires a higher level of software interaction and increased CPU load.

7.5 BT UART

The BT UART primarily serves as a programming interface, but it also has the capability to function as a general-purpose UART. Additionally, it supports high-speed data transfer with a maximum baud rate of up to 4 Mbps. BT UART is available for user.

The baud rate may be selected through a vendor-specific UART HCI command. UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA/CPU. The UART supports the Bluetooth® UART specification. The default baud rate is 115.2 Kbaud. CYW5591x UART can perform XON/XOFF flow control and includes hardware support for the serial line input protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state. Normally, the UART baud rate is set by a configuration record downloaded after device reset and the host does not need to adjust the baud rate. Support for changing the baud rate during normal BT UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. CYW5591x UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within ±2%.

Table 8 Example of common baud rates

Desired rate	Actual rate	Error (%)
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00

(table continues...)

Table 8 (continued) Example of common baud rates

Desired rate	Actual rate	Error (%)
14400	14423	0.16
9600	9600	0.00

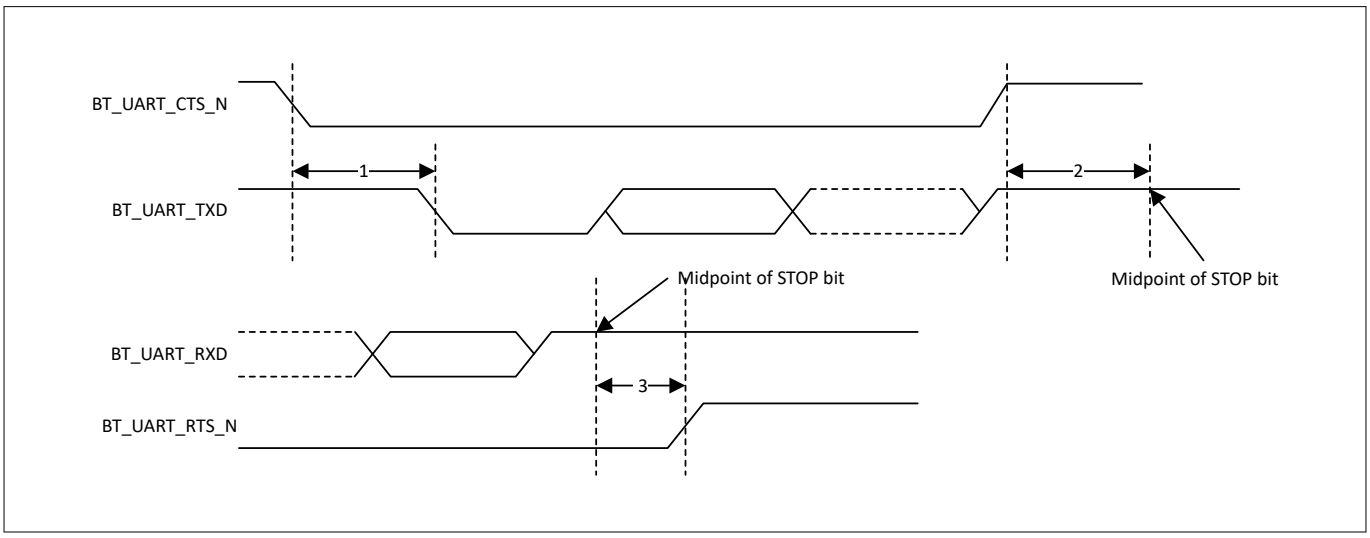


Figure 8 UART timing

Table 9 UART timing specification

Reference	Characteristics	Min	Typ	Max	Unit
1	Delay time, BT_UART_CTS_N LOW to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_N HIGH before midpoint of stop bit			0.5	
3	Delay time, midpoint of stop bit to BT_UART_RTS_N HIGH			0.5	

7.6 TDM

CYW5591x contains a TDM block. The following are the characteristics of the interface:

- A pair of TDM interfaces (TDM1 and TDM2) are available, and each TDMx (TX and RX) consists of a TDM transmitter and a TDM receiver
- The transmitter and receiver can function simultaneously and have a dedicated clock control
- The transmitter and receiver have a dedicated FIFO interrupt and FIFO trigger
- A single interface consists of a TDM transmitter and a TDM receiver
- Both, transmitter and receiver support master and slave functionality

Following are the features of the TDM block:

- Supports I2S or TDM/PCM functionality
- Full-duplex transmitter and receiver operation
- Support for up to eight channels. Each channel can be individually enabled/disabled
- Programmable Interface clock
- Programmable half cycle delayed sampling support

- Programmable late capture extra delay of 1, 2 or 3 cycles, for multi-cycle round-trip latencies in receiver master mode
- Programmable PCM sample formatting (8, 10, 12, 14, 16, 18, 20, 24, 32 bits)
- Supports all common sampling frequencies: 4 / 8 / 11.025 / 12 / 16 / 20 / 22.05 / 24 / 30 / 32 / 40 / 44.1 / 48 / 60 / 96 kHz
- 8-channel (each 32-bit) TDM can operate at a maximum data rate of 48 kHz for Tx and Rx.
- Programmable synchronization pulse type
- Left-aligned and right-aligned sample formatting
- Test mode (transmitter to receiver loopback)

Operating modes

Each TDM transmitter and receiver can be configured independently. They have two possible configurations – master and slave. Masters output the TDM clock and frame sync, slaves on the other hand take the same signals as inputs. The operating modes are shown in the Figure 9.

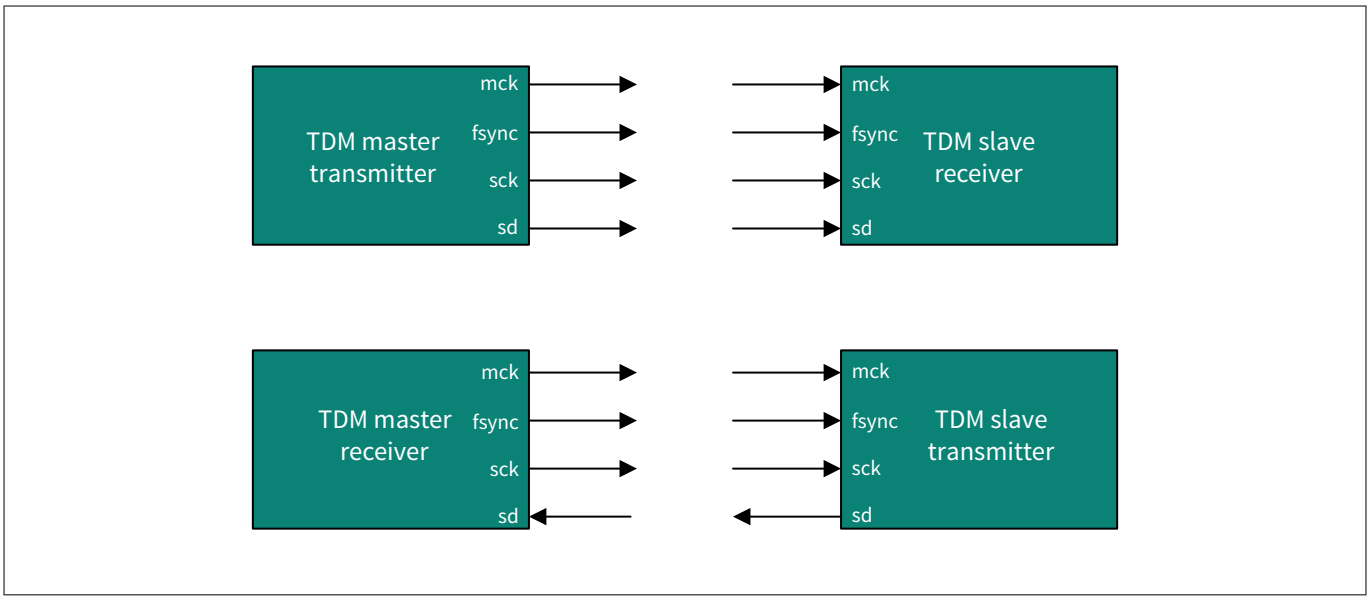


Figure 9 Operating modes

7.7 PDM

CYW5591x supports digital PDM microphone interface and provides support for 512 kHz, 1 MHz, and 2 MHz microphone clock. Internally, the PDM samples are captured and converted to 16 bit PCM samples. The PDM to PCM conversion block supports both 16 kHz and 8 kHz data rates. CYW5591x supports the following digital mic configurations.

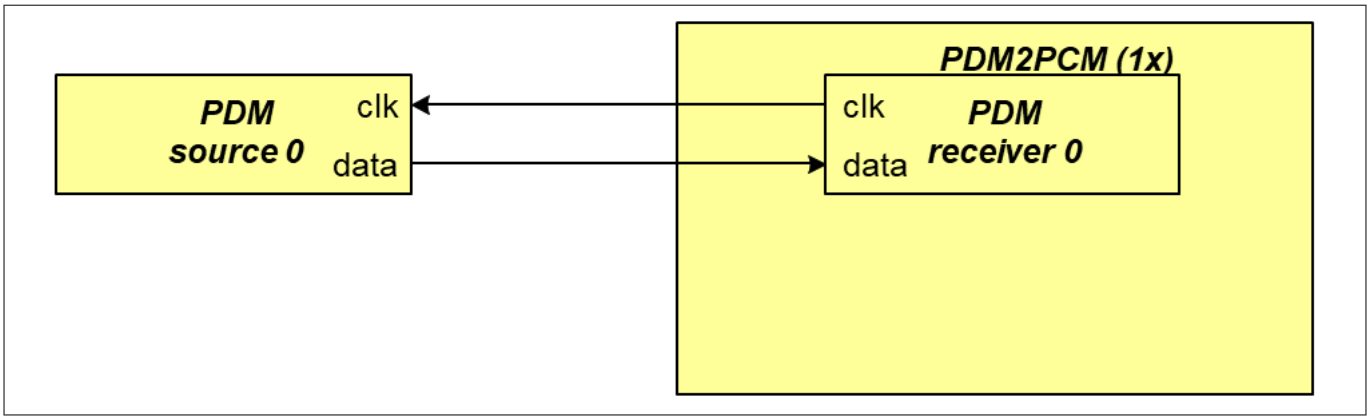


Figure 10 Single microphone

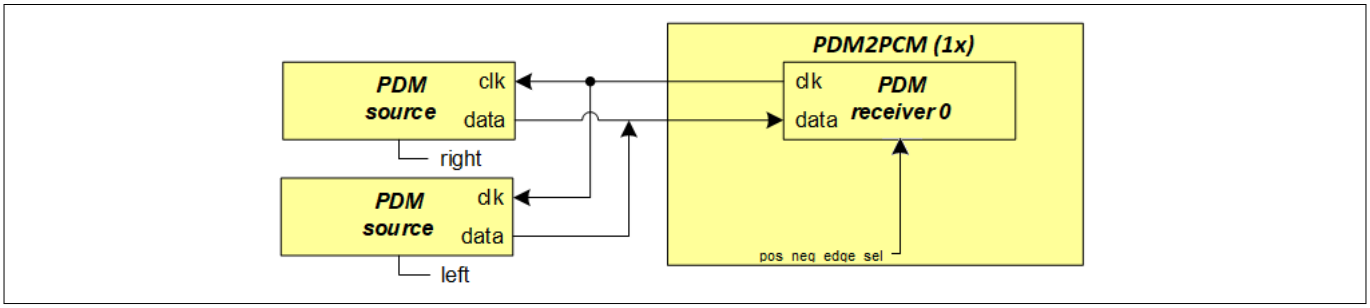


Figure 11 Selectable mono (L & R) shared data line

7.7.1 Timing counter pulse width modulator (TCPWM)

CYW5591x provides nine TCPWM instances. The TCPWM block has the following features:

- 16- or 32-bit counter, compare/capture (CC) and period registers
- Up, down and up/down counting modes
- Support for one interrupt output for each counter
- Two PWM complementary output lines for each counter with dead time insertion
- Functional modes:
  - Timer: Counter increments or decrements by every counter clock cycle in which a count cyle is detected
  - Capture
  - Counter increments or decrements by every counter clock cycle in which a count event is detected. A capture event copies the counter value into the capture register.
  - Quadrature: Quadrature decoding. Counter is decremented or incremented based on two phases according to X1, X2, or X4 encoding scheme.
  - Pulse-width modulation (PWM)
  - PWM with clock pre-scaling
  - PWM with dead time insertion, 8-bit (PWM_DT)
  - Pseudo Random (PWM_RR) with modulation which uses 16-bits LFSR to generate pseudo random noise

Each TCPWM counter can be programmed to perform the functionality of any of the six modes.

7.8 Serial memory interface (SMIF)

CYW5591x chip provides a serial memory interface (SMIF) which provides a low pin count connection to off-chip (single/dual/quad) SPI devices in SDR or DDR mode.

SMIF provides two modes of operations:

- XIP mode: The read and write transfers are translated on the fly to external device SPI transfers.
- MMIO mode: This mode supports MMIO based accesses to external devices. MMIO operation mode is less efficient than XIP operation mode for read and writes. However, MMIO operation mode is more flexible than XIP operation mode. This flexibility is used to implement device operations other than read and write operations, e.g., programming, changing power mode, etc.

SMIF provides the following operations:

- SPI Master functionality only
- SPI protocol
  - SPI Mode 0 only (CPOL is 0 and CPHA is 0), with configurable MISO sampling timing
  - Support for Single/Dual/Quad/ SPI (S/D/Q SPI transfer mode)
  - Support for Dual-Quad SPI mode
  - Support for Single Data Rate (SDR) at 96 MHz / 48 Mbps and Dual Data Rate (DDR) at 75 MHz / 75 Mbps transfers
- Memory device
  - Support for overall device capacity in the range of (64 KB to 16 MB).
  - Support for configurable external device capacities
  - Support for up to two external memory devices with two chip selects
  - Design time configurable support for multiple (1 or 2) external devices
  - 4 KB dedicated cache
- Memory Mapped IO (MMIO) operation mode
- Boot from external flash
  - XIP operation mode for both read and write accesses
  - XIP mode supports on-the-fly AES-128 encryption and decryption

Figure 12 shows how SMIF can be used to connect to external serial devices.

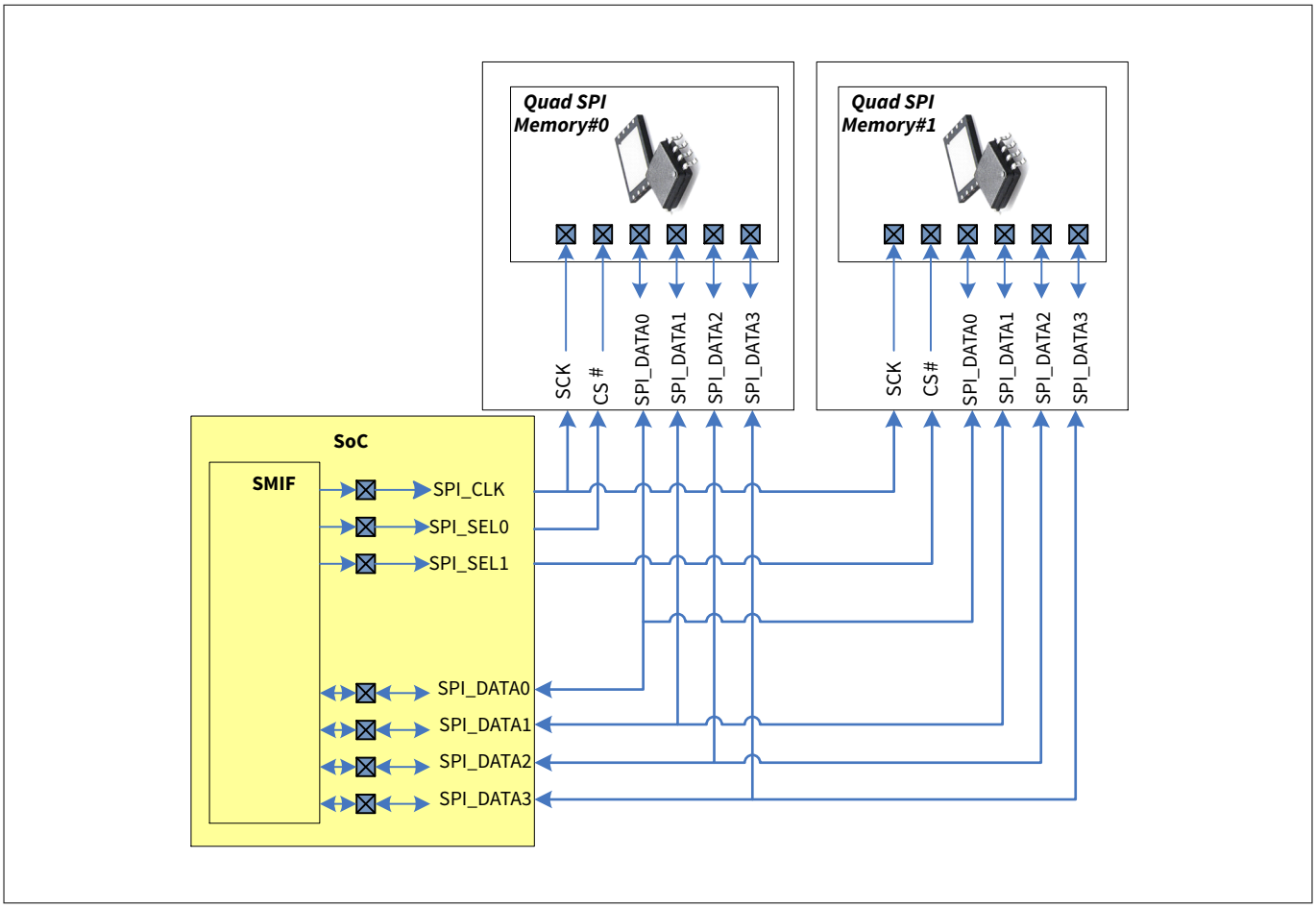


Figure 12 QSPI device example

8 Host interface

8.1 SDIO

All package options of the CYW5591x chip provide support for SDIO V 3.0, including the new UHS-I modes:

- DS: Default speed (DS) up to 25 MHz, including 1 and 4-bit modes (1.8 V signaling)
- HS: High-speed up to 50 MHz (1.8 V signaling)
- SDR12: SDR up to 25 MHz (1.8 V signaling)
- SDR25: SDR up to 50 MHz (1.8 V signaling)
- SDR50: SDR up to 100 MHz (1.8 V signaling)
- DDR50: DDR up to 50 MHz (1.8 V signaling)

***Notes**:*

1. *The UHS-1 rate SDR104, that is part of the SDIO V 3.0 specification is not supported.*

2. *The CYW55913 is backward compatible with SDIO V 2.0 host interfaces. Note however that the CYW55913 device can only support 1.8 V signaling. It cannot support 3.3 V signaling during initialization post power cycle and in default/high speed SDIO V 2.0 modes. The host must use 1.8 V signaling to work with CYW55913.*

The SDIO interface also has the ability to map the interrupt signal on to a GPIO pin for applications requiring an interrupt different from the one provided by the SDIO interface. The ability to force control of the gated clocks from within the device is also provided.

The following three functions are supported:

- Function 0 standard SDIO function (Maximum BlockSize/ByteCount = 32 B)
- Function 1 backplane function to access the internal system on chip (SoC) address space (Max. BlockSize/ ByteCount = 64 B)
- Function 2 DMA for Traffic/Data Exchange

8.1.1 SDIO pins

Table 10 SDIO pin description

SD 4-bit mode		SD 1-bit mode	
DATA0	Data line 0	DATA	Data line
DATA1	Data line 1 or interrupt	IRQ	Interrupt
DATA2	Data line 2 or Read Wait	RW	Read Wait
DATA3	Data line 3	N/C	Not used
CLK	Clock	CLK	Clock
CMD	Command line	CMD	Command line

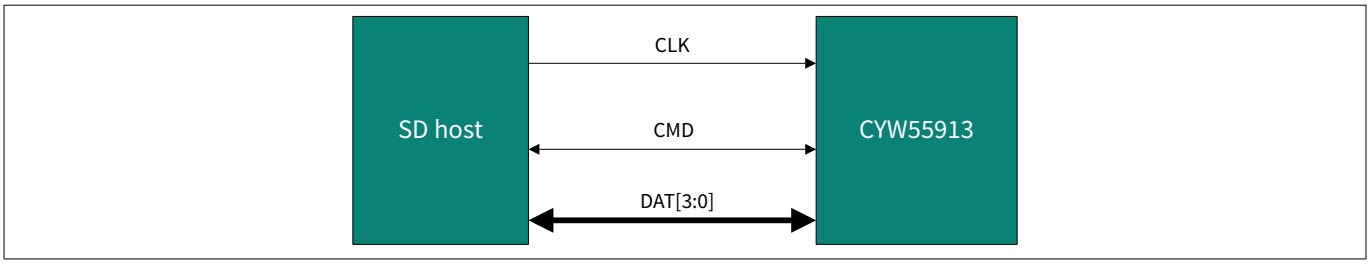


Figure 13 Signal connections to SDIO host (SD 4-bit mode)

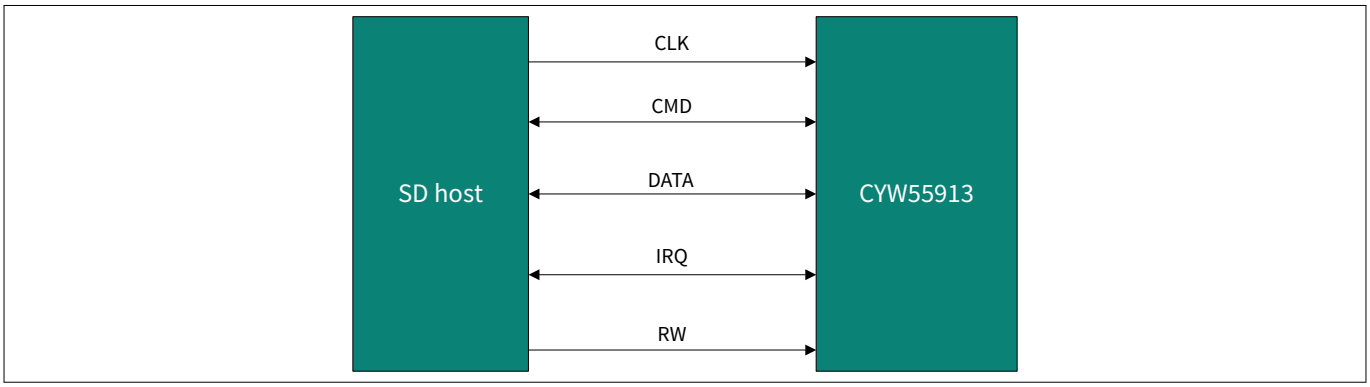


Figure 14 Signal connections to SDIO host (SD 1-bit mode)

***Note**: According to the SDIO specification, pull-ups in the 10 kΩ to 100 kΩ range are required on the four DATA lines and the CMD line. This requirement must be met during all operating states either through the use of external pull-up resistors or through proper programming of the SDIO host's internal pull-ups.*

8.1.2 gSPI

In addition to the full SDIO mode, the CYW55913 includes the option of using the simplified generic SPI (gSPI) interface/protocol.

Characteristics of the gSPI mode include:

- Up to 50-MHz operation
- Fixed delays for responses and data from the device
- Alignment to host gSPI frames (16 or 32 bits)
- Up to 2-KB frame size per transfer
- Little-endian and big-endian configurations
- A configurable active edge for shifting
- Packet transfer for CCM/CP Traffic/Data Exchange

gSPI mode is enabled using the strapping option pins

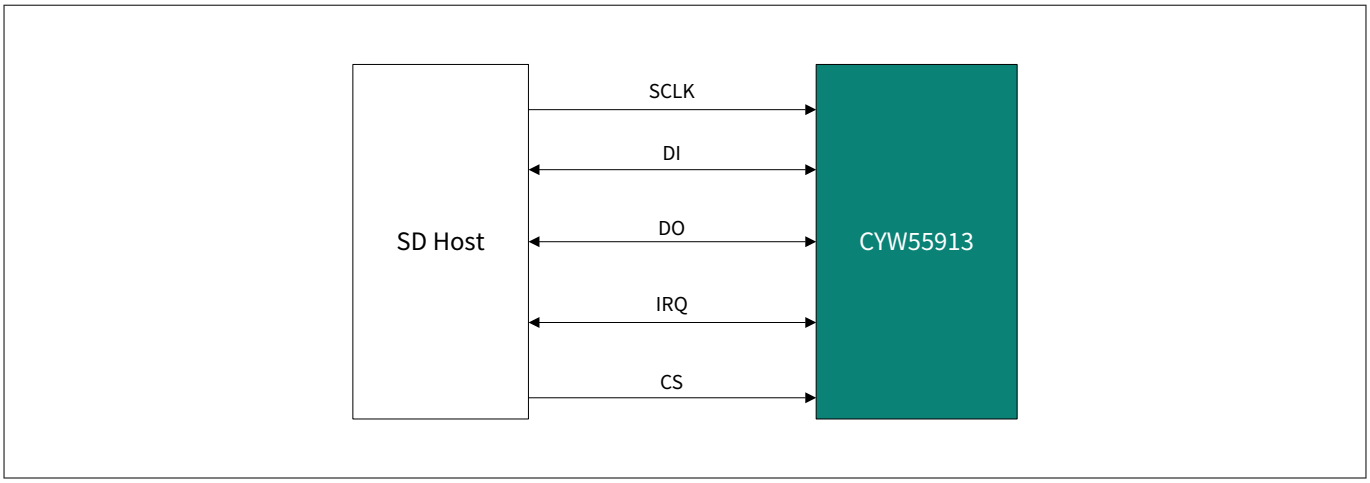


Figure 15 Signal connections to SDIO host (gSPI mode)

According to the SDIO specification, pull-ups in the 10 kΩ to 100 kΩ range are required on the four DATA lines and the CMD line. This requirement must be met during all operating states either through the use of external pull-up resistors or through proper programming of the SDIO host's internal pull-ups.

8.1.2.1 gSPI protocol

The gSPI protocol supports both 16-bit and 32-bit word operation. Byte endianness is supported in both modes. Figure 16 and Figure 17 show the basic write and write/read commands.

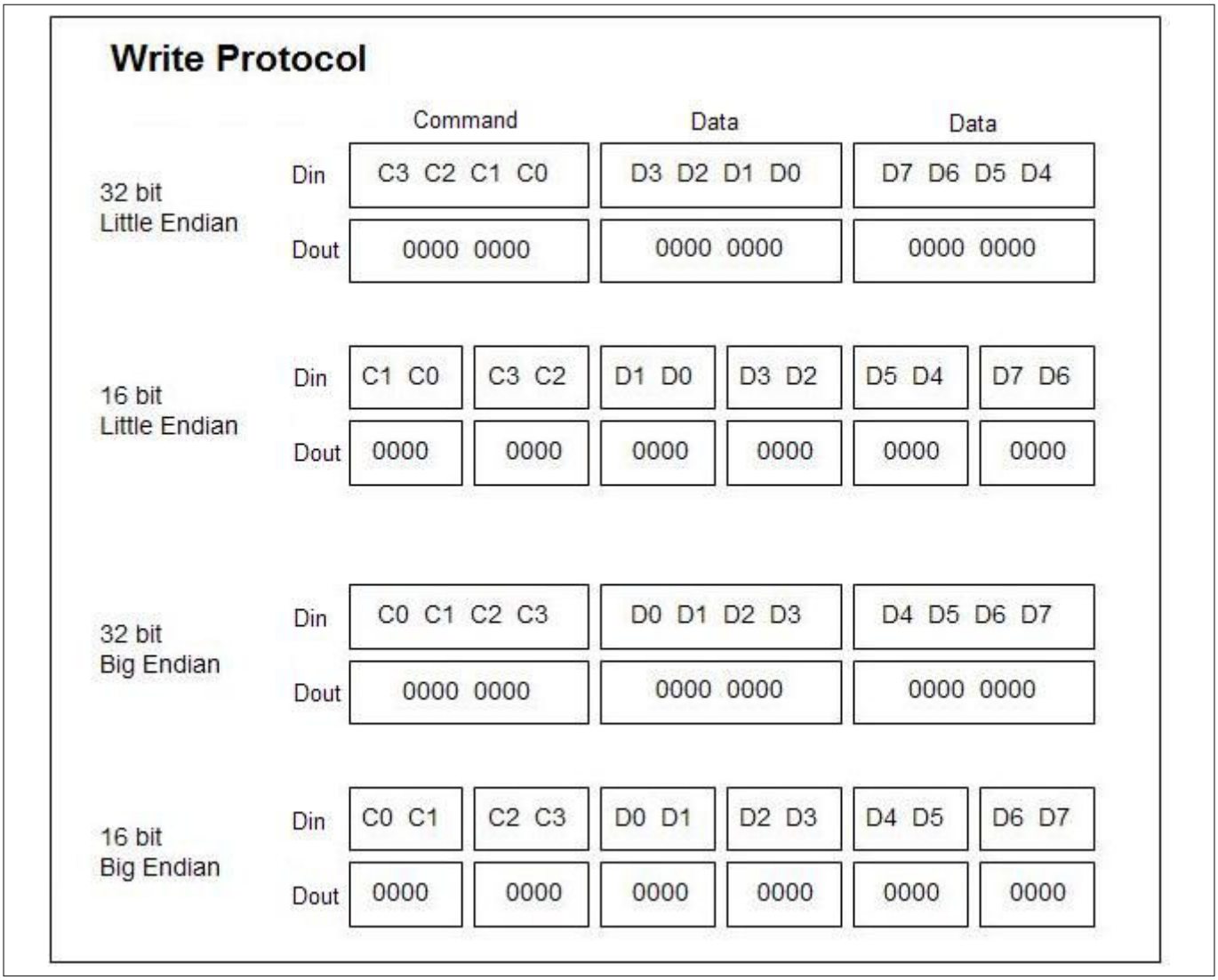


Figure 16 gSPI write protocol

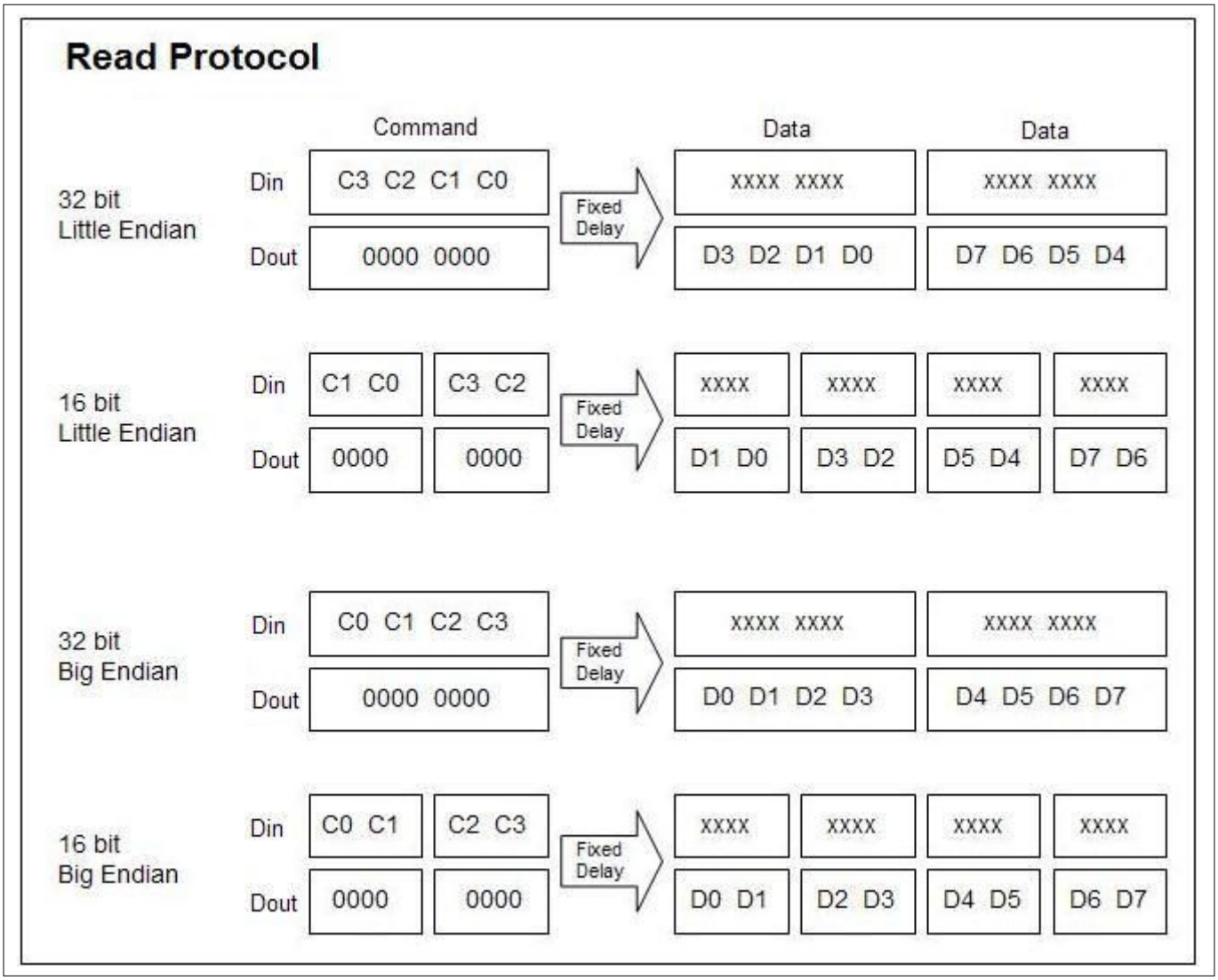


Figure 17 gSPI read protocol

Command structure

The gSPI command structure is 32 bits. The bit positions and definitions are shown in Figure 18.

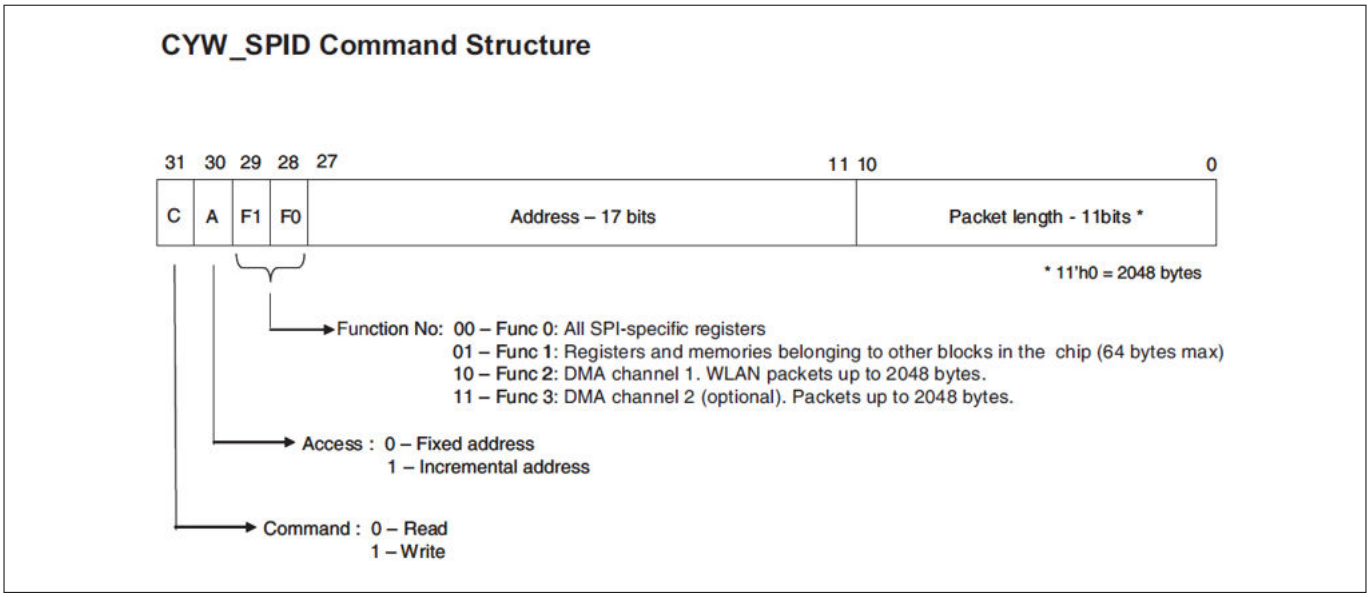


Figure 18 gSPI command structure

Write

The host puts the first bit of the data onto the bus half a clock-cycle before the first active edge following the CS going LOW. The following bits are clocked out on the falling edge of the gSPI clock. The device samples the data on the active edge.

Write/read

The host reads on the rising edge of the clock requiring data from the device to be made available before the first rising-clock edge of the data. The last clock edge of the fixed delay word can be used to represent the first bit of the following data word. This allows data to be ready for the first clock edge without relying on asynchronous delays.

Read

The read command always follows a separate write to set up the WLAN device for a read. This command differs from the write/read command in the following respects: a) chip selects go HIGH between the command/address and the data, and b) the time interval between the command/address is not fixed.

Status

The gSPI interface supports status notification to the host after a read/write transaction. This status notification provides information about packet errors, protocol errors, available packets in the RX queue, and so on. The status information helps reduce the number of interrupts to the host. The status-reporting feature can be switched off using a register bit, without any timing overhead. The gSPI bus timing for read/write transactions with and without status notification are as shown in Figure 19 below and Figure 20. See Table 11 for information on status-field details.

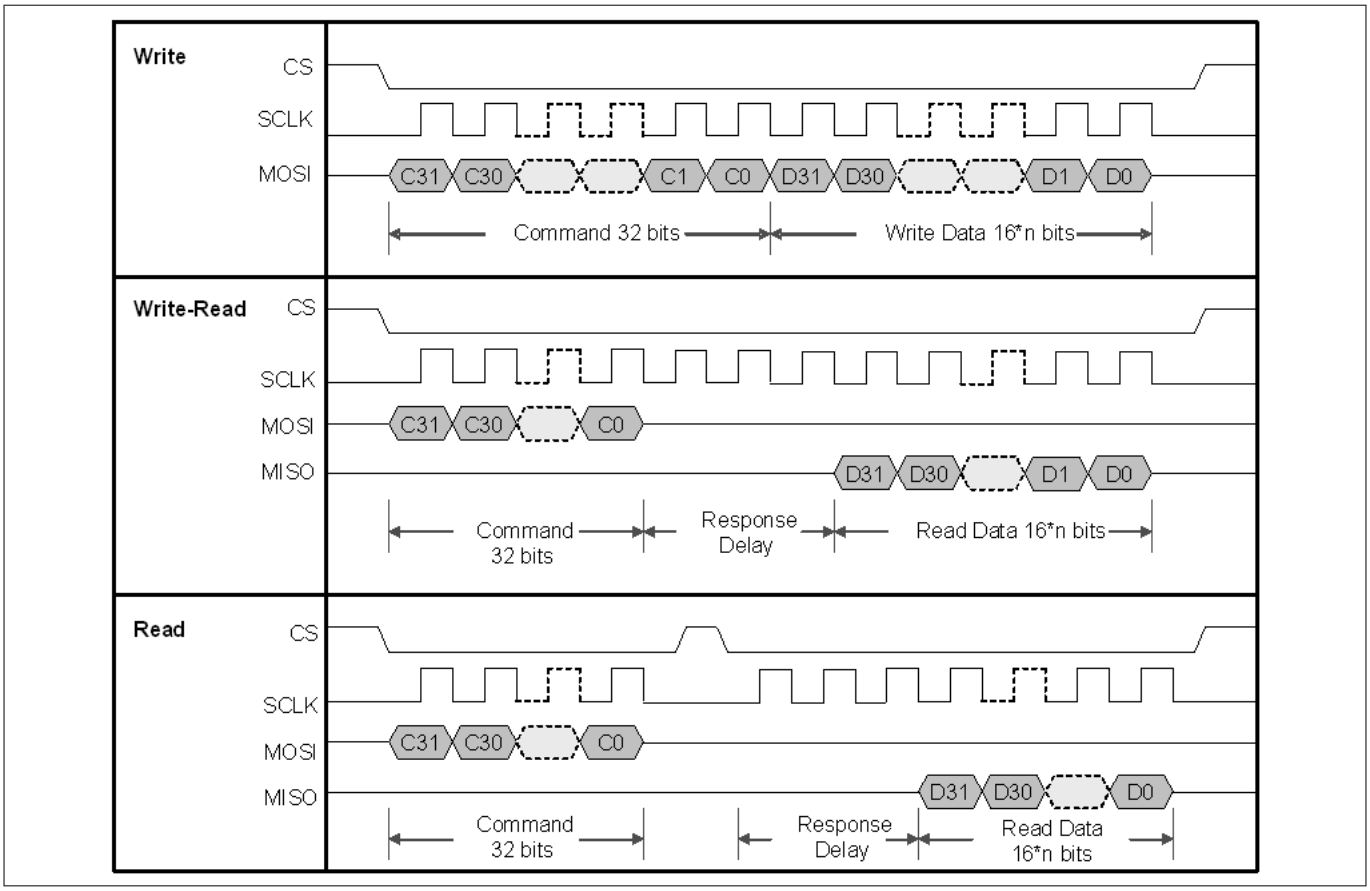


Figure 19 gSPI signal timing without status

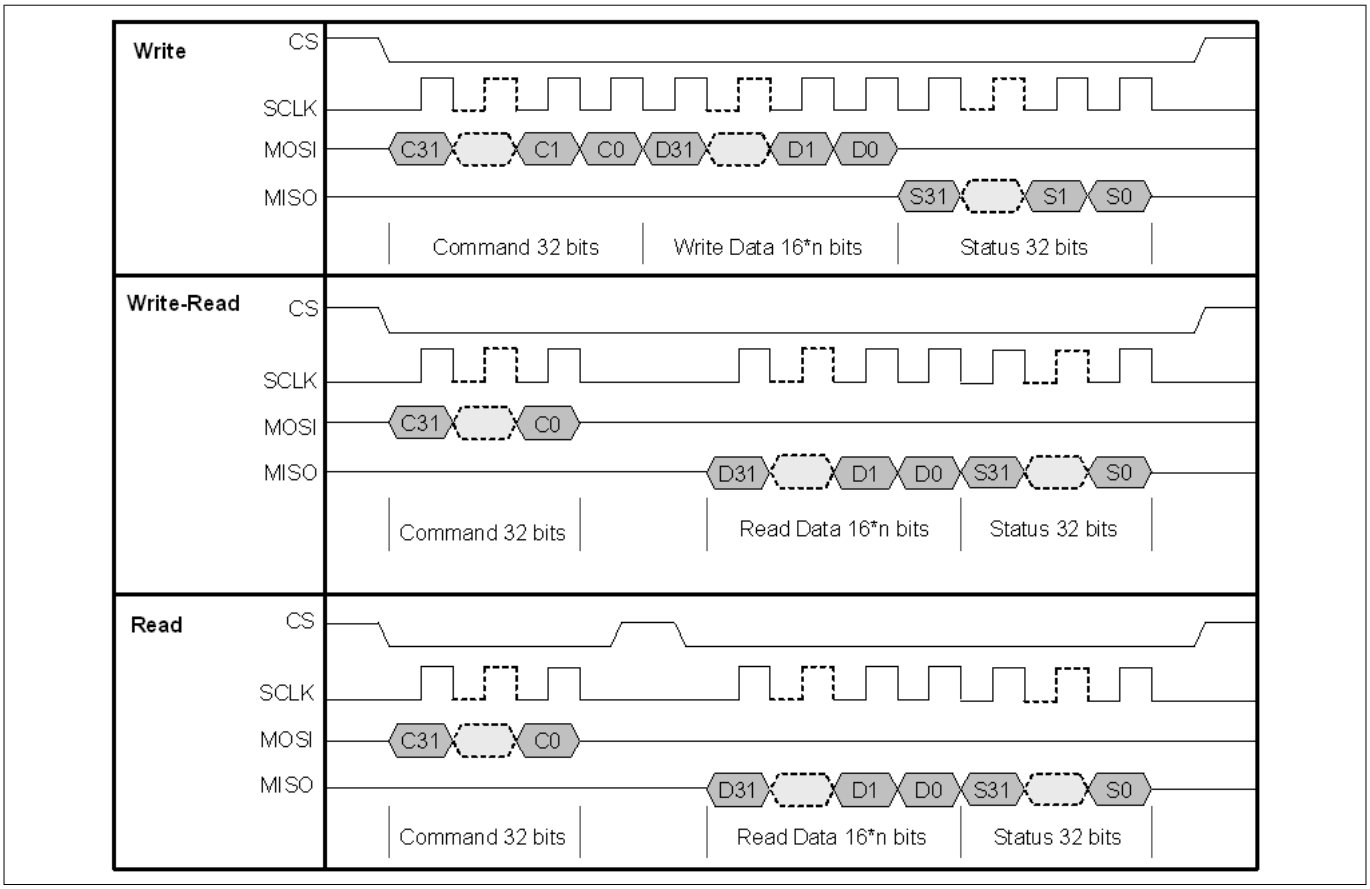


Figure 20 gSPI signal timing with status (response delay = 0)

Table 11 gSPI Status field details

Bit	Name	Description
0	Data not available	The requested read data is not available
1	Underflow	FIFO underflow occurred due to current (F2, F3) read command
2	Overflow	FIFO overflow occurred due to current (F1, F2, F3) write command
3	F2 interrupt	F2 channel interrupt
5	F2 RX ready	F2 FIFO is ready to receive data (FIFO empty)
7	Reserved	–
8	F2 packet available	Packet is available/ready in F2 TX FIFO
9:19	F2 packet length	Length of packet available in F2 FIFO

9 WLAN MAC and PHY

9.1 IEEE 802.11ax MAC

The CYW5591x WLAN MAC is designed to support for low-power consumption. It does so without compromising the Bluetooth® coexistence policies, thereby enabling optimal performance over both networks. In addition, several power saving modes have been implemented that allow the MAC to consume very little power while maintaining network-wide timing synchronization.

CYW5591x WLAN medium access controller (MAC) supports the following features:

- IEEE 802.11a/b/g/n/ac/ax
- 1x1 11ax-20 MHz
- 11ax STA support
- STA + SoftAP (SCC) STA + SoftAP (MCC)
- Long Guard Intervals, Operating Mode Indicator (OMI), Long OFDM Symbols, Dual-Carrier Modulation
- MBO, OCE (11k/r/v/w/as)
- Transmission and reception of HE-SU and HE-ER-SU PPDU
- Reception of HE-MU PPDU-OFDMA/MU-MIMO Frame
- Transmission of HE-TB PPDU (Uplink MU OFDMA)
- Trigger frame reception
- QoS null transmission in triggered/non-triggered data
- MU RTS and MU BA reception
- Dual NAV
- Individual target wake time (TWT) and broadcast TWT
- Transmission and reception of AMPDUs/AMSDUs
- Support for power management schemes, including WMM power-save
- Support for all ACK and Block-ACK policies as per standard
- Interframe space timing support, including RIFS
- Support for RTS/CTS and CTS-to-nowhere frame sequences for protecting frame exchanges
- WMM/802.11e/802.11w support
- Timing synchronization function (TSF), network allocation vector (NAV) maintenance, and target beacon transmission time (TBTT) generation in hardware and capturing the TSF timer on an external time synchronization pulse
- Hardware offload for cipher suites/encryption type AES(WPA2) support for WPA3-SAE and key management
- Support for MBSS
- Support for coexistence with Bluetooth® and other external radios
- RTS-CTS based BW signaling mechanism support
- Support for roaming based of RSSI threshold

9.2 IEEE 802.11ax/ac PHY

CYW5591x WLAN PHY supports features specified in the IEEE 802.11-2016 standard and amended 802.11ax specification. The PHY has been designed to work in the presence of interference, radio nonlinearity, and various other impairments. It incorporates optimized implementations of the filters, FFT, and Viterbi decoder algorithms. The PHY has been designed for sharing an antenna between WLAN and Bluetooth®.

Key PHY features include:

- 1 stream HE-11ax STA support (based on draft 2.0 11ax)
- Supports 20 MHz channels
- Supports 11ax MCS0-11
- Supports transmission and reception of HE-SU and HE-ER-SU PPDU
- Supports reception of HE-MU PPDU
  - Downlink MU OFDMA
  - Downlink MU-MIMO on full band (non-OFDMA RU)
- Supports transmission of HE-TB PPDU (uplink MU OFDMA)
- Supports dual carrier modulation (DCM)
- Support for all mandatory GI-LTF combinations
- 20-MHz only STA support
- Supports responding to HE-sounding frame with up to four spatial streams
- Supports MU-MIMO STA capability with full band RU - Required to allow AP (with up to 4 antenna) to use MU-MIMO when transmitting to the STA, improving network efficiency
- Supports legacy 802.11a/b/g/n/ac
- Hardware based adjacent channel detection (HWACI) for improved receiver performance under congested environment
- Narrow band detection to improve RX sensitivity in presence of spurs or narrow band signal
- 11ax soft-AP mode with capability to receive single user allocation TB-PPDU frames
- Supports 5G DFS slave mode

9.3 External coexistence interface

An external handshake interface is available to enable signaling between the device and an external co-located wireless device, such as LTE to manage wireless medium sharing for optimal performance. Figure 21 shows the LTE coexistence interface (including UART). See Table 16 for further details on multiplexed signals, such as the GPIO pins.

The CYW5591x family implements highly sophisticated enhanced collaborative coexistence hardware mechanisms and algorithms to enable WLAN and Bluetooth® to operate simultaneously. A collaborative coexistence interface between WLAN and Bluetooth® is implemented according to IEEE 802.15.2 Packet Traffic Arbitration (PTA) and communicated through Infineon's serial enhanced coexistence interface (SECI) or global coexistence interface (GCI).

The SECI augments PTA signaling by enabling an exchange of additional information required for implementing more advanced collaborative coexistence methods.

Table 12 3-Wire GPIO mode (External radio - BT/BLE/Zigbee)

Coexistence signal	Type	Comment
RF_ACTIV	Input	Request for the medium
PRIORITY	Input	Priority of the medium
TXCONF	Output	Grant/deny

Table 13 3-Wire GPIO mode (External LTE)

Coexistence signal	Type	Comment
FRAME SYNC	Input	Frame sync pulse every 10 ms frame boundary
LTE TX	Input	Advanced notice of upcoming LTE TX activity
BT/WLAN PRIORITY	Output	Indication of BT or WLAN priority. LTE to back off transmission for the duration of this event.

Table 14 2-Wire WCI2/SECI mode (External radios like LTE/Infineon BT)

Coexistence signal	Type	Comment
WECI2/SECI RX	Input	Serial input. Proprietary serial messages in SECI mode, and it follows BTSIG signaling in WCI2 mode.
WCI2/SECI TX	Output	Serial output. Proprietary serial messages in SECI mode, and it follows BTSIG signaling in WCI2 mode.

***Note**: The LTECX chip has hardware interface capability.*

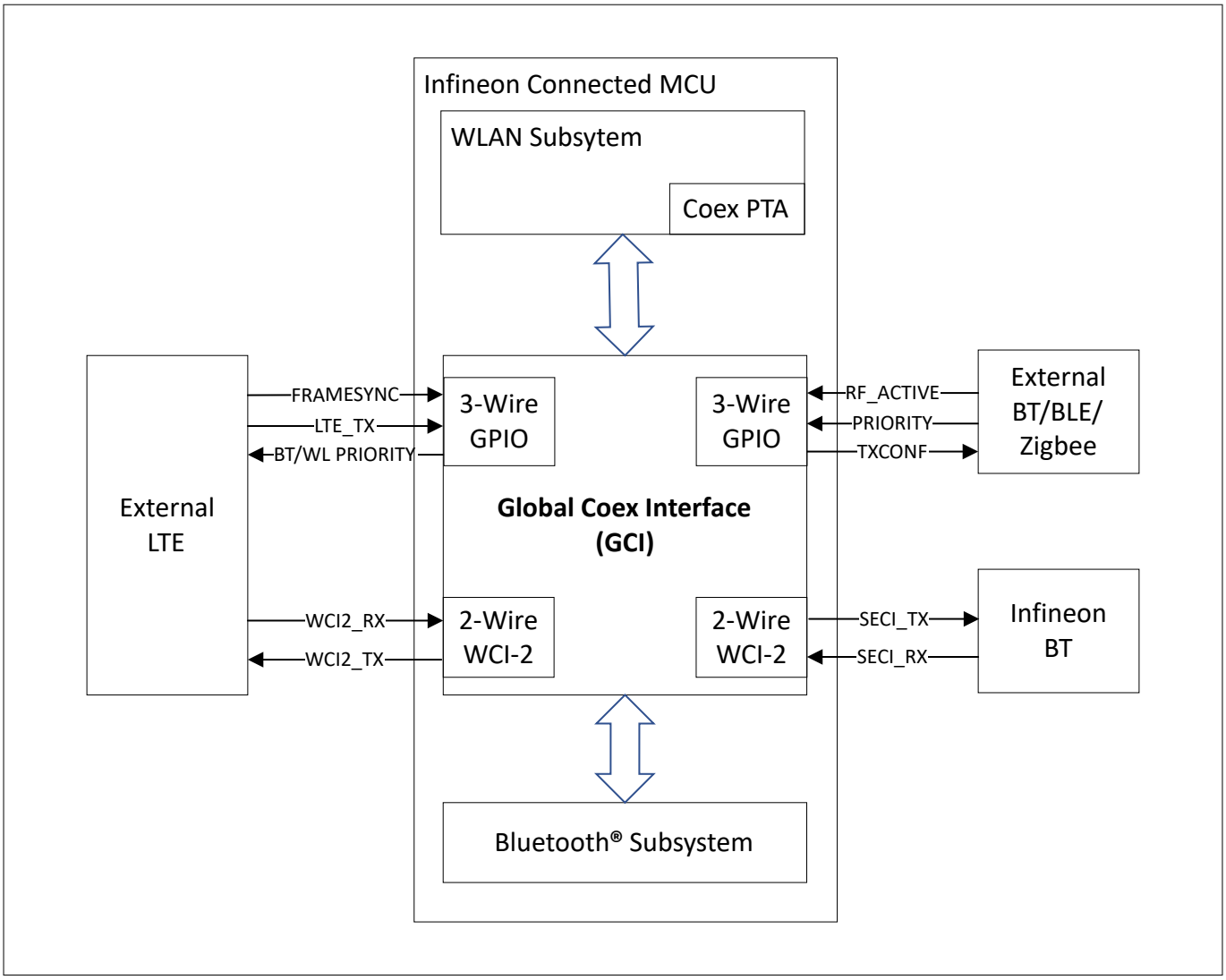


Figure 21 Multipoint global coexistence interface

10 Pinout and signal descriptions

10.1 CYW55913 WLBGA package ball map

	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	
10	WRF_RFIN_5G	WRF_RX5G_GND	WRF_LOGEN_GND	WRF_SYNTH_VDD_1P12	WRF_VCO_GND	NC1	RFSW_CTRL7	VDDIO_RFSW	GPIO_0	GPIO_4	VDDOUT_RF3P3	WLLDO_VDDBAT	BTLDO_VDDBAT	ASR_VDDBAT	ASR_VLX	10
9	WRF_PAOUT_5G	WRF_TX5G_GND	WRF_GPAIO_TSSI2G_OUT				RFSW_CTRL6	VSSC	GPIO_2	GPIO_6	PMU_VDD1P8	VDDOUT_PA3P3	VDDOUT_BT3P3	VDDOUT_CLDO	PVSSA	9
8	WRF_PA_GND	WRF_PA_VDD_3P3	WRF_TX_GND	WRF_SYNTH_VDD_3P3	WRF_SYNTH_GND	NC2	RFSW_CTRL5	VDDC	GPIO_3	GPIO_5	MIC_P	PMU_AVSS	REG_ON	ASR_VDD1P12	REG_ON	8
7	WRF_PAOUT_2G	WRF_TX2G_GND	WRF_LO_GND	WRF_PMU_VDD_3P3	WRF_AFE_VDD_1P12	RFSW_CTRL4	LHL_XTALI	LHL_XTALO	BT_UART_RTS_N	BT_UART_TXD	VSSC	BT_GPIO_5	SDIO_DATA_2	SDIO_DATA_1	SDIO_CLK	7
6	WRF_RFIN_2G	WRF_RX2G_GND	WRF_TSSI5G_OUT	WRF_PMU_GND	WRF_PMU_TX_VDD_1P12	RFSW_CTRL3	VDDC	LHL_GPIO_2	BT_UART_RXD	BT_UART_CTS_N	BT_GPIO_6	VDDIO	SDIO_DATA_3	SDIO_DATA_0	SDIO_CMD	6
5	BTRF_RF_OP	BTRF_VSS	BTRF_IF_VSS	WRF_VDD_1P8	WRF_AFE_LPF_TIA_GND	RFSW_CTRL2	LPO_IN_OUT	LHL_GPIO_3	AVDD_BBPLL	BT_GPIO_4	BT_GPIO_3	VDDC	SMIF_SPHB_DQ3	SMIF_SPHB_DQ2	SMIF_SPHB_CK	5
4	BTRF_VSS	BTRF_TEST	BTRF_PLL_VSS	BTRF_RX_DVSS	RFSW_CTRL1	RFSW_CTRL0	VSSC	LHL_GPIO_4	VSSC	BT_VDDO	BT_GPIO_2	TDM1_DI	SMIF_SPHB_CS0_N	SMIF_SPHB_DQ1	SMIF_SPHB_DQ0	4
3	BTRF_13DBM_OP	BTRF_VCO_VSS		BTRF_LDO_VDD_1P12		JTAG_SEL	BT_DEV_WAKE	LHL_GPIO_5	SMIF_SPHB_CS1_N	TDM1_DO	TDM1_SCK	TDM1_WS	BT_GPIO_17	BT_GPIO_16	BT_GPIO_7	3
2		BTRF_PA_VSS	BTRF_TX_VSS	BTRF_TX_DVSS	XTAL_GND	VDD_XTAL	WL_DEV_WAKE	VDDC	LHL_GPIO_8	BT_HOST_WAKE	TDM1_MCK	TDM2_DI	VSSC	VDDC	TDM2_WS	2
1	BTRF_20DBM_OP	BTRF_PA_VSS	BTRF_PA_VDD_3P3	BTRF_TXIF_VSS	XTAL_XON	XTAL_XOP		LHL_GPIO_9	LHL_GPIO_6	BT_GPIO_0	DMIC_DQ	DMIC_CK	TDM2_DO	TDM2_MCK	TDM2_SCK	1
	R	P	N	M	L	K	J	H	G	F	E	D	C	B	A	

Figure 22 WLBGA package ball map

10.2 Pin function description

Table 15 Pin function description

Ball #	Ball name	Type	Description
R10	WRF_RFIN_5G	I	WLAN Radio 5/6 GHz Receiver input
R9	WRF_PAOUT_5G	O	WLAN Radio 5/6 GHz PA output
R8	WRF_PA_GND	GND	WLAN PA ground
R7	WRF_PAOUT_2G	O	WLAN Radio 2.4 GHz PA output
R6	WRF_RFIN_2G	I	WLAN Radio 2.4 GHz Receiver input
P10	WRF_RX5G_GND	GND	WLAN Radio RX 5 GHz Ground
P9	WRF_TX5G_GND		WLAN Radio TX 5 GHz Ground
P8	WRF_PA_VDD_3P3	PWR	WLAN Radio 3.3 V PA Supply
P7	WRF_TX2G_GND	GND	WLAN Radio TX 5 GHz Ground
P6	WRF_RX2G_GND		WLAN Radio RX 2 GHz Ground
N10	WRF_LOGEN_GND		WLAN Radio Logen Ground
N9	WRF_GPAIO_TSSI2G_OUT	O	WLAN Radio 2.4 GHz TSSI
N8	WRF_TX_GND	GND	WLAN Radio Logen Ground
N7	WRF_LO_GND		WLAN Radio LO Ground

(table continues...)

Table 15 (continued) Pin function description

Ball #	Ball name	Type	Description
N6	WRF_TSSI5G_OUT	O	WLAN Radio 5/6 GHz TSSI
M10	WRF_SYNTH_VDD_1P12	PWR	WLAN Radio 1.12 V supply
M8	WRF_SYNTH_VDD_3P3		WLAN Radio 3.3 V supply
M7	WRF_PMU_VDD_3P3		WLAN Radio 3.3 V supply
M6	WRF_PMU_GND	GND	WLAN PMU Ground
M5	WRF_VDD_1P8	PWR	WLAN Radio 1.8 V supply
L10	WRF_VCO_GND	GND	WLAN Radio VCO Ground
L8	WRF_SYNTH_GND		WLAN Radio SYNTH Ground
L7	WRF_AFE_VDD_1P12	PWR	WLAN Radio 1.12 V supply
L6	WRF_PMU_TX_VDD_1P12		WLAN PMU TX 1.12 V supply
L5	WRF_AFE_LPF_TIA_GND	GND	WLAN Radio AFE Ground
K2	VDD_XTAL	PWR	Xtal oscillator 1.0 V supply
K1	XTAL_XOP	I	Xtal oscillator Input
J7	LHL_XTALI		32.768 kHz crystal oscillator input
L2	XTAL_GND	GND	XTAL oscillator ground
L1	XTAL_XON	O	XTAL oscillator output
H7	LHL_XTALO		32.768 kHz crystal oscillator output
R5	BTRF_RF_OP		Low-power TX output/dLNA RX input
R4	BTRF_VSS	GND	Bluetooth® Radio ground
R3	BTRF_13DBM_OP	O	Bluetooth® Radio (13 dBm) output
R1	BTRF_20DBM_OP	O	Bluetooth® Radio (+19 dBm) output
P5	BTRF_VSS	GND	Bluetooth® Radio ground
P4	BTRF_TEST	I/O	Bluetooth® Radio test input/ output pin
P3	BTRF_VCO_VSS	GND	Bluetooth® Radio VCO Ground
P2	BTRF_PA_VSS		Bluetooth® Radio PA Ground
P1	BTRF_PA_VSS		
N5	BTRF_IF_VSS		Bluetooth® Radio IF Ground
N4	BTRF_PLL_VSS		Bluetooth® Radio PLL Ground
N2	BTRF_TX_VSS		Bluetooth® Radio TX Ground

(table continues...)

Table 15 (continued) Pin function description

Ball #	Ball name	Type	Description
N1	BTRF_PA_VDD_3P3	PWR	Bluetooth® Radio PA 3.3 V input supply
M4	BTRF_RX_DVSS	GND	Bluetooth® Radio RX DVSS
M3	BTRF_LDO_VDD_1P12	PWR	Bluetooth® Radio 1.12 V input supply
M2	BTRF_TX_DVSS	GND	Bluetooth® Radio TX DVSS
M1	BTRF_TXIF_VSS		Bluetooth® Radio TXIF DVSS
C8 A8	REG_ON	I	Used by the PMU to power up or power down the internal CYW5591x regulators . When deasserted, this pin holds the chip in reset. This pin has an internal 50 kΩ pull-down resistor that is auto enabled and disabled upon recognizing high on this pin.
G7	BT_UART_RTS_N	O	UART request-to-send. Active-low request-to-send signal for the BT UART interface. Bluetooth® LED control pin.
G6	BT_UART_RXD	I	UART serial input. Serial data input for the BT UART interface.
F7	BT_UART_TXD	O	UART serial output. Serial data output for the BT UART interface.
F6	BT_UART_CTS_N	I	UART clear-to-send. Active-low clear-to-send signal for the BT UART interface.
F4	BT_VDDO	PWR	1.8-V IO supply for Bluetooth® GPIOs
F3	TDM1_DO	I/O	Bluetooth® TDM1 Interface Data Out
F2	BT_HOST_WAKE		Bluetooth® HOST WAKE
L4	RFSW_CTRL1	O	Programmable RF switch control lines. The control lines are programmable via the driver and NVRAM file.
K7	RFSW_CTRL4		
K6	RFSW_CTRL3		
K5	RFSW_CTRL2		
K4	RFSW_CTRL0		
J10	RFSW_CTRL7		

(table continues...)

Table 15 (continued) Pin function description

Ball #	Ball name	Type	Description
J9	RFSW_CTRL6		
J8	RFSW_CTRL5		
F5	BT_GPIO_4	I/O	Bluetooth® general purpose I/O
A3	BT_GPIO_7		
E6	BT_GPIO_6		
E5	BT_GPIO_3		
E4	BT_GPIO_2		
F1	BT_GPIO_0		
D7	BT_GPIO_5		
C3	BT_GPIO_17		
B3	BT_GPIO_16		
H6	LHL_GPIO_2		Miscellaneous general purpose I/O
H5	LHL_GPIO_3		
H4	LHL_GPIO_4		
H3	LHL_GPIO_5		
G2	LHL_GPIO_8		
G1	LHL_GPIO_6		
H1	LHL_GPIO_9		
G10	GPIO_0		WLAN general purpose I/O
G9	GPIO_2		
G8	GPIO_3		
F10	GPIO_4		
F9	GPIO_6		
F8	GPIO_5		
C7	SDIO_DATA_2		SDIO data line 2
C6	SDIO_DATA_3		SDIO data line 3
B7	SDIO_DATA_1		SDIO data line 1
B6	SDIO_DATA_0		SDIO data line 0
A7	SDIO_CLK	I	SDIO clock input
A6	SDIO_CMD	I/O	SDIO command line
A2	TDM2_WS		TDM2 Interface Word Select
A1	TDM2_SCK		TDM2 Interface Slave Clock
E3	TDM1_SCK		TDM1 Interface Slave Clock

(table continues...)

Table 15 (continued) Pin function description

Ball #	Ball name	Type	Description
E2	TDM1_MCK		TDM1 Interface Master Clock
D4	TDM1_DI		TDM1 Interface Data In
D3	TDM1_WS		TDM1 Interface Word Select
D2	TDM2_DI		TDM2 Interface Data In
C1	TDM2_DO		TDM2 Interface Data Out
B1	TDM2_MCK		TDM2 Interface Master Clock
C5	SMIF_SPHB_DQ3		SMIF data line 3
B5	SMIF_SPHB_DQ2		SMIF data line 2
B4	SMIF_SPHB_DQ1	I/O	SMIF data line 1
A4	SMIF_SPHB_DQ0		SMIF data line 0
C4	SMIF_SPHB_CS0_N	O	SMIF chip select0 active-low output
G3	SMIF_SPHB_CS1_N		SMIF chip select1 active-low output
A5	SMIF_SPHB_CK		SMIF clock output
K10	NC1	–	No Connect
K8	NC2		
D6	VDDIO	PWR	1.8 V IO supply for WLAN GPIOs
H8	VDDC		0.9 V digital core supply
H2	VDDC		
B2	VDDC		
D5	VDDC		
J6	VDDC		
C10	BTLDO_VDDBAT		Battery supply Input for Bluetooth® PA LDO
C9	VDDOUT_BT3P3		3.3 V output to supply Bluetooth® PA
B10	ASR_VDDBAT		Battery supply input for ASR power stage
B9	VDDOUT_CLDO	O	Output of CLDO
B8	ASR_VDD1P12	I	Sense or feedback input of ASR power stage
D10	WLLDO_VDDBAT	PWR	Battery supply input for WLAN PA LDO and RF LDO
D9	VDDOUT_PA3P3		3.3 V output to supply WLAN PA
D8	PMU_AVSS	GND	PMU analog ground

(table continues...)

Table 15 (continued) Pin function description

Ball #	Ball name	Type	Description
A10	ASR_VLX	O	ASR power stage output to inductor
A9	PVSSA	GND	Ground input of ASR power stage
K3	JTAG_SEL	I	JTAG select input: Pull high to select the Test Access Port and connect this pin to ground to enable Arm® Debug Access Port.
J5	LPO_IN_OUT	I/O	Based on configuration it can be either 1. As an external 32 KHz clock source input 2. As a 32 KHz clock output if XTAL is connected (XTAL_IN, XTAL_OUT). 3. LHL_GPIO_10 similar to other LHL GPIOs
J3	BT_DEV_WAKE	I/O	Bluetooth® DEVICE WAKE
J2	WL_DEV_WAKE		WLAN DEVICE WAKE
H10	VDDIO_RFSW	PWR	IO supply for RF switch control pads
H9	VSSC	GND	Core ground for WLAN and Bluetooth®
G4			
E7			
J4			
C2			
G5	AVDD_BBPLL	PWR	Baseband PLL 0.9 V supply
E10	VDDOUT_RF3P3		3.3 V output to supply WLAN radio
E9	PMU_VDD1P8		1.8 V PMU supply input
E8	MIC_P	I	ADC microphone positive input
E1	DMIC_DQ	I/O	Digital mic data
D1	DMIC_CK	I/O	Digital mic clock

10.3 GPIO strapping options

Table 16 GPIO strap pins

Pad name	Default pull during strapping	All packages
sdiod_data[2]	1	1 = SDIOD, 0 = gSPI

10.4 GPIO signal functions

***Notes**:*

1. *The notation for a signal is of the form IPName[x].signal_name_[u]. Eg: SCB0-SPI_SEL0, SCB denotes the IPName, SCB"0" denotes the instance of the IP, SPI_SEL0 is the signal name*
2. *TCPWM IP alone represented in a different way TCPWM_Signal name_[u][v]. Eg: TCPWM_OUT_12, "OUT" denotes the signal name,[u]=1 denotes the TCPWM group 1 is 16-bit and 2 is 32-bit groups. [v]=2 denotes the counter instance in a TCPWM group. There two 32-bit and Seven 16-bit counter in TCPWM group 1 and 2 Respectively.*
3. *You might see same signal name appearing in different cells, this means they are copies of the signal. Signal copies are provided to allow flexibility in routing and to maximize use of on-chip resources.*
4. *If SDIO is the strap settings, then all SDIO lines except SDIO_CLK will be at static pull-up of 50 KΩ and there is no pull up/down on SDIO_CLK.*
5. *On UART lines, static pull-up on all four lines.*
6. *On BT_HOST_WAKE pull-down of 50 KΩ*

Table 17 GPIO signal functions

PIN/PAD NAME	Function Sel															
	FUNC #0	FUNC #1[1)]	FUNC #2	FUNC #3	FUNC #4	FUNC #5	FUNC #6	FUNC #7	FUNC #8	FUNC #9	FUNC #10	FUNC #11	FUNC #12	FUNC #13	FUNC #14	FUNC #15
BT GPIO alternative signal functions																
Peripherals	—	GPIO	—	Audio Interfaces		SCB0			SCB1			SCB2			TCPWM	
Functions	—	GPIO	UART/ LPCOMP	Audio Codec	PDM DMIC	I2C	SPI	UART	I2C	SPI	UART	I2C	SPI	UART	TCPWM	TCPWM_ECO
BT_UART_CTS_N	—	FUNC_A_GPIO_1	BT_UART_CTS_N	—	—	—	SCB0-SPI_SEL0	SCB0-UART_CTS	—	—	—	—	—	—	—	—
BT_UART_RTS_N	—	FUNC_A_GPIO_0	BT_UART_RTS_N	—	—	—	SCB0-SPI_CLK	SCB0-UART_RTS	—	—	—	—	—	—	—	—
BT_UART_RXD	—	FUNC_GPIO_5	BT_UART_RXD	—	—	—	SCB0-SPI_MOSI	SCB0-UART_RXD	—	—	—	—	—	—	—	—
BT_UART_TXD	—	FUNC_GPIO_4	BT_UART_TXD	—	—	—	SCB0-SPI_MISO	SCB0-UART_TXD	—	—	—	—	—	—	—	—
BT_GPIO_0	—	FUNC_GPIO_0	—	—	—	—	—	—	—	—	—	—	SCB2-SPI_SEL3	—	TCPWM_TR_ALL_5	—
BT_HOST_WAKE/ BT_GPIO_1	—	FUNC_GPIO_1	BT_HOST_WAKE	—	—	—	—	—	—	—	—	—		—	TCPWM_TR_ALL_6	—

(table continues...)

Table 17 (continued) GPIO signal functions

PIN/PAD NAME	Function Sel															
	FUNC #0	FUNC #1[1)]	FUNC #2	FUNC #3	FUNC #4	FUNC #5	FUNC #6	FUNC #7	FUNC #8	FUNC #9	FUNC #10	FUNC #11	FUNC #12	FUNC #13	FUNC #14	FUNC #15
BT_GPIO_2	—	FUNC_GPIO_2	—	—	—	—	SCB0-SPI_SEL3	—	SCB1-SDA	SCB1-SPI_MISO	SCB1-UART_RXD	—	—	—	TCPWM_TR_ALL_7	—
BT_GPIO_3	—	FUNC_GPIO_3	—	—	—	—		—	SCB1-SCL	SCB1-SPI_MOSI	SCB1-UART_TXD	—	—	—	TCPWM_TR_ALL_8	—
BT_GPIO_4	—	FUNC_GPIO_4	—	—	—	SCB0-SDA	SCB0-SPI_SEL2	—	—	SCB1-SPI_SEL1	SCB1-UART_CTS	—	—	—	TCPWM_OUT_11	—
BT_GPIO_5	—	FUNC_GPIO_5	—	—	—	SCB0-SCL	SCB0-SPI_SEL1	—	—		SCB1-UART_RTS	—	—	—	TCPWM_OUT_12	—
BT_GPIO_6	—	FUNC_GPIO_6	—	—	—	—	—	—	—	SCB1-SPI_SEL3	—	SCB2-SDA	—	—	TCPWM_OUT_21	—
BT_GPIO_7	—	FUNC_GPIO_7	—	—	—	—	—	—	—	SCB1-SPI_SEL2	—	SCB2-SCL	—	—	TCPWM_OUT_22	—
BT_GPIO_16	—	FUNC_A_GPIO_0	—	—	—	—	—	—	SCB1-SCL	SCB1-SPI_SEL0	—	—	—	—	TCPWM_OUT_12 / TCPWM_COMP_OUT_12	—

(table continues...)

Table 17 (continued) GPIO signal functions

PIN/PAD NAME	Function Sel															
	FUNC #0	FUNC #1[1)]	FUNC #2	FUNC #3	FUNC #4	FUNC #5	FUNC #6	FUNC #7	FUNC #8	FUNC #9	FUNC #10	FUNC #11	FUNC #12	FUNC #13	FUNC #14	FUNC #15
BT_GPIO_17	—	FUNC_A_GPIO_1	—	—	—	—	—	—	SCB1-SDA	SCB1-SPI_CLK	—	—	—	—	TCPWM_OUT_11 / TCPWM_COMP_OUT_21	—
TDM1_WS	—	FUNC_A_GPIO_2	—	TDM1_WS	—	—	—	—	—	—	—	—	—	—	—	TCPWM_OUT_23
TDM1_SCK	—	FUNC_A_GPIO_3	—	TDM1_SCK	—	—	—	—	—	—	—	—	—	—	—	TCPWM_OUT_24
TDM1_MCK	—	FUNC_A_GPIO_4	—	TDM1_MCK	—	—	SCB0-SPI_SEL2	—	—	—	—	—	—	—	—	TCPWM_OUT_25
TDM1_DI	—	FUNC_A_GPIO_5	—	TDM1_DI	—	—	—	—	—	SCB1-SPI_SEL3	—	—	—	—	—	TCPWM_OUT_26
TDM1_DO	—	FUNC_A_GPIO_6	—	TDM1_DO	—	—	—	—	—	SCB1-SPI_SEL2	—	—	—	—	—	TCPWM_OUT_27
TDM2_WS	—	FUNC_A_GPIO_7	—	TDM2_WS	—	—	—	—	—	—	—	—	—	—	—	—

(table continues...)

Table 17 (continued) GPIO signal functions

PIN/PAD NAME	Function Sel															
	FUNC #0	FUNC #1[1)]	FUNC #2	FUNC #3	FUNC #4	FUNC #5	FUNC #6	FUNC #7	FUNC #8	FUNC #9	FUNC #10	FUNC #11	FUNC #12	FUNC #13	FUNC #14	FUNC #15
TDM2_SCK	—	FUNC_A_GPIO_0	—	TDM2_SCK	—	—	—	—		—	—	SCB2-SDA	SCB2-SPI_SEL1	—	—	—
TDM2_MCK	—	FUNC_A_GPIO_7/ FUNC_A_GPIO_1	—	TDM2_MCK	—	—	SCB0-SPI_SEL1	—	—	—	—	SCB2-SCL	SCB2-SPI_SEL2	—	—	—
TDM2_DI	—	FUNC_GPIO_6	—	TDM2_DI	—	—		—	—	—	—	—	SCB2-SPI_MOSI	—	—	—
TDM2_DO	—	FUNC_GPIO_7	—	TDM2_DO	—	—	—	—	—	—	—	—	SCB2-SPI_MISO	—	—	—
DMIC_CK	—	FUNC_GPIO_0	—	—	DMIC_CK	—	—	—	—	—	—	—	SCB2-SPI_CLK	—	—	—
DMIC_DQ	—	FUNC_GPIO_1	—	—	DMIC_DQ	—	—	—	—	—	—	—	SCB2-SPI_SEL0	—	—	—
WL GPIO																
GPIO_0	—	GCI_GPIO_0	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GPIO_2	ARM DAP TCK	GCI_GPIO_2	—	—	—	—	—	—	—	—	—	—	—	—	—	—

(table continues...)

Table 17 (continued) GPIO signal functions

PIN/PAD NAME	Function Sel															
	FUNC #0	FUNC #1[1)]	FUNC #2	FUNC #3	FUNC #4	FUNC #5	FUNC #6	FUNC #7	FUNC #8	FUNC #9	FUNC #10	FUNC #11	FUNC #12	FUNC #13	FUNC #14	FUNC #15
GPIO_3	ARM DAP TMS	GCI_GPIO_3	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GPIO_4	ARM DAP TDI	GCI_GPIO_4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GPIO_5	ARM DAP TDO	GCI_GPIO_5	—	—	—	—	—	—	—	—	—	—	—	—	—	—
GPIO_6	ARM DAP TRST_L	GCI_GPIO_1	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SDIO_CLK[2)]	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SDIO_CMD	SDIO_CMD	GCI_GPIO_0	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SDIO_DATA_0	SDIO_DATA_0	GCI_GPIO_1	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SDIO_DATA_1	SDIO_DATA_1	GCI_GPIO_2	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SDIO_DATA_2	SDIO_DATA_2	GCI_GPIO_3	—	—	—	—	—	—	—	—	—	—	—	—	—	—

(table continues...)

Table 17 (continued) GPIO signal functions

PIN/PAD NAME	Function Sel															
	FUNC #0	FUNC #1[1)]	FUNC #2	FUNC #3	FUNC #4	FUNC #5	FUNC #6	FUNC #7	FUNC #8	FUNC #9	FUNC #10	FUNC #11	FUNC #12	FUNC #13	FUNC #14	FUNC #15
SDIO_DATA_3	SDIO_DATA_3	GCI_GPIO_4	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RFSW_CTRL6[3)]	RFSW_CTRL	GCI_GPIO_8	—	—	—	—	—	—	—	—	—	—	—	—	—	—
RFSW_CTRL7[3)]	RFSW_CTRL	GCI_GPIO_9	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SMIF_SPHB_CK[2)]	SMIF_CLK	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SMIF_SPHB_DQ3[2)]	SMIF_DATA	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SMIF_SPHB_DQ2 [2)]	SMIF_DATA	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SMIF_SPHB_DQ1 [2)]	SMIF_DATA	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SMIF_SPHB_DQ0 [2)]	SMIF_DATA	—		—	—	—	—	—	—	—	—	—	—	—	—	—
SMIF_SPHB_CS0_N [2)]	SMIF FLASH CS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

(table continues...)

Table 17 (continued) GPIO signal functions

PIN/PAD NAME	Function Sel															
	FUNC #0	FUNC #1[1)]	FUNC #2	FUNC #3	FUNC #4	FUNC #5	FUNC #6	FUNC #7	FUNC #8	FUNC #9	FUNC #10	FUNC #11	FUNC #12	FUNC #13	FUNC #14	FUNC #15
SMIF_SPHB_CS1_N[2)]	SMIF PSRAM CS	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
LHL GPIO																
WL_DEV_WAKE/ LHL_GPIO_0	—	FUNC_LHL_IO_0	—	—	—	—	—	—	—	—	—	—	—	—	—	—
BT_DEV_WAKE/ LHL_GPIO_1	—	FUNC_LHL_IO_1	—	—	—	—	—	—	—	—	—	—	—	—	—	—
LHL_GPIO_2	ADCIn0	FUNC_B_GPIO[0]	LP_COMP_IN_N	—	—	—	—	—	—	—	SCB1-UART_TXD	—	—	—	TCPWM_TR_ALL_1	—
LHL_GPIO_3	ADCIn1	FUNC_B_GPIO[1]	LP_COMP_IN_N	—	—	—	—	—	—	—	SCB1-UART_RXD	—	—	—	TCPWM_TR_ALL_2	—
LHL_GPIO_4	ADCIn2	FUNC_B_GPIO[2]	LP_COMP_IN_P	—	DMIC_CK		SCB0-SPI_MOSI	—	—		SCB1-UART_CTS	—	—	—	TCPWM_TR_ALL_4	—
LHL_GPIO_5	ADCIn3	FUNC_B_GPIO[3]	LP_COMP_IN_P	—	DMIC_DQ		SCB0-SPI_MISO	—	—	—	SCB1-UART_RTS	—	—	—	TCPWM_TR_ALL_3	—

(table continues...)

Table 17 (continued) GPIO signal functions

PIN/PAD NAME	Function Sel														
	FUNC #0	FUNC #1[1)]	FUNC #2	FUNC #3	FUNC #4	FUNC #5	FUNC #6	FUNC #7	FUNC #8	FUNC #9	FUNC #10	FUNC #11	FUNC #12	FUNC #13	FUNC #14	FUNC #15
LHL_GPIO_6	ADCIn4	FUNC_B_GPIO[4]	LP_COMP_IN_N	—	—	SCB0-SCL	SCB0-SPI_SEL0	—	—	SCB1-SPI_CLK	—	—	—	SCB2-UART_CTS	TCPWM_COMP_OUT_11	TCPWM_OUT_23
LHL_GPIO_8	ADCIn6	FUNC_B_GPIO[6]	LP_COMP_IN_P	—	—	—		—	—	SCB1-SPI_MOSI	—	—	—	SCB2-UART_RXD	TCPWM_COMP_OUT_21	TCPWM_OUT_25
LHL_GPIO_9	ADCIn7	FUNC_B_GPIO[7]	LP_COMP_IN_P	—	—	—		—	—	SCB1-SPI_MISO	—	—	—	SCB2-UART_TXD	TCPWM_COMP_OUT_22	TCPWM_OUT_26

1) The pins that have function in the Func#1/GPIO column can be used as generic GPIOs. Please note that some GPIO functions are shared across pins
2) These pins does not have GPIO Function.
3) RFSW_CTRL6 and RFSW_CTRL7 operate at 3.3V(VDDIO_RFSW) and the remaining GPIOs operate 1.8V(VDDIO)

10.5 I/O states

The following notations are used in Table 18.

- I = Input signal
- O = Output signal
- I/O = Input/output signal
- PU = Pulled up
- PD = Pulled down
- NoPull = Neither pulled up nor pulled down

Where applicable, the default value is shown in bold brackets (for example,**[default value]**)

Table 18 I/O states

Name	I/O	Keeper	Active mode	Low-power state/Sleep (All power present)	Power-down (REG_ON Held Low)	Out-of-reset; Before SW Download (REG_ON High)	(REG_ON = 0) and VDDIOs are present	Power rail
REG_ON[1]	I	N	I: PD Pull-down auto disabled	I: PD Pull-down auto disabled	I: PD (of 50K)	I: PD (of 50K)	I: PD (of 50K)	–
GPIO_0	I/O	Y	I/O: PU, PD, NoPull Programmable [PD]	I/O: PU, PD, NoPull Programmable [PD]	High-Z, NoPull	High-Z, NoPull	High Z, NoPull	VDDIO
GPIO_2			I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I:PU	I:PU	
GPIO_3			I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I:PU	I:PU	
GPIO_4			I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I:PU	I:PU	
GPIO_5			I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: NoPull[13]	I: NoPull	

(table continues...)

Table 18 (continued) I/O states

Name	I/O	Keeper	Active mode	Low-power state/Sleep (All power present)	Power-down (REG_ON Held Low)	Out-of-reset; Before SW Download (REG_ON High)	(REG_ON = 0) and VDDIOs are present	Power rail
GPIO_6			I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, NoPull	I: PU	I:PU	
RF_SW_CTRL_X	O	N	O: NoPull	O: NoPull	High-Z, NoPull	O: NoPull	O: NoPull	VDDIO_RFSW
SMIF_SPHB_CK	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
SMIF_SPHB_DQ3	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
SMIF_SPHB_DQ2	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
SMIF_SPHB_DQ1	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
SMIF_SPHB_DQ0	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO

(table continues...)

Table 18 (continued) I/O states

Name	I/O	Keeper	Active mode	Low-power state/Sleep (All power present)	Power-down (REG_ON Held Low)	Out-of-reset; Before SW Download (REG_ON High)	(REG_ON = 0) and VDDIOs are present	Power rail
SMIF_SPHB_CS0_N	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
SMIF_SPHB_CS1_N	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
BT_GPIO_0	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
BT_GPIO_2	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
BT_GPIO_3	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PU	I: PU	BT_VDDO
BT_GPIO_4	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PU	I: PU	BT_VDDO

(table continues...)

Table 18 (continued) I/O states

Name	I/O	Keeper	Active mode	Low-power state/Sleep (All power present)	Power-down (REG_ON Held Low)	Out-of-reset; Before SW Download (REG_ON High)	(REG_ON = 0) and VDDIOs are present	Power rail
BT_GPIO_5	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PU	I: PU	BT_VDDO
BT_GPIO_6	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
BT_GPIO_7	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
BT_GPIO_16	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
BT_GPIO_17	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
TDM1_WS	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO

(table continues...)

Table 18 (continued) I/O states

Name	I/O	Keeper	Active mode	Low-power state/Sleep (All power present)	Power-down (REG_ON Held Low)	Out-of-reset; Before SW Download (REG_ON High)	(REG_ON = 0) and VDDIOs are present	Power rail
TDM1_SCK	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
TDM1_MCK	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
TDM1_DI	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
TDM1_DO	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
TDM2_WS	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
TDM2_SCK	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO

(table continues...)

Table 18 (continued) I/O states

Name	I/O	Keeper	Active mode	Low-power state/Sleep (All power present)	Power-down (REG_ON Held Low)	Out-of-reset; Before SW Download (REG_ON High)	(REG_ON = 0) and VDDIOs are present	Power rail
TDM2_MCK	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
TDM2_DI	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
TDM2_DO	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
DMIC_CK	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
DMIC_DQ	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO
BT_HOST_WAKE	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: PD	I: PD	BT_VDDO

(table continues...)

Table 18 (continued) I/O states

Name	I/O	Keeper	Active mode	Low-power state/Sleep (All power present)	Power-down (REG_ON Held Low)	Out-of-reset; Before SW Download (REG_ON High)	(REG_ON = 0) and VDDIOs are present	Power rail
BT_DEV_WAKE	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: No Pull	I: No Pull	VDDIO
WL_DEV_WAKE	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: No Pull	I: No Pull	VDDIO
LHL_GPIO 2	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: No Pull	I: No Pull	VDDIO
LHL_GPIO 3	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: No Pull	I: No Pull	VDDIO
LHL_GPIO 4	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: No Pull	I: No Pull	VDDIO
LHL_GPIO 5	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: No Pull	I: No Pull	VDDIO

(table continues...)

Table 18 (continued) I/O states

Name	I/O	Keeper	Active mode	Low-power state/Sleep (All power present)	Power-down (REG_ON Held Low)	Out-of-reset; Before SW Download (REG_ON High)	(REG_ON = 0) and VDDIOs are present	Power rail
LHL_GPIO 6	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: No Pull	I: No Pull	VDDIO
LHL_GPIO 8	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: No Pull	I: No Pull	VDDIO
LHL_GPIO 9	I/O	Y	I/O: PU, PD, NoPull Programmable [NoPull]	I/O: PU, PD, NoPull Programmable [NoPull]	High-Z, No Pull	I: No Pull	I: No Pull	VDDIO

1) REGON should be tied to GND for CYW55913.

***Note**: When JTAG is not enabled on the GPIO.*

11 Internal regulator electrical specifications

Functional operation is not guaranteed outside of the specification limits provided in this section.

11.1 Main PMU

Table 19 PMU specifications

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input supply voltage	V_{BAT}	–	3.0	3.3	4.8	V
I/O supply voltage	V_{DDIO}		1.71	1.80	1.89	
V_{BAT} UVLO threshold	V_{UVLO_RISE} V_{UVLO_FALL}	Rising (UVLO clear) Falling (UVLO set)	2.32 2.20	2.48 2.34	2.62 2.44	V
V_{DDIO} brownout threshold	V_{BRWO_RISE} V_{BRWO_FALL}	Rising (Brownout clear) Falling (Brownout set)	1.44 1.38	1.51 1.44	1.58 1.51	

11.2 Analog switching regulator specifications

Table 20 Analog switching regulator specifications

Specification	Symbol	Notes	Min	Typ	Max	Unit
Switching frequency	F_{SW}	With calibration (PWM mode only) programming range	3.04 2.8	3.2	3.36 5.0	MHz
Output current	I_{OUT}	PWM mode, max DC at Tj 125°C	–	–	400	mA
Output voltage	V_{OUT}	Active LP Sleep Programming range	0.64	1.12 1.12 0.74	1.26	V
DC accuracy	ΔV_{OUT_ERR}	Untrimmed Trimmed (PWM mode)	-4 -2	–	4 2	%
Ripple voltage	V_{RIPPLE}	PWM mode PFM mode Measured 20 MHz BW limit, static load	–	5 7	10 20	mVpp
Power up time	T_{PU_CSR}	V_{BAT} and V_{DDIO} as always ON, ULBG ON REG_ON < asr_pok	–	472	–	µs
External inductor	L	See Analog switching regulator specifications section for more details	–	2.2	–	µH

(table continues...)

Table 20 (continued) Analog switching regulator specifications

Specification	Symbol	Notes	Min	Typ	Max	Unit
External output capacitor	C_O	See Analog switching regulator specifications section for more details	–	4.7	–	µF
External input capacitor	C_{IN}	See Analog switching regulator specifications section for more details	–	4.7	–	µF

11.3 CLDO

Table 21 CLDO specifications

Specification	Symbol	Notes	Min	Typ	Max	Unit
Input voltage	V_{IN}	$V_{IN} = V_{OUT} + V_{DROPOUT}$	0.74	1.12	1.26	V
Output voltage	V_{OUT}	–	_	0.900	_	V
Output voltage accuracy	–	–	-4	–	4	%
Dropout voltage	$V_{DROPOUT}$	I_{OUT} = 125 mA	80	–	–	mV
Output current	I_{OUT}	T ≤ 25°C	0.01	–	125	mA
		T > 25°C	0.06	–	125	
Line regulation	–	1.12 ≤ V_{IN} ≤ 1.26 V V_{OUT} = 0.9 V IOUT = 125 mA.	–	–	3	mV/V
Load regulation	–	V_{IN} = 1.12 V V_{OUT} = 0.9 V 1 mA ≤ I_{OUT} ≤ 125 mA	–	–	0.125	mV/mA
Load step error	–	V_{IN} = 1.12 V V_{OUT} = 0.9 V I_{OUT} step from 1 mA to 125 mA in 200 ns COUT = 1.0 µF[2)]	–	–	70	mV
PSRR	–	100 Hz ≤ f ≤ 100 kHz V_{IN} = 1.12 V V_{OUT} = 0.9 V IOUT = 125 mA	20	–	–	dB
Turn-on time[1)]	T_{ON}	Time from enable to V_{OUT} = 855 mV IOUT = 60 µA V_{OUT} = 0.9 V COUT = 1.0 µF[2)]	–	40	–	µs

(table continues...)

Table 21 (continued) CLDO specifications

Specification	Symbol	Notes	Min	Typ	Max	Unit
In-rush current	I_{INRUSH}	IOUT = 60 µA V_{OUT} = 0.9 V COUT =1.0 µF [2]	–	–	60	mA
Output capacitor	C_{OUT}	6.3 V, 0201, ±20%	–	1	–	µF

1) Refer to register map for actual inrush delay setting.
2) Output capacitor is Murata GRM033C80J105ME05.

11.4 BTLDO

Table 22 BTLDO specifications

Specification	Symbol	Notes	Min	Typ	Max	Unit
Input supply voltage	V_{BAT}	Range	3.0	3.3	4.8	V
Nominal output voltage	V_{OUT}	–	–	2.915[1]	–	V
Output voltage accuracy	–	–	-4	–	4	%
Dropout voltage	–	I_{OUT} = 400 mA	200	–	–	mV
Output current	I_{OUT}	–	0.2		400	mA
Line regulation	–	3.5 V ≤ V_{BAT} ≤ 4.8 V I_{OUT} = 400 mA, V_{OUT} = 3.3 V	–	–	3	mV/V
Load regulation	–	1 mA ≤ I_{OUT} ≤ 400 mA V_{BAT} = 3.7 V, V_{OUT} = 3.3 V	–	–	0.3	mV/ mA
Load step error	–	Load step from 1 mA to 200 mA in 1 µs, V_{BAT} = 3.7 V, V_{OUT} = 3.3 V, C_{OUT} = 2.2 µF.	–	–	72	mV
PSRR	–	100 Hz ≤ f_{TEST} ≤ 100 kHz I_{OUT} = 200 mA	20	–	–	dB
Turn-on time[2]	T_{ON}		–	–	80	µs
Output current limit	$I_{OUT(LIMIT)}$		–	–	1.1	A
In-rush current	I_{INRUSH}		–	–	193	mA
Output capacitor	C_{OUT}	6.3 V, 0402, ±10%	–	2.2		µF

1) LDO output voltage is configured to 2.915 V with a minimum headroom (V_{BAT}-LDO OUPUT) of 120 mV.
2) Refer to register map for actual inrush delay setting.

11.5 PALDO

Table 23 PALDO specifications

Specification	Symbol	Notes	Min	Typ	Max	Unit
Input supply voltage	V_{BAT}	Range	3.0	3.3	4.8	V
Nominal output voltage	V_{OUT}	–	–	2.915[1)]	–	V
Output voltage accuracy	–	–	-4	–	4	%
Dropout voltage	–	I_{OUT} = 400 mA	200	–		mV
Output current	I_{OUT}	–	0.2	–	400	mA
Line regulation	–	3.5 V ≤ V_{BAT} ≤ 4.8 V I_{OUT} = 400 mA, V_{OUT}=3.3 V	–	–	3	mV/V
Load regulation	–	1 mA ≤ I_{OUT} ≤ 400 mA V_{BAT} = 3.7 V, V_{OUT} = 3.3 V	–	–	0.3	mV/mA
Load step error	–	Load step from 1 mA to 200 mA in 1 µs, V_{BAT} = 3.7 V, V_{OUT} = 3.3 V, C_{OUT} = 2.2 µF.	–	–	72	mV
PSRR	–	100 Hz ≤ f_{TEST} ≤ 100 kHz I_{OUT} = 200 mA	20	–	–	dB
Turn-on time[2)]	T_{ON}		–	–	80	µs
Output current limit	$I_{OUT(LIMIT)}$		–	–	1.1	A
In-rush current	I_{INRUSH}		–	–	193	mA
Output capacitor	C_{OUT}	6.3 V, 0402, ±10%	–	2.2	–	µF

1) LDO output voltage is configured to 2.915 V with a minimum headroom (V_{BAT}-LDO OUPUT) of 120 mV.
2) Refer to register map for actual inrush delay setting.

11.6 RFLDO

Table 24 RFLDO specifications

Specification	Symbol	Notes	Min	Typ	Max	Unit
Input supply voltage	V_{BAT}	Range	3.0	3.3	4.8	V
Nominal output voltage	V_{OUT}	–	–	2.915[1)]	–	V
Output voltage accuracy	–	–	–4	–	4	%
Dropout voltage	–	I_{OUT} = 100 mA	–	127	200	mV

(table continues...)

Table 24 (continued) RFLDO specifications

Specification	Symbol	Notes	Min	Typ	Max	Unit
Output current	I_{OUT}	–	0.1	–	100	mA
Line regulation	–	3.5 V ≤ V_{BAT} ≤ 4.8 V I_{OUT} = 100 mA, V_{OUT} = 3.3 V	–	–	3	mV/V
Load regulation	–	1 mA ≤ I_{OUT} ≤ 100 mA V_{BAT} = 3.7 V, V_{OUT}=3.3 V	–	–	0.3	mV/m A
Load step error	–	Load step from 1 mA to 100 mA in 1 µs, V_{BAT} = 3.7 V, V_{OUT} = 3.3 V, C_{OUT} = 1 µF.	–	–	55	mV
PSRR	–	100 Hz ≤ f_{TEST} ≤ 100 kHz I_{OUT} = 100 mA, V_{BAT} = 3.7 V, V_{OUT} = 3.3 V, C_{OUT} = 1 µF.	–	–	-20	dB
Turn-on time[2)]	T_{ON}		–	–	145	µs
Output current limit	$I_{OUT(LIMIT)}$		–	–	250	mA
In-rush current	I_{INRUSH}		–	–	60	mA
Output capacitor	C_{OUT}	1 mF, 6.3 V, 0201, ±20%	–	1.0	2.2	µF

1) LDO output voltage is configured to 2.915 V with a minimum headroom (V_{BAT}-LDO OUPUT) of 120 mV.
2) Refer to register map for actual inrush delay setting.

11.7 External components

Choice of inductor depends on DCR, ACR, saturation currents, temperature rise criteria, and footprint/height. Use of smaller components may negatively impact overall efficiency performance.

Table 25 Inductor specifications

Vendor	Part Number	L (micro H)	Tol (%)	DCR_{max} (mΩ)	DCR_{AVG} (mΩ)	Current rating (A)	Size (in)	Purpose
Murata	DFE201610E_2R2M	2.2	±20	140	117	1.7	0806	ASR Output Inductor
Murata	LQM2MPN2R2MG0	2.2	±20	138	110	1.2	0806	
Murata	WIP201610S-2R2ML	2.2	±20	140	117	2.0	0806	

Recommended capacitor options are as follows:

Table 26 Capacitor specifications

Vendor	Part	C (micro F)	Tol (%)	Voltage (V)	Temp rating	Size (in)	Purpose
Murata	GRM033R60J224ME15	0.22	±20	6.3	X5R	0201	PMU input bypass
Murata	GRM033R60J105MEA2D	1.0	±20	6.3	X5R	0201	CLDO, RFLDO output
Murata	GRM033C80J105ME05	1.0	±20	6.3	X6S	0201	
Murata	GRM155C70J225KE11	2.2	±10	6.3	X7S	0402	BTLDO, PALDO Outputs
Murata	GRM155R61C225KE11	2.2	±10	16	X5R	0402	
Murata	GRM155R61A475MEAA	4.7	±20	10	X5R	0402	ASR, PMU input bypass
Murata	GRM188R60J475ME84	4.7	±20	6.3	X5R	0603	
Murata	GRM188R60J475KE19	4.7	±10	6.3	X5R	0603	
Murata	GRM188R61C106KAAL	10	±10	16	X5R	0603	

12 DC characteristics

12.1 Absolute maximum ratings

Table 27 Absolute maximum ratings

Parameter	Symbol	Value	Unit
DC supply for VBAT and PA driver supply	ASR_VDDBAT, BTLDO_VDDBAT, WLLDO_VDDBAT	–0.5 to +6.0	V
DC supply voltage for digital I/O	VDDIO, BT_VDDO, PMU_VDD1P8	–0.5 to 2.2	
DC supply voltage for RF switch I/Os	VDDIO_RFSW	–0.5 to 3.9	
DC supply voltage for core	VDDC, AVDD_BBPLL	–0.5 to 1.1	
Maximum undershoot voltage for I/O[1)]	Vundershoot	–0.5	
Maximum overshoot voltage for I/O[1)]	Vovershoot	VDDIO + 0.5	
Maximum junction temperature	Tj	125	°C
Maximum input power for RX input ports[2)]	–	13	dBm

1) Duration not to exceed 25% of the duty cycle.
2) Devices incur a maximum of 3 dB reduction in LNA gain with a maximum input level of 13 dBm at a 1.5% duty-cycle derated from a 7-year lifetime.

12.2 Environmental ratings

Table 28 Environmental ratings

Characteristics	Value	Unit	Conditions
Ambient temperature (T_A)	–40 to +85	°C	Functional operation[1)]
Storage temperature	–40 to +125		–
Relative humidity	< 60	%	Storage
	< 85		Operation

1) The device is functional across this range of temperature. The device autonomously monitors its junction temperature and employs transmit throughput throttling to regulate power dissipation and ensure that the junction temperature is held below maximum ratings for device reliability.

12.3 Recommended operating conditions and DC characteristics

Caution! Functional operation is not guaranteed outside of the limits shown in Table 29, and operation outside these limits for extended periods can adversely affect long-term reliability of the device.

Table 29 Recommended operating conditions and DC characteristics

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
DC supply voltage for VBAT	ASR_VDDBAT, BTLDO_VDDBAT, WLLDO_VDDBAT	3.0[1]	3.3	4.8[2]	V
DC supply voltage for core	VDDC, AVDD_BBPLL	0.86	0.9	0.94	
DC supply voltage for digital I/O	VDDIO, BT_VDDO, PMU_VDD1P8	1.71	1.8	1.89	
DC supply voltage for RF switch I/Os when supporting 3.3 V RF_SW_CTRL pads	VDDIO_RFSW	3.13	3.3	3.47	
External TSSI input	TSSI	0.15	–	0.95	
Internal POR threshold	Vth_POR	0.4		0.7	
Digital I/O pins[3]					
For VDDIO, BT_VDDO = 1.8 V					
Input high voltage	VIH	0.65 × VDDIO	–	–	V
Input low voltage	VIL	–		0.35 × VDDIO	
Output high voltage @ 2 mA	VOH	VDDIO – 0.40		–	
Output low voltage @ 2 mA	VOL	–		0.45	
RF switch control output pins[3]					
For VDDIO_RFSW = 3.3 V					
Output high voltage @ 2 mA	VOH	VDDIO_RFSW – 0.4	–	–	V
Output low voltage @ 2 mA	VOL	–		0.4	
REG_ON Pins					
Input capacitance	CIN	_	_	5	pF
Input high voltage	VIH	1.2	_	VBAT	V
Input low voltage	VIL	_	_	0.3	V
Pull down resistance	R_{PD}	_	50	_	kΩ

1) CYW55913 is functional across this range of voltages. Optimal RF performance specified in the datasheet, however, is guaranteed only for 3.13 V < VBAT < 3.6 V.
2) The maximum continuous voltage is 5.25 V. Voltage transients up to 6.0 V for up to 10 seconds, cumulative duration over the lifetime of the device, are allowed.
Voltage transients as high as 5.5 V for up to 250 seconds, cumulative duration over the lifetime of the device, are allowed.
3) Programmable 2 mA to 16 mA drive strength. Default is 10 mA.

12.4 Electrostatic Discharge (ESD) specifications

Extreme caution must be exercised to prevent electrostatic discharge damage. Proper use of wrist and heel grounding straps to discharge static electricity is required when handling these devices. Always store unused material in its antistatic packaging.

Table 30 ESD specifications

Pin type	Symbol	Conditions	ESD rating	Unit
ESD, Handling Reference: NQY00083, Section 3.4, Group D9, Table B	ESD_HAND_HBM	Human body model contact discharge per JEDEC EID/ JESD22-A114	+/- 2	kV
CDM	ESD_HAND_CDM	Charged device model contact discharge per JEDEC EIA/JESD22-C101	+/- 300 [1)]	V
Latch-up	_	At 125°C	+/- 200	mA

1) BTRF_13dBm and 20dBm pass at 250V.

13 Bluetooth® RF specifications

Unless otherwise stated, limit values apply for the conditions specified in Bluetooth® TX13 transmitter RF specifications and Bluetooth® TX0 transmitter RF specifications. Typical values apply for an ambient temperature of +25°C. Unless otherwise stated, the values in this section are design targets, to be confirmed by silicon characterization. RF port locations for Bluetooth® testing in a two-antenna system - Bluetooth® shared LNA with WLAN shows the RF port locations for testing Bluetooth® in a system configuration with two antennas. Only one of the two system antennas is available to Bluetooth® in this configuration.

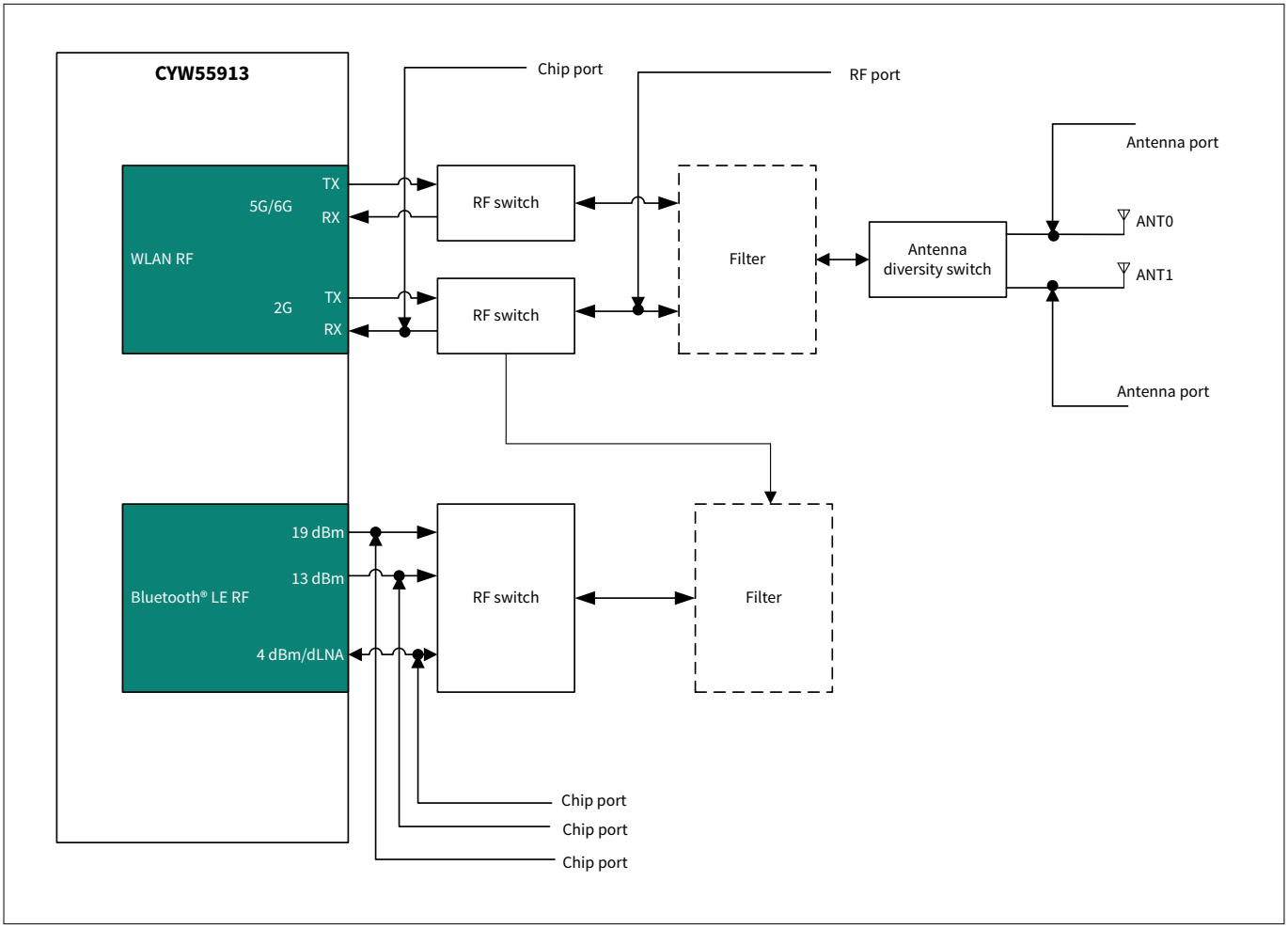


Figure 23 RF port locations for Bluetooth® testing in a two-antenna system - Bluetooth® shared LNA with WLAN

RF port locations for Bluetooth® testing in a three-antenna system - Bluetooth® dedicated LNA with dedicated antenna configuration shows the RF port locations for testing Bluetooth® in a system configuration with three antennas. In this system configuration, any one of the three system antennas can be used for Bluetooth®.

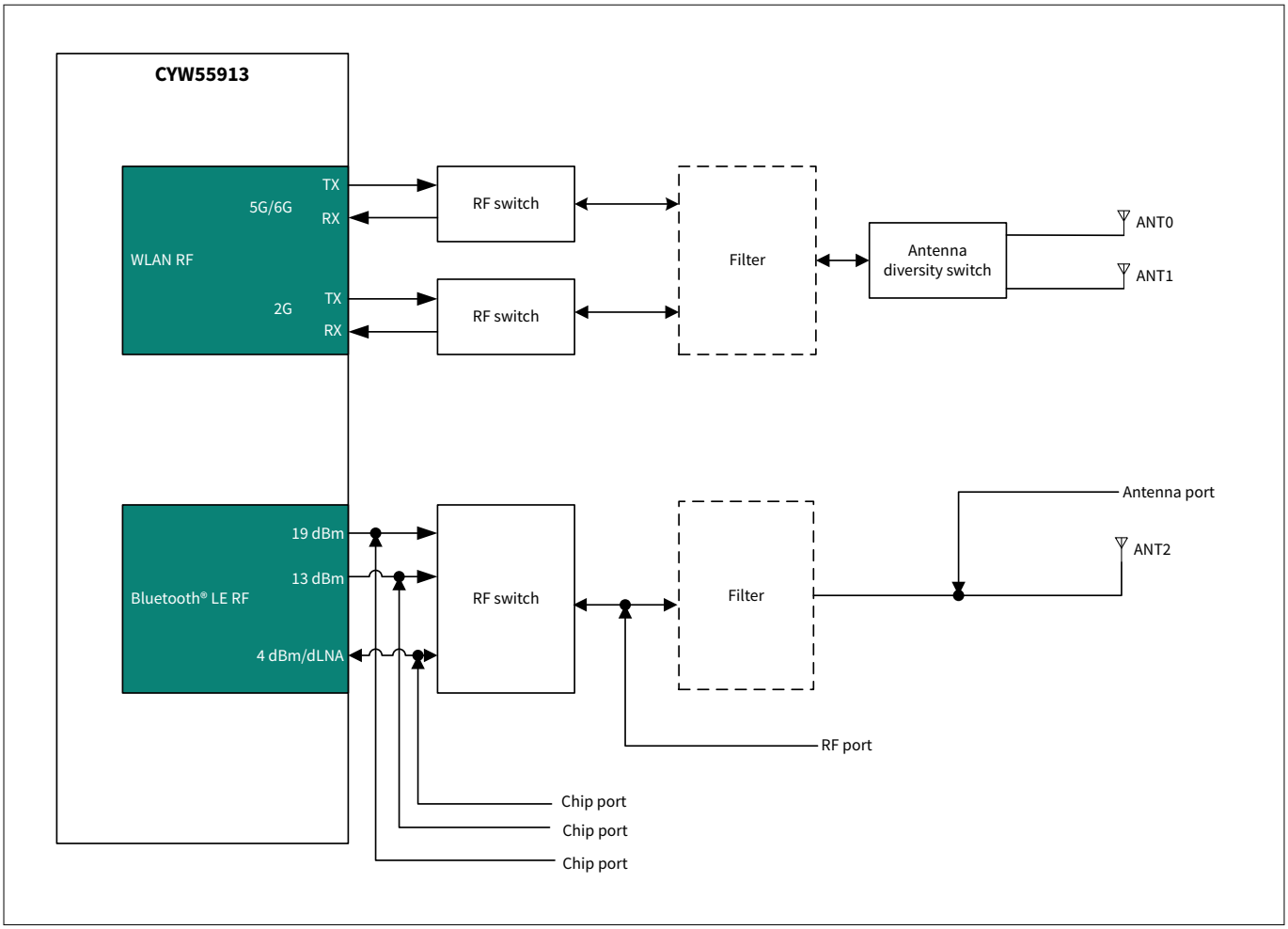


Figure 24 **RF port locations for Bluetooth® testing in a three-antenna system - Bluetooth® dedicated LNA with dedicated antenna configuration**

13.1 Bluetooth® LE receiver and TX13 transmitter specifications

Table 31 **Bluetooth® LE receiver and TX13 transmitter specifications**

Parameter	Conditions	Min	Typ	Max	Unit
***Note**: The specifications in this table are measured at the Chip port output unless otherwise specified.*					
Frequency range	–	2402	–	2480	MHz
RX sensitivity (dLNA)[1)]	GFSK, 1 Mbps	–	–101.0	–	dBm
	GFSK, 2 Mbps	–	–97.0	–	dBm
	GFSK, 500 Kbps	–	–106.0	–	dBm
	GFSK, 125 Kbps	–	–111.0	–	dBm
RX sensitivity (sLNA)[1)]	GFSK, 1 Mbps	–	–101.5	–	dBm
	GFSK, 2 Mbps	–	–97.5	–	dBm
	GFSK, 500 Kbps	–	–106.5	–	dBm

(table continues...)

Table 31 (continued) Bluetooth® LE receiver and TX13 transmitter specifications

Parameter	Conditions	Min	Typ	Max	Unit
	GFSK, 125 Kbps	–	–111.5	–	dBm
Interference performance [2)]					
C/I co-channel	uncoded 1Ms/s, 30.8% PER	–	8.5	21	dB
C/I 1 MHz adjacent channel	uncoded 1Ms/s, 30.8% PER	–	-2.5	15	dB
C/I 2 MHz adjacent channel	uncoded 1Ms/s, 30.8% PER	–	-34	-17	dB
C/I ≥ 3 MHz adjacent channel	uncoded 1Ms/s, 30.8% PER	–	-39	-27	dB
C/I image channel	uncoded 1Ms/s, 30.8% PER	–	-30	-9	dB
C/I 1 MHz adjacent to image channel	uncoded 1Ms/s, 30.8% PER	–	-42	-15	dB
C/I co-channel	2Ms/S, 30.8% PER	–	7.5	21	dB
C/I 2 MHz adjacent channel	2Ms/S, 30.8% PER	–	0	15	dB
C/I 4 MHz adjacent channel	2Ms/S, 30.8% PER	–	-41	-17	dB
C/I ≥ 6 MHz adjacent channel	2Ms/S, 30.8% PER	–	-51	-27	dB
C/I image channel	2Ms/S, 30.8% PER	–	-31	-9	dB
C/I 2 MHz adjacent to image channel	2Ms/S, 30.8% PER	–	-37	-15	dB
C/I co-channel	LE coded (S=2), 30.8% PER	–	4.0	17	dB
C/I 1 MHz adjacent channel	LE coded (S=2), 30.8% PER	–	-11	11	dB
C/I 2 MHz adjacent channel	LE coded (S=2), 30.8% PER	–	-51	-21	dB
C/I ≥ 3 MHz adjacent channel	LE coded (S=2), 30.8% PER	–	-53	-31	dB
C/I Image channel	LE coded (S=2), 30.8% PER	–	-35	-13	dB
C/I 1 MHz adjacent to image channel	LE coded (S=2), 30.8% PER	–	-49	-19	dB
C/I co-channel	LE coded (S=8), 30.8% PER	–	6.5	12	dB
C/I 1 MHz adjacent channel	LE coded (S=8), 30.8% PER	–	-16	6	dB
C/I 2 MHz adjacent channel	LE coded (S=8), 30.8% PER	–	-51	-26	dB
C/I ≥ 3 MHz adjacent channel	LE coded (S=8), 30.8% PER	–	-61	-36	dB
C/I Image channel	LE coded (S=8), 30.8% PER	–	-34	-18	dB
C/I 1 MHz adjacent to image channel	LE coded (S=8), 30.8% PER	–	-49	-24	dB
TX power	–	–	13.0	–	dBm
Power control step	–	–	4	–	dB
Minimum power control range	–	–	28	–	dB
Mod Char: delta F1 average	GFSK, 1 Mbps	225	250	275.0	kHz
Mod Char: delta F2 max	GFSK, 1 Mbps	185	240	–	kHz

(table continues...)

Table 31 (continued) Bluetooth® LE receiver and TX13 transmitter specifications

Parameter	Conditions	Min	Typ	Max	Unit
Mod Char: ratio	GFSK, 1 Mbps	0.8	1.0	–	no unit
Mod Char: delta F1 average	GFSK, 2 Mbps	450	500	550	kHz
Mod Char: delta F2 max	GFSK, 2 Mbps	370	460	–	kHz
Mod Char: ratio	GFSK, 2 Mbps	0.8	0.95	–	no unit
Mod Char: delta F1 average	GFSK, 125 kbps	225	250	275	kHz

1) With stable mod index and 37 byte packet length.
2) The maximum value represents the actual Bluetooth® specification required for Bluetooth® qualification as defined in the v4.0 specification.

13.2 Bluetooth® LE TX0 transmitter specifications

Table 32 Bluetooth® LE TX0 transmitter specifications

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range	–	2402		2480	MHz
TX power	–	–	4.0	–	dBm
Power control step	–	–	4	–	dB
Minimum power control range	–	–	28	–	dB
Mod Char: delta F1 average	GFSK, 1 Mbps	225	250	275.0	kHz
Mod Char: delta F2 max	GFSK, 1 Mbps	185	240	–	kHz
Mod Char: ratio	GFSK, 1 Mbps	0.8	1.05	–	no unit
Mod Char: delta F1 average	GFSK, 2 Mbps	450	500	550	kHz
Mod Char: delta F2 max	GFSK, 2 Mbps	370	460	–	kHz
Mod Char: ratio	GFSK, 2 Mbps	0.8	0.95	–	no unit
Mod Char: delta F1 average	GFSK, 125 kbps	225	250	275	kHz

13.3 Bluetooth® TX19 LE transmitter RF specifications

Table 33 Bluetooth® TX19 LE transmitter RF specifications

Parameter	Conditions	Min	Typ	Max	Unit
Frequency range	–	2402	–	2480	MHz
TX power	–	–	19	–	dBm
Power control step	–	–	4	–	dB
Minimum power control range	–	–	6	–	dB
Mod Char: delta F1 average	GFSK, 1 Mbps	225	250	275.0	kHz
Mod Char: delta F2 max	GFSK, 1 Mbps	185	242	–	kHz

(table continues...)

Table 33 (continued) Bluetooth® TX19 LE transmitter RF specifications

Parameter	Conditions	Min	Typ	Max	Unit
Mod Char: ratio	GFSK, 1 Mbps	0.8	1.0	–	no unit
Mod Char: delta F1 average	GFSK, 2 Mbps	450	500	550	kHz
Mod Char: delta F2 max	GFSK, 2 Mbps	370	470	–	kHz
Mod Char: ratio	GFSK, 2 Mbps	0.8	1.0	–	no unit
Mod Char: delta F1 average	GFSK, 125 kbps	225	250	275	kHz

14 WLAN RF specifications

14.1 Introduction

CYW5591x includes an integrated tri-band radio that supports the 2.4 GHz, 5/6 GHz bands. This section describes the RF characteristics of the 2.4 GHz and 5/6 GHz radios.

14.2 WLAN 2.4 GHz RX performance specifications

***Note**: The values in Table 34 are specified at the chip port unless otherwise noted.*

Table 34 WLAN 2.4 GHz RX performance specifications

Parameter	Conditions		Min	Typ	Max	Unit
Sensitivity						
RX sensitivity IEEE 802.11b (8% PER for 1024 octet PSDU)	1 Mbps	-	-	-101.5	-	dBm
	2 Mbps	-	-	-98.0	-	dBm
	5.5 Mbps	-	-	-96.5	-	dBm
	11 Mbps	-	-	-93.0	-	dBm
RX sensitivity IEEE 802.11g (10% PER for 1024 octet PSDU)	6 Mbps	-	-	-96.0	-	dBm
	9 Mbps	-	-	-95.0	-	dBm
	12 Mbps	-	-	-94.0	-	dBm
	18 Mbps	-	-	-91.5	-	dBm
	24 Mbps	-	-	-89.0	-	dBm
	36 Mbps	-	-	-85.5	-	dBm
	48 Mbps	-	-	-81.0	-	dBm
	54 Mbps	-	-	-79.5	-	dBm
RX sensitivity IEEE 802.11n 20 MHz channel spacing with high performance channel coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: 800 ns GI, high performance channel coding, and non-STBC	MCS0	-	-	-96.0	-	dBm
	MCS1	-	-	-95.0	-	dBm
	MCS2	-	-	-93.0	-	dBm
	MCS3	-	-	-90.5	-	dBm
	MCS4	-	-	-86.5	-	dBm
	MCS5	-	-	-82.5	-	dBm
	MCS6	-	-	-80.5	-	dBm
	MCS7	-	-	-79.0	-	dBm
RX sensitivity IEEE 802.11ax 20 MHz channel spacing with high performance channel coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 µs + 2	MCS0, Nss = 1	-	-	-96.0	-	dBm
	MCS7, Nss = 1	-	-	-79.0	-	dBm
	MCS8, Nss = 1	-	-	-75.5	-	dBm
	MCS9, Nss = 1	-	-	-73.5	-	dBm

(table continues...)

Table 34 (continued) WLAN 2.4 GHz RX performance specifications

Parameter	Conditions		Min	Typ	Max	Unit
× LTF high performance channel coding, non-STBC, and 20 MHz BW	MCS11, Nss = 1	-	-	-64.5	-	dBm
RX sensitivity IEEE 802.11ax HE-RE PPDU 10% PER for 4096 octet PSDU at chip port. Defined for default parameters: CP/LTF = 0.8 + 2 × LTF	RU242, MCS0, Nss = 1	-	-	-98.5	-	dBm
	RU106, MCS0, Nss = 1	-	-	-98.5	-	dBm
Maximum receiver level at 2.4 GHz	1, 2 Mbps (8% PER, 1024 octets)	-	-	-5.0	-	dBm
	5.5, 11 Mbps (8% PER, 1024 octets)	-	-	-5.0	-	dBm
	6-54 Mbps (10% PER, 1024 octets)	-	-	-10.0	-	dBm
	MCS0-MCS7 rates (10% PER, 4096 octets)	-	-	-10.0	-	dBm
	MCS8-MCS11 rates (10% PER, 4096 octets)	-	-	-10.0	-	dBm
RSSI accuracy [1)]	Range -90 dBm to -30 dBm	_	_	-3.0 to +3.0	_	dB
	Range above -30 dBm	_	_	-3.0 to +3.0	_	dB
ACI/AACI						
Adjacent channel rejection - CCK (difference between interfering and desired signal (20 MHz apart) at 8% PER for 1024 octet PSDU with desired signal level as 6 dB higher than IEEE specification) [2)]	Desired and interfering signal 30 MHz apart					
	1 Mbps	-74 dBm	-	>48	-	dB
	Desired and interfering signal 25 MHz apart					
	11 Mbps	-70 dBm	-	>46	-	dB
Adjacent channel rejection - OFDM (difference between interfering and desired signal (20 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as 3 dB higher than IEEE specification) [3)]	6 Mbps	-79 dBm	-	40.0	-	dB
	54 Mbps	-62 dBm	-	22.0	-	dB
Adjacent channel rejection - MCS0-11 in 20 MHz (difference between interfering and desired signal (20 MHz apart) at 10% PER for 4096 octet PSDU	MCS0	-79 dBm	-	35.0	-	dB
	MCS7	-61 dBm	-	11.5	-	dB

(table continues...)

Table 34 (continued) WLAN 2.4 GHz RX performance specifications

Parameter	Conditions		Min	Typ	Max	Unit
with desired signal level 3 dB higher than IEEE specification) [3]	HE9	-54 dBm	_	10.3	_	dB
	HE11	-49 dBm	_	5.3	_	dB
In-band static CW jammer immunity (fc -8 MHz < fcw < +8 MHz)	RX PER < 1%,54 Mbps OFDM, 1024octet PSDU for: (RxSens +23 dB < Rxlevel < maximum input level)	_	_	-80.0	_	_

1) The minimum and maximum values shown have a 95% confidence level.
2) Desired signal is at a power level 6 dB higher than the IEEE specification for the minimum sensitivity limit.
3) Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.

14.3 WLAN 2.4 GHz Tx performance specifications

***Note**: The values in Table 35 are specified at the chip port unless otherwise noted.*

Table 35 WLAN 2.4 GHz TX performance specifications

Parameter	Conditions	EVM limit	Min	Typ	Max	Unit
EVM not exceed @ output power						
TX power for highest power level setting at 25°C and VBAT = 3.3 V with spectral mask and EVM compliance[1]	DSSS - 1 Mbps	–9 dB	–	24.0	–	dBm
	DSSS - 11 Mbps	–9 dB	–	24.0	–	dBm
	OFDM - BPSK, R = 1/2	–8 dB	–	23.5	–	dBm
	OFDM - QPSK, R = 3/4	–13 dB	–	23.5	–	dBm
	OFDM - 16QAM, R = 3/4	–19 dB	–	23.5	–	dBm
	OFDM - 64QAM, R = 3/4	–25 dB	–	23.0	–	dBm
	OFDM - 64QAM, R = 5/6 - HE20	–28 dB	–	22.5	–	dBm
	OFDM - 256QAM, R = 3/4 - HE20	–30 dB	–	22.0	–	dBm
	OFDM - 256QAM, R = 5/6 - HE20	–32 dB	–	21.0	–	dBm
	OFDM - 1024QAM, R = 3/4 - HE20	–35 dB	–	20.0	–	dBm
	OFDM - 1024QAM, R = 5/6 - HE20	–35 dB	–	20.0	–	dBm
Carrier suppression	–	–	–	-45.0	–	dBc
TX power control dynamic range	–	–	–	34	–	dB
Gain control step	–	–	–	0.5	–	dB

(table continues...)

Table 35 (continued) WLAN 2.4 GHz TX performance specifications

Parameter	Conditions	EVM limit	Min	Typ	Max	Unit
Tx power control variation [2)]	Applies to -10 dBm to 24 dBm output power range.	–	–	±1.5	–	dB

1) The TX power at the chip output port is controlled by firmware and is approximately 1.5 dB lower from the numbers mentioned here, to account for closed loop TX power control variation and other factors.
2) Tx power variation ±3.0 dB for process, voltage, and temperature variation across -40°C to +85°C.

14.4 WLAN 5 GHz Rx performance specifications

***Note**: The values in Table 36 are specified at the chip port unless otherwise noted.*

Table 36 WLAN 5 GHz Rx performance specifications

Parameter	Conditions		Min	Typ	Max	Unit
Sensitivity						
RX sensitivity IEEE 802.11a (10% PER for 1000 octet PSDU)	6 Mbps	–	–	-94.5	–	dBm
	9 Mbps	–	–	-93.0	–	dBm
	12 Mbps	–	–	-92.0	–	dBm
	18 Mbps	–	–	-90.0	–	dBm
	24 Mbps	–	–	-87.5	–	dBm
	36 Mbps	–	–	-84.0	–	dBm
	48 Mbps	–	–	-79.5	–	dBm
	54 Mbps	–	–	-78.0	–	dBm
RX sensitivity IEEE 802.11n 20 MHz channel spacing with high performance channel coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: 800 ns GI, high performance channel coding, and non-STBC	MCS0	–	–	-94.5	–	dBm
	MCS1	–	–	-93.0	–	dBm
	MCS2	–	–	-91.0	–	dBm
	MCS3	–	–	-88.5	–	dBm
	MCS4	–	–	-85.5	–	dBm
	MCS5	–	–	-81.0	–	dBm
	MCS6	–	–	-79.0	–	dBm
	MCS7	–	–	-77.5	–	dBm
RX sensitivity IEEE 802.11ac 20 MHz channel spacing with high performance channel coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: 800 ns GI, high performance channel coding, and non-STBC	MCS7, Nss = 1	–	–	-77.5	–	dBm
	MCS8, Nss = 1	–	–	-73.5	–	dBm

(table continues...)

Table 36 (continued) WLAN 5 GHz Rx performance specifications

Parameter	Conditions		Min	Typ	Max	Unit
RX Sensitivity IEEE 802.11ax 20 MHz channel spacing with high performance channel coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 µs + 2 × LTF, high performance channel coding, non-STBC, and 20 MHz BW	MCS0, Nss = 1	–	–	-94.5	–	dBm
	MCS7, Nss = 1	–	–	-77.5	–	dBm
	MCS8, Nss = 1	–	–	-73.5	–	dBm
	MCS9, Nss = 1	–	–	-71.5	–	dBm
	MCS11, Nss = 1	–	–	-62.2	–	dBm
RX sensitivity IEEE 802.11ax HE-RE PPDU (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 µs + 2 × LTF	RU242, MCS0, Nss = 1	–	–	-97.0	–	dBm
	RU106, MCS0, Nss = 1	–	–	-97.0	–	dBm
Maximum receiver level at 5 GHz	6-54 Mbps (10% PER, 1024 octets)	–	–	-5	–	dBm
	MCS0-MCS7 rates (10% PER, 4096 octets)	–	–	-5	–	dBm
	MCS8-MCS11 rates (10% PER, 4096 octets)	–	–	-8	–	dBm
RSSI accuracy [1)]	Range -90 dBm to -30 dBm	_	_	-3.0 to +3.0	_	dB
	Range above -30dBm	_	_	-3.0 to +3.0	_	dB
ACI/AACI						
Adjacent channel rejection - OFDM (difference between interfering and desired signal (20 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as 3 dB higher than IEEE specification)[2)]	6 Mbps	–79 dBm	–	28.5	–	dB
	54 Mbps	–62 dBm	–	9.5	–	dB
Adjacent channel rejection - MCS0–11 in 20 MHz (difference between interfering and desired signal (20 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level 3 dB higher than IEEE spec)[2)]	MCS0	–79 dBm	–	25.0	–	dB
	MCS7	–61 dBm	–	5.0	–	dB
	HE9	-54 dBm	_	0.4	_	dB
	HE11	-49 dBm	_	-5.3	_	dB

1) The minimum and maximum values shown have a 95% confidence level.
2) Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.

14.5 WLAN 5 GHz Tx performance specifications

***Note**: The values in Table 37 are specified at the chip port unless otherwise noted.*

Table 37 WLAN 5 GHz TX performance specifications

Parameter	Condition	EVM limit	Min	Typ	Max	Unit
EVM not exceed @ output power						
TX power for highest power level setting at 25°C and VBAT = 3.3 V with spectral mask and EVM compliance[1)]	OFDM - BPSK, R = 1/2	–8 dB	–	22.5	–	dBm
	OFDM - QPSK, R = 3/4	–13 dB	–	22.5	–	dBm
	OFDM - 16QAM, R = 3/4	–19 dB	–	22.5	–	dBm
	OFDM - 64QAM, R = 3/4	–25 dB	–	21.5	–	dBm
	OFDM - 64QAM, R = 5/6 HT20	–28 dB	–	21.0	–	dBm
	OFDM - 256QAM, R = 3/4 - VHT20	–30 dB	–	20.0	–	dBm
	OFDM - 256QAM, R = 3/4 - HE20	–30 dB	–	20.0	–	dBm
	OFDM - 256QAM, R = 5/6 - HE20	–32 dB	–	19.0	–	dBm
	OFDM - 1024QAM, R = 3/4 - HE20	–35 dB	–	18.0	–	dBm
	OFDM - 1024QAM, R = 5/6 - HE20	–35 dB	–	18.0	–	dBm
Carrier suppression	–	–	–	-45.0	–	dBc
TX power control dynamic range	–	–	–	31	–	dB
Gain control step	–	–	–	0.5	–	dB
Tx power control variation [2)]	Applies to -10 dBm to 20.5 dBm output power range.	–	–	±1.5	–	dB

1) The TX power at the chip output port is controlled by firmware and is approximately 1.5 dB lower from the numbers mentioned herein, to account for closed loop TX power control variation and other factors.
2) Tx power variation ±3.0 dB for process, voltage, and temperature variation across -40°C to +85°C.

14.6 WLAN 6 GHz Rx performance specifications

***Note**: The values in WLAN 6 GHz Rx performance specifications are specified at the chip port unless otherwise noted.*

Table 38 WLAN 6 GHz Rx performance specifications

Parameter	Conditions		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
			UNII-5			UNII-6			UNII-7			UNII-8			
Sensitivity															
Rx Sensitivity IEEE 802.11a (10% PER for 1000 octet PSDU)	6 Mbps	–	–	–95.0	–	–	–95.0	–	–	–94.5	–	–	–93.0	–	dBm
	9 Mbps	–	–	–94.0	–	–	–94.0	–	–	–93.5	–	–	–92.0	–	dBm
	12 Mbps	–	–	–92.5	–	–	–92.5	–	–	–92.5	–	–	–91.0	–	dBm
	18 Mbps	–	–	–90.0	–	–	–90.0	–	–	–90.0	–	–	–88.5	–	dBm
	24 Mbps	–	–	–87.0	–	–	–87.0	–	–	–87.0	–	–	–85.5	–	dBm
Rx Sensitivity IEEE 802.11ax 20 MHz channel spacing with High Performance Coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 µs + 2 × LTF, High Performance Coding, non-STBC, and 20 MHz BW[1)]	MCS0, Nss = 1	–	–	–95.0	–	–	–95.0	–	–	–95.0	–	–	–93.5	–	dBm
	MCS1, Nss = 1	–	–	–93.5	–	–	–93.5	–	–	–93.0	–	–	–92.0	–	dBm
	MCS2, Nss = 1	–	–	–91.0	–	–	–91.0	–	–	–90.5	–	–	–89.0	–	dBm
	MCS3, Nss = 1	–	–	–88.5	–	–	–88.5	–	–	–88.0	–	–	–86.5	–	dBm
	MCS4, Nss = 1	–	–	–84.5	–	–	–84.5	–	–	–84.0	–	–	–83.0	–	dBm
	MCS5, Nss = 1	–	–	–80.5	–	–	–80.5	–	–	–80.0	–	–	–79.0	–	dBm
	MCS6, Nss = 1	–	–	–79.0	–	–	–79.0	–	–	–78.5	–	–	–77.5	–	dBm
	MCS7, Nss = 1	–	–	–77.5	–	–	–77.5	–	–	–77.0	–	–	–75.5	–	dBm

(table continues...)

Table 38 (continued) WLAN 6 GHz Rx performance specifications

Parameter	Conditions		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
			UNII-5			UNII-6			UNII-7			UNII-8			
Rx Sensitivity IEEE 802.11ax 20 MHz channel spacing with High Performance Coding (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 µs + 2 × LTF, High Performance Coding, non-STBC, and 20 MHz BW[1)]	MCS8, Nss = 1	–	–	–73.5	–	–	–73.5	–	–	–73.0	–	–	–71.5	–	dBm
	MCS9, Nss = 1	–	–	–71.0	–	–	–71.0	–	–	–70.5	–	–	–69.5	–	dBm
	MCS10, Nss = 1	–	–	–66.5	–	–	–66.5	–	–	–66.0	–	–	–64.5	–	dBm
	MCS11, Nss = 1	–	–	–62.5	–	–	–62.5	–	–	–62.0	–	–	–60.5	–	dBm
Rx Sensitivity IEEE 802.11ax HE-RE PPDU (10% PER for 4096 octet PSDU) at chip port. Defined for default parameters: CP/LTF = 0.8 µs + 2 × LTF[1)]	RU242, MCS0, Nss = 1	–	–	–97.0	–	–	–97.0	–	–	–96.5	–	–	–95.0	–	dBm
	RU242, MCS1, Nss = 1	–	–	–94.0	–	–	–94.0	–	–	–93.5	–	–	–92.0	–	dBm
	RU242, MCS2, Nss = 1	–	–	–91.0	–	–	–91.0	–	–	–90.5	–	–	–89.5	–	dBm
	RU106, MCS0, Nss = 1	–	–	–97.0	–	–	–97.0	–	–	–96.5	–	–	–95.5	–	dBm

(table continues...)

Table 38 (continued) WLAN 6 GHz Rx performance specifications

Parameter	Conditions		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
			UNII-5			UNII-6			UNII-7			UNII-8			
Maximum Receiver Level @ 6 GHz	6–24 Mbps (10% PER, 1024 octets)	–	–	–5.0	–	–	–5.0	–	–	–5.0	–	–	–5.0	–	dBm
	MCS0–MCS7 rates (10% PER, 4096 octets)	–	–	–5.0	–	–	–5.0	–	–	–5.0	–	–	–5.0	–	dBm
	MCS8–MCS11 rates (10% PER, 4096 octets)	–	–	–8.0	–	–	–8.0	–	–	–8.0	–	–	–8.0	–	dBm
Adjacent Channel Rejection - OFDM (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 1000 octet PSDU with desired signal level as 3 dB higher than IEEE spec)[2)]	6 Mbps	–79 dBm	–	28.5	–	–	29.0	–	–	29.0	–	–	28.0	–	dB
	24 Mbps	–76 dBm	–	21.0	–	–	21.0	–	–	21.5	–	–	20.5	–	dB
Adjacent Channel Rejection -	MCS0	–79 dBm	–	27.0	–	–	27.0	–	–	27.5	–	–	27.0	–	dB
	MCS7	–61 dBm	–	6	–	–	5.5	–	–	6.5	–	–	7.0	–	dB

(table continues...)

Table 38 (continued) WLAN 6 GHz Rx performance specifications

Parameter	Conditions		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
			UNII-5			UNII-6			UNII-7			UNII-8			
MCS0–11 in 20 MHz (Difference between interfering and desired signal (20 MHz apart) at 10% PER for 4096 octet PSDU with desired signal level 3 dB higher than IEEE spec)[2]	MCS9	–54 dBm	–	1.0	–	–	1.0	–	–	1.5	–	–	1.0	–	dB
	MCS11	–49 dBm	–	–5.0	–	–	–5.0	–	–	–4.5	–	–	–5.0	–	dB
Other RF parameters															
RSSI accuracy[3]	Range –85 dBm to –30 dBm	–	–3	–	3	–3	–	3	–3	–	3	–3	–	3	dB
	Range above –30 dBm	–	–3	–	3	–3	–	3	–3	–	3	–3	–	3	dB

1) Sensitivity degradations for alternate settings in MCS modes. SGI: 1.5 dB (1024QAM rates in 20 MHz) and negligible (for other rates/BW).
2) Desired signal is at a power level 3 dB higher than the IEEE specification for the minimum sensitivity limit.
3) The minimum and maximum values shown have a 95% confidence level.

14.7 WLAN 6 GHz Tx performance specifications

***Note**: The values in Table WLAN 6 GHz Tx performance specifications are specified at the chip port unless otherwise noted*

Table 39 WLAN 6 GHz Tx performance specifications

Parameter	Condition	EVM	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
			UNII-5			UNII-6			UNII-7			UNII-8			
EVM not exceed @ output power															
TX power for highest power level setting at 25°C and VBAT = 3.3 V with spectral mask and EVM compliance[1)]	OFDM BPSK, R = 1/2	–8 dB	–	21.0	–	–	21.0	–	–	20.5	–	–	20.5	–	dBm
	OFDM - BPSK, R = 3/4	–8 dB	–	21.0	–	–	21.0	–	–	20.5	–	–	20.5	–	dBm
	OFDM - QPSK, R = 3/4	–13 dB	–	21.0	–	–	21.0	–	–	20.5	–	–	20.5	–	dBm
	OFDM - 16QAM, R = 1/2	–16 dB	–	21.0	–	–	21.0	–	–	20.5	–	–	20.5	–	dBm
	OFDM - 16QAM, R = 3/4 - HE20	–19 dB	–	21.0	–	–	21.0	–	–	20.5	–	–	20.5	–	dBm
	OFDM - 64QAM, R = 5/6 - HE20	–28 dB	–	19.5	–	–	19.5	–	–	19.0	–	–	18.5	–	dBm
	OFDM - 256QAM, R = 3/4 - HE20	–30 dB	–	19.0	–	–	19.0	–	–	18.5	–	–	18.0		dBm
	OFDM - 256QAM, R = 5/6 - HE20	–32 dB	–	18.5	–	–	18.0	–	–	18.0	–	–	17.0	–	dBm
	OFDM - 1024QAM, R = 3/4 - HE20	–35 dB	–	17.5	–	–	17.5	–	–	17.5	–	–	16.5	–	dBm
	OFDM - 1024QAM, R = 5/6 - HE20	–35 dB	–	17.5	–	–	17.5	–	–	17.5	–	–	16.5	–	dBm
Carrier suppression	–	–	–	–45.0	–	–	–45.0	–	–	–45.0	–	–	–45.0	–	dBc

(table continues...)

Table 39 (continued) WLAN 6 GHz Tx performance specifications

Parameter	Condition	EVM	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	Unit
			UNII-5			UNII-6			UNII-7			UNII-8			
TX power control dynamic range	–	–	–	29.0	–	–	29.0	–	–	29.0	–	–	29.0	–	dB
Gain control step	–	–	–	0.5	–	–	0.5	–	–	0.5	–	–	0.5	–	dB
TX power variation[2)]	Applies to –10 dBm to 19 dBm output power range.	–	–	±1.5	–	–	±1.5	–	–	±1.5	–	–	±1.5	–	dB

1) The TX power at the chip output port is controlled by firmware and is approximately 1.5 dB lower from the numbers across process corners, to account for closed loop TX power control and other factors.
2) Tx power variation ±3.0 dB for process, voltage and temperature variation across –40°C to +85°C.

15 System power consumption

15.1 WLAN current consumption 2.4/5 GHz

The WLAN current consumption measurements are shown in Table 40. All values in Table 40 are with the M33 MCU core in deep sleep.

Table 40 WLAN current consumption - 2.4/5 GHz

Mode	Output power	Band	Typical current at TA = +25°C		Unit
			VBAT = 3.3 V	VDDIO = 1.8 V	
Sleep Modes					
Off[1]	–	–	0.27	0.47	µA
Sleep[2]	–	–	76	9	µA
IEEE power save, DTIM 1[3]	–	2.4 GHz	657	28.6	µA
IEEE power save, DTIM 3[3]	–	2.4 GHz	276	14.8	µA
IEEE power save, DTIM 10[3]	–	2.4 GHz	140	10.6	µA
IEEE power save, DTIM 1[4]	–	5 GHz	510	24.1	µA
IEEE power save, DTIM 3[4]	–	5 GHz	227	13.3	µA
IEEE power save, DTIM 10[4]	–	5 GHz	126	10.2	µA
All values in below table are with the M33 MCU core in active state					
Active modes[5]					
Transmit					
DSSS- 1 Mbps[6] , [7]	Max output power, 100% duty cycle	2.4 GHz	258.0	2.4	mA
DSSS- 11 Mbps[6]	Max output power, 100% duty cycle	2.4 GHz	268.0	2.4	mA
OFDM - BPSK, R = 1/2 (MCS0)[8]	Max output power, 100% duty cycle	2.4 GHz	218.0	1.9	mA
OFDM - QPSK, R = 3/4 (MCS2)[8]	Max output power, 100% duty cycle	2.4 GHz	255.0	1.9	mA
OFDM - 16QAM, R = 3/4 (MCS4)[8]	Max output power, 100% duty cycle	2.4 GHz	265.0	1.9	mA
OFDM - 64QAM, R = 3/4 (MCS6) [9]	Max output power, 100% duty cycle	2.4 GHz	257.4	1.9	mA
OFDM - 64QAM, R = 5/6 (MCS7) [13] , [7]	Max output power, 100% duty cycle	2.4 GHz	249.4	1.9	mA
OFDM - 256QAM, R = 3/4 (MCS8)[10]	Max output power, 100% duty cycle	2.4 GHz	227.6	1.9	mA

(table continues...)

Table 40 (continued) WLAN current consumption - 2.4/5 GHz

Mode	Output power	Band	Typical current at TA = +25°C		Unit
			VBAT = 3.3 V	VDDIO = 1.8 V	
OFDM - 256QAM, R = 5/6 (MCS9)[7], [11],	Max output power, 100% duty cycle	2.4 GHz	219.3	1.9	mA
OFDM - 1024QAM, R = 3/4 (MCS10)[12]	Max output power, 100% duty cycle	2.4 GHz	206.0	1.9	mA
OFDM - 1024QAM, R = 5/6 (MCS11)[12], [7]	Max output power, 100% duty cycle	2.4 GHz	206.4	1.9	mA
OFDM - BPSK, R = 1/2 (6 Mbps)[13], [7]	Max output power, 100% duty cycle	5 GHz	296.0	2.1	mA
OFDM - QPSK, R = 3/4 (MCS2)[13]	Max output power, 100% duty cycle	5 GHz	328.5	2.1	mA
OFDM - 16QAM, R = 3/4 (MCS4)[13]	Max output power, 100% duty cycle	5 GHz	339.2	2.1	mA
OFDM - 64QAM, R = 3/4(MCS6) [14], [7]	Max output power, 100% duty cycle	5 GHz	320.2	2.1	mA
OFDM - 64QAM, R = 5/6(MCS7) [10], [7],	Max output power, 100% duty cycle	5 GHz	313.4	2.1	mA
OFDM - 256QAM, R = 3/4 (MCS8)[15]	Max output power, 100% duty cycle	5 GHz	299.6	2.1	mA
OFDM - 256QAM, R = 5/6(MCS9) [16], [7]	Max output power, 100% duty cycle	5 GHz	282.7	2.1	mA
OFDM - 1024QAM, R = 3/4 (MCS10)[17]	Max output power, 100% duty cycle	5 GHz	266.1	2.1	mA
OFDM - 1024QAM, R = 5/6(MCS11)[17], [7]	Max output power, 100% duty cycle	5 GHz	267.0	2.1	mA
Receive					
1 Mbps[18]	–	2.4 GHz	31.9	0.79	mA
6 Mbps	_	2.4 GHz	32.2	0.79	mA
11 Mbps	_	2.4 GHz	32.2	0.79	mA
MCS7[18]	–	2.4 GHz	33.6	0.79	mA
MCS11[18]	–	2.4 GHz	34.6	0.79	mA
CRS[19]	–	2.4 GHz	31.0	0.79	mA
6 Mbps[18]	–	5 GHz	41.3	0.79	mA
MCS7[18]	–	5 GHz	42.8	0.79	mA
MCS9[18]	-	5 GHz	43.1	0.79	mA
MCS11[18]	–	5 GHz	43.8	0.79	mA

(table continues...)

Table 40 (continued) WLAN current consumption - 2.4/5 GHz

Mode	Output power	Band	Typical current at TA = +25°C		Unit
			VBAT = 3.3 V	VDDIO = 1.8 V	
CRS[19]	–	5 GHz	39.9	0.79	mA
Calibration					
Peak calibration current	_	2.4 GHz	354.3	7.5	mA
Peak calibration current	_	5 GHz	493.2	7.3	mA

1) REG_ON, is LOW.
2) Idle, not associated or inter-beacon.
3) Beacon Interval = 102.4 ms. Beacon duration = 1 ms at 1 Mbps. Average current over 20x DTIM intervals.
4) Beacon interval = 102.4 ms. Beacon duration = 300 µs at 6 Mbps. Average current over 20x DTIM intervals.
5) All the active current measurements are done with CPU clock frequency of 96MHz
6) Output power at chip port = 22.5 dBm.
7) Duty cycle is 100%.
8) Output power at chip port = 22.0 dBm.
9) Output power at chip port = 21.5 dBm
10) Output power at chip port = 19.5 dBm.
11) Output power at chip port = 19.0 dBm
12) Output power at chip port = 18.0 dBm.
13) Output power at chip port = 21.0 dBm.
14) Output power at chip port = 20.0 dBm
15) Output power at chip port = 18.5 dBm.
16) Output power at chip port = 17.5 dBm
17) Output power at chip port = 16.5 dBm.
18) Duty cycle 100%. Carrier sense (CS) detect/packet receive.
19) Carrier sense (CCA) when no carrier is present.

15.2 WLAN current consumption - 6 GHz

***Note**: The values in Table 41 are with the M33 MCU core in deep sleep.*

Table 41 WLAN Current Consumption – 6 GHz

Mode	Bandwidth (MHz)	Band (GHz)	Vbat = 3.3 V	Vi_o = 1.8 V [1]	Unit
Sleep Modes					
OFF [2]	–	–	0.27	0.47	µA
Sleep [3]	–	–	76	9	µA
IEEE power save, DTIM 1 [4]	20.0	6-UNII5	521	23.8	µA
IEEE power save, DTIM 3[4]	20.0	6-UNII5	230	13.3	µA
IEEE power save, DTIM 10[4]	20.0	6-UNII5	126	10.0	µA

(table continues...)

Table 41 (continued) WLAN Current Consumption – 6 GHz

Mode	Bandwidth (MHz)	Band (GHz)	Vbat = 3.3 V	Vi_o = 1.8 V [1]	Unit
IEEE power save, DTIM 1 [4]	20.0	6-UNII6	523	24.1	µA
IEEE power save, DTIM 3 [4]	20.0	6-UNII6	232	13.3	µA
IEEE power save, DTIM 10 [4]	20.0	6-UNII6	126	10.0	µA
IEEE power save, DTIM 1 [4]	20.0	6-UNII7	528	24.1	µA
IEEE power save, DTIM 3 [4]	20.0	6-UNII7	234	13.3	µA
IEEE power save, DTIM 10 [4]	20.0	6-UNII7	127	10.5	µA
IEEE power save, DTIM 1 [4]	20.0	6-UNII8	532	24.1	µA
IEEE power save, DTIM 3 [4]	20.0	6-UNII8	232	13.3	µA
IEEE power save, DTIM 10 [4]	20.0	6-UNII8	127	10.5	µA
Active modes [5]					
Transmit					
6 Mbps [6] ,[7] ,[8]	20	6-UNII-5	282.70	2.1	mA
24 Mbps [6] , [7] , [8]	20	6-UNII-5	324.40	2.0	mA
OFDM - BPSK, R = 1/2 (HE0NSS1) [6] , [7] , [8])	20	6-UNII-5	295.60	2.1	mA
OFDM - 64QAM, R = 5/6 (HE7NSS1) [6] , [7] , [9])	20	6-UNII-5	312.80	2.1	mA
OFDM - 256QAM, R=3/4 (HE8NSS1) [6] , [7] , [13]	20	6-UNII-5	294.70	2.1	mA
OFDM - 256QAM, R=5/6 (HE9NSS1) [6] , [7] ,[10]	20	6-UNII-5	276.40	2.1	mA

(table continues...)

Table 41 (continued) WLAN Current Consumption – 6 GHz

Mode	Bandwidth (MHz)	Band (GHz)	Vbat = 3.3 V	Vi_o = 1.8 V [1]	Unit
OFDM - 1024QAM, R=3/4 (HE10NSS1) [6], [7], [11]	20	6-UNII-5	263.10	2.1	mA
OFDM - 1024QAM, R=5/6 (HE11NSS1) [6], [7], [11]	20	6-UNII-5	263.40	2.1	mA
6 Mbps [6], [7], [8]	20	6-UNII-6	311.60	2.1	mA
24 Mbps [6], [7], [8]	20	6-UNII-6	354.12	2.1	mA
OFDM - BPSK, R = 1/2 (HE0NSS1) [6], [7], [8]	20	6-UNII-6	325.00	2.1	mA
OFDM - 64QAM, R = 5/6 (HE7NSS1) [6], [7], [12]	20	6-UNII-6	333.90	2.1	mA
OFDM - 256QAM, R=3/4 (HE8NSS1) [6], [7], [13]	20	6-UNII-6	324.40	2.1	mA
OFDM - 256QAM, R=5/6 (HE9NSS1) [6], [7], [10]	20	6-UNII-6	305.90	2.1	mA
OFDM - 1024QAM, R=3/4 (HE10NSS1)[6], [7], [11]	20	6-UNII-6	292.70	2.1	mA
OFDM - 1024QAM, R=5/6 (HE11NSS1) [6], [7], [11]	20	6-UNII-6	292.10	2.1	mA
6 Mbps [6], [7], [14]	20	6-UNII-7	283.10	2.1	mA
24 Mbps [6], [7], [14]	20	6-UNII-7	320.80	2.0	mA
OFDM - BPSK, R = 1/2 (HE0NSS1) [6], [7], [14]	20	6-UNII-7	295.20	2.1	mA

(table continues...)

Table 41 (continued) WLAN Current Consumption – 6 GHz

Mode	Bandwidth (MHz)	Band (GHz)	Vbat = 3.3 V	Vi_o = 1.8 V [1]	Unit
OFDM - 64QAM, R = 5/6 (HE7NSS1) [6], [7], [13]	20	6-UNII-7	303.70	2.1	mA
OFDM - 256QAM, R=3/4 (HE8NSS1)[6], [7], [15]	20	6-UNII-7	295.00	2.1	mA
OFDM - 256QAM, R=5/6 (HE9NSS1) [6], [7], [16]	20	6-UNII-7	280.10	2.1	mA
OFDM - 1024QAM, R=3/4 (HE10NSS1) [6], [7], [11]	20	6-UNII-7	274.00	2.1	mA
OFDM - 1024QAM, R=5/6 (HE11NSS1) [6], [7], [11]	20	6-UNII-7	273.70	2.1	mA
6 Mbps [6], [7], [14]	20	6-UNII-8	290.30	2.1	mA
24 Mbps [6], [7], [14]	20	6-UNII-8	330.50	2.0	mA
OFDM - BPSK, R = 1/2 (HE0NSS1) [6], [7], [14]	20	6-UNII-8	301.80	2.1	mA
OFDM - 64QAM, R = 5/6 (HE7NSS1) [6], [7], [15]	20	6-UNII-8	300.70	2.1	mA
OFDM - 256QAM, R=3/4 (HE8NSS1)[6], [7], [16]	20	6-UNII-8	286.10	2.1	mA
OFDM - 256QAM, R=5/6 (HE9NSS1) [6], [7], [11]	20	6-UNII-8	272.20	2.1	mA
OFDM - 1024QAM, R=3/4 (HE10NSS1)[6], [7], [17]	20	6-UNII-8	260.80	2.1	mA

(table continues...)

Table 41 (continued) WLAN Current Consumption – 6 GHz

Mode	Bandwidth (MHz)	Band (GHz)	Vbat = 3.3 V	Vi_o = 1.8 V [1]	Unit
OFDM - 1024QAM, R=5/6 (HE11NSS1) [6], [7], [17]	20	6-UNII-8	260.90	2.1	mA
Receive					
6 Mbps [7]	20	6-UNII-5	43.1	0.79	mA
24 Mbps [7]	20	6-UNII-5	43.3	0.79	mA
OFDM - BPSK, R = 1/2 (HE0NSS1) [7]	20	6-UNII-5	44.6	0.79	mA
OFDM - 64QAM, R = 5/6 (HE7NSS1) [7]	20	6-UNII-5	45	0.79	mA
OFDM - 256QAM, R=3/4 (HE8NSS1)	20	6-UNII-5	45.4	0.79	mA
OFDM - 256QAM, R=5/6 (HE9NSS1) [7]	20	6-UNII-5	45.3	0.79	mA
OFDM - 1024QAM, R=3/4 (HE10NSS1)	20	6-UNII-5	45.7	0.79	mA
OFDM - 1024QAM, R=5/6 (HE11NSS1) [7]	20	6-UNII-5	45.7	0.79	mA
CRS [18]	20	6-UNII-5	41.7	0.79	mA
6 Mbps [7]	20	6-UNII-6	43.9	0.79	mA
24 Mbps [7]	20	6-UNII-6	43.7	0.79	mA
OFDM - BPSK, R = 1/2 (HE0NSS1) [7]	20	6-UNII-6	44.9	0.79	mA
OFDM - 64QAM, R = 5/6 (HE7NSS1) [7]	20	6-UNII-6	45.4	0.79	mA
OFDM - 256QAM, R=3/4 (HE8NSS1)	20	6-UNII-6	45.7	0.79	mA
OFDM - 256QAM, R=5/6 (HE9NSS1) [7]	20	6-UNII-6	45.6	0.79	mA
OFDM - 1024QAM, R=3/4 (HE10NSS1)	20	6-UNII-6	46	0.79	mA

(table continues...)

Table 41 (continued) WLAN Current Consumption – 6 GHz

Mode	Bandwidth (MHz)	Band (GHz)	Vbat = 3.3 V	Vi_o = 1.8 V [1]	Unit
OFDM - 1024QAM, R=5/6 (HE11NSS1) [7], [13]	20	6-UNII-6	45.9	0.79	mA
CRS [18]	20	6-UNII-6	42	0.79	mA
6 Mbps [7]	20	6-UNII-7	44.4	0.79	mA
24 Mbps [7]	20	6-UNII-7	44.7	0.79	mA
OFDM - BPSK, R = 1/2 (HE0NSS1)	20	6-UNII-7	45.9	0.79	mA
OFDM - 64QAM, R = 5/6 (HE7NSS1) [7]	20	6-UNII-7	46.4	0.79	mA
OFDM - 256QAM, R=3/4 (HE8NSS1)	20	6-UNII-7	46.7	0.79	mA
OFDM - 256QAM, R=5/6 (HE9NSS1) [7]	20	6-UNII-7	46.6	0.79	mA
OFDM - 1024QAM, R=3/4 (HE10NSS1)	20	6-UNII-7	47	0.79	mA
OFDM - 1024QAM, R=5/6 (HE11NSS1) [7]	20	6-UNII-7	47	0.79	mA
CRS [18]	20	6-UNII-7	43	0.79	mA
6 Mbps [7]	20	6-UNII-8	45	0.79	mA
24 Mbps [7]	20	6-UNII-8	45.3	0.79	mA
OFDM - BPSK, R = 1/2 (HE0NSS1) [7]	20	6-UNII-8	46.5	0.79	mA
OFDM - 64QAM, R = 5/6 (HE7NSS1) [7]	20	6-UNII-8	46.9	0.79	mA
OFDM - 256QAM, R=3/4 (HE8NSS1)	20	6-UNII-8	47.3	0.79	mA
OFDM - 256QAM, R=5/6 (HE9NSS1) [7]	20	6-UNII-8	47.2	0.79	mA
OFDM - 1024QAM, R=3/4 (HE10NSS1)	20	6-UNII-8	47.7	0.79	mA

(table continues...)

Table 41 (continued) WLAN Current Consumption – 6 GHz

Mode	Bandwidth (MHz)	Band (GHz)	Vbat = 3.3 V	Vi_o = 1.8 V [1)]	Unit
OFDM - 1024QAM, R=5/6 (HE11NSS1) [7)]	20	6-UNII-8	47.7	0.79	mA
CRS [18)]	20	6-UNII-8	43.6	0.79	mA
Calibration					
Peak Calibration Current	20	6-UNII-5	422.2	7.1	mA
Peak Calibration Current	20	6-UNII-6	440.7	6.8	mA
Peak Calibration Current	20	6-UNII-7	515.7	7.0	mA
Peak Calibration Current	20	6-UNII-8	346.9	7.5	mA

1) Specified with all pins idle (not switching) and not driving any loads.
2) REG_ON is low.
3) Idle, not associated, or inter-beacon.
4) Beacon Interval = 102.4 ms. Beacon duration = 300 µs @ 6 Mbps. Average current over 20x DTIM intervals.
5) All the active current measurements are done with CPU clock frequency of 96MHz
6) Duty cycle is 100%.
7) Measured using Packet engine test mode.
8) Output power per core at chip port = 19.5 dBm.
9) Output power per core at chip port = 18.5 dBm.
10) Output power per core at chip port = 16.5 dBm.
11) Output power per core at chip port = 15.5 dBm
12) Output power per core at chip port = 18.0 dBm
13) Output power per core at chip port = 17.5 dBm
14) Output power per core at chip port = 19.0 dBm
15) Output power per core at chip port = 17.0 dBm
16) Output power per core at chip port = 16.0 dBm
17) Output power per core at chip port = 14.5 dBm.
18) Carrier sense (CCA) when no carrier is present, measured in IFS interval during active Rx.

15.3 Bluetooth® current consumption

Bluetooth® Low Energy current consumption measurements are shown in Table 42.

Note:
- *The Bluetooth® LE current consumption numbers are measured based on BLE GFSK TX output power = 13 dBm and the Tx output power for the low-power-Tx path mentioned in Table 42 and Table 43 equal to 4 dBm*
- *The WLAN core is put in reset for all measurements provided in Table 42*

Table 42 Bluetooth® LE current consumption

Operating mode	VBAT (VBAT = 3.3 V) typical	VDDIO (VDDIO = 1.8 V) typical	Unit
Sleep	31.2	8.8	µA

(table continues...)

Table 42 (continued) Bluetooth® LE current consumption

Operating mode	VBAT (VBAT = 3.3 V) typical	VDDIO (VDDIO = 1.8 V) typical	Unit
Bluetooth® LE scan	160.0	12.4	µA
Bluetooth® LE non connectable 1.28 s ADV (3-channels)	74.0	10.0	µA
Bluetooth® LE non connectable 1.28 s ADV (3-channels) (low-power TX path)	67.0	10.0	µA
Bluetooth® LE 300 ms connected peripheral	160.3	14.0	µA
Bluetooth® LE 300 ms connected peripheral +4 dBm (low-power TX path)	153.7	14.0	µA
Bluetooth® LE 1 s connected peripheral	78.7	10.3	µA
Transmit packet current - LE	32.1	0.3	mA
Receive packet current - LE	11.2	0.3	mA

Table 43 Bluetooth® LE current consumption (TX19 High power Tx path)

Operating Mode	VBAT (VBAT = 3.3V) Typical	VDDIO (VDDIO = 1.8V) Typical	Unit
Sleep	31.2	8.78	µA
Bluetooth® LE scan (Passive, Scan Int:1.28 sec, Scan Window :11.25 ms)	160.0	12.4	µA
Bluetooth® LE non-connectable 1.28 sec ADV (3 Channels)	111.1	10.0	µA
Bluetooth® LE 300 ms connected peripheral	181.7	13.9	µA
Bluetooth® LE 1 sec connected peripheral	84.8	10.3	µA
Transmit packet current - LE	130.0	0.3	mA
Receive packet current - LE	11.2	0.3	mA

Table 44 Connected MCU Current Consumption

M33 CPU Modes	VBAT=3.3 V	VDDIO=1.8 V	BLE	WLAN	Conditions	Unit
Deep Sleep	34.45	9.35	Deep Sleep	OFF	-	µA

(table continues...)

Table 44 (continued) Connected MCU Current Consumption

M33 CPU Modes	VBAT=3.3 V	VDDIO=1.8 V	BLE	WLAN	Conditions	Unit
Deep Sleep	32.50	9.35	Not initialized	OFF	-	µA
192 MHz [1)]	12.31	0.28	Not initialized	OFF	VCO = 384 MHz, VBAT = 3.3V and VDDIO = 1.8V	mA
96 MHz	9.30	0.26				mA
48 MHz	7.20	0.24				mA
96 MHz [2)]	8.14	0.24	Not initialized	OFF	VCO = 192 MHz, VBAT = 3.3 V, and VDDIO = 1.8 V	mA
48 MHz[2)]	6.07	0.22				mA

1) To run Connected MCU at 192 MHz, VCO has to be set at 384 MHz, VCO settings cannot be changed in run time.
2) BLE needs CPU clock to be 48 MHz or higher.

16 Interface timing and AC characteristics

16.1 SDIO timing

16.1.1 SDIO default mode timing

SDIO default mode timing is shown by the combination of Figure 25 and Table 45.

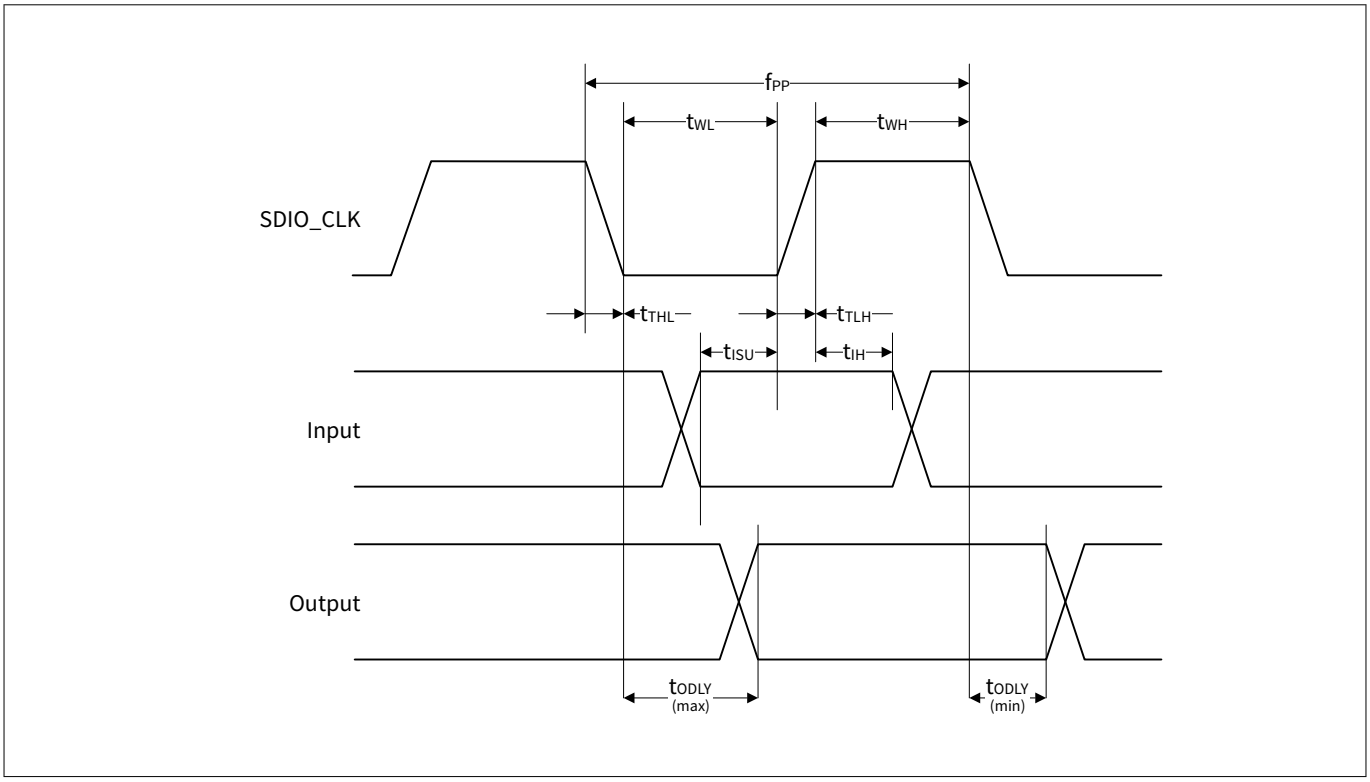


Figure 25 SDIO bus timing (default mode)

Table 45 SDIO bus timing parameters (default mode)

Parameter	Symbol	Min	Typ	Max	Unit
SDIO CLK (all values are referred to minimum VIH and maximum VIL[1])					
Frequency – Data transfer mode	f_{PP}	0	–	25.0	MHz
Frequency – Identification mode	f_{OD}			400	kHz
Clock low time	t_{WL}	10.0		–	ns
Clock high time	t_{WH}				
Clock rise time	t_{TLH}	–		10.0	
Clock low time	t_{THL}				
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	5.0	–	–	ns
Input hold time	t_{IH}				

(table continues...)

Table 45 (continued) SDIO bus timing parameters (default mode)

Parameter	Symbol	Min	Typ	Max	Unit
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data transfer mode	t_{ODLY}	0	–	14.0	ns
Output delay time – Identification mode	t_{ODLY}			50.0	

1) Min (Vih) = 0.7 × VDDIO and max (Vil) = 0.2 × VDDIO.

***Note**: Timing is based on CL ≤ 40 pF load on CMD and data.*

16.1.2 SDIO High-speed (HS) mode timing

SDIO High-speed mode timing is shown by the combination of Figure 26 and Table 46.

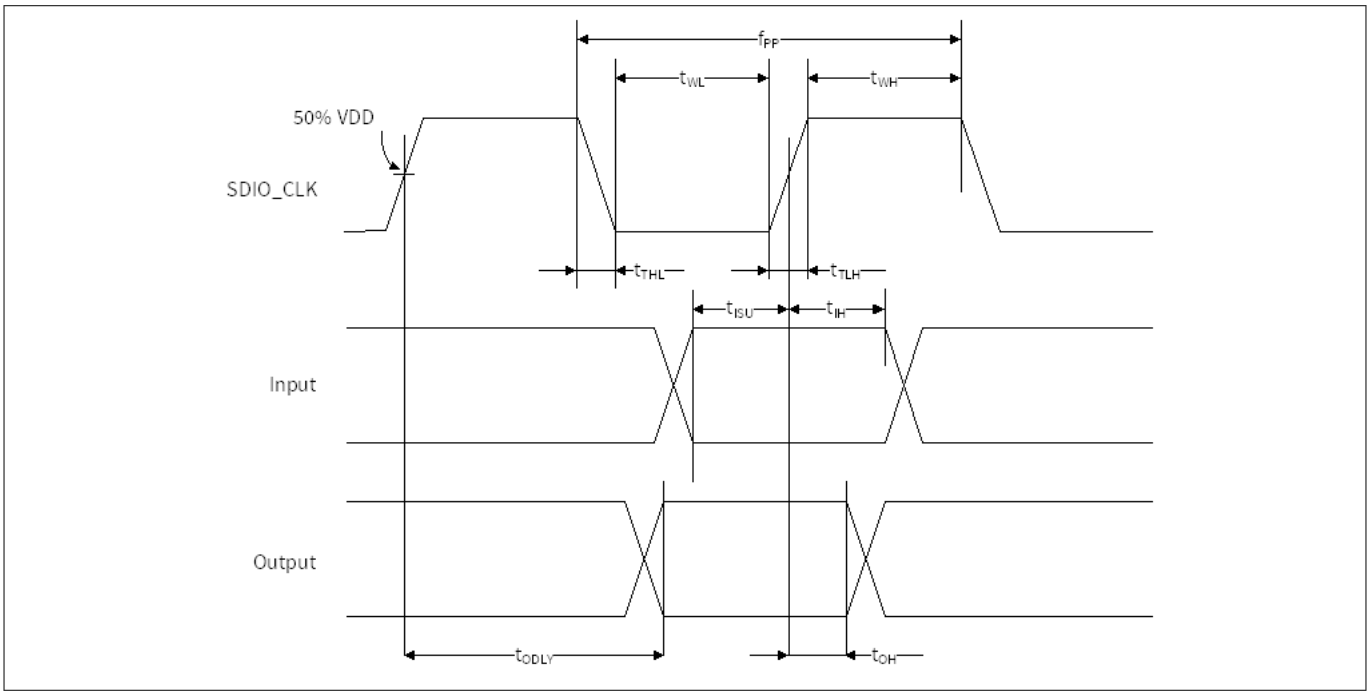


Figure 26 SDIO bus timing (HS mode)

Table 46 SDIO bus timing parameters (HS mode)

Parameter	Symbol	Min	Typ	Max	Unit
SDIO CLK (all values are referred to minimum VIH and maximum VIL[1)])					
Frequency – Data transfer mode	f_{PP}	0	–	50	MHz
Frequency – Identification mode	f_{OD}			400	kHz
Clock low time	t_{WL}	7.0		–	ns
Clock high time	t_{WH}				
Clock rise time	t_{TLH}	–		3.0	
Clock low time	t_{THL}				

(table continues...)

Table 46 (continued) SDIO bus timing parameters (HS mode)

Parameter	Symbol	Min	Typ	Max	Unit
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	6.0	–	–	ns
Input hold time	t_{IH}	2.0			
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data transfer mode	t_{ODLY}	–	–	14.0	ns
Output hold time	t_{OH}	2.5.0		–	
Total system capacitance (each line)	CL	–		40.0	pF

1) Min (Vih) = 0.7 × VDDIO and max (Vil) = 0.2 × VDDIO.

***Note**: Timing is based on CL ≤ 40 pF load on CMD and data.*

16.1.3 SDIO bus timing specifications in SDR modes

Clock timing

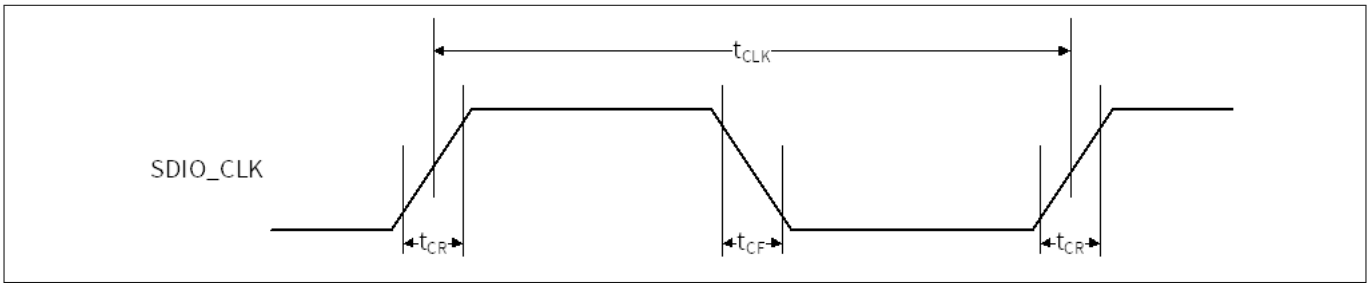


Figure 27 SDIO clock timing (SDR modes)

Table 47 SDIO bus clock timing parameters (SDR modes)

Parameter	Symbol	Min	Max	Unit	Comments
–	t_{CLK}	40.0	–	ns	SDR12 mode
		20.0			SDR25 mode
		10.0			SDR50 mode
–	t_{CR}, t_{CF}	–	0.2 × t_{CLK}	ns	t_{CR}, t_{CF} < 2.00 ns (max) @100 MHz, C_{CARD} = 10 pF t_{CR}, t_{CF} < 0.96 ns (max) @208 MHz, C_{CARD} = 10 pF
Clock duty	–	30.0	70.0	%	–

Device input timing

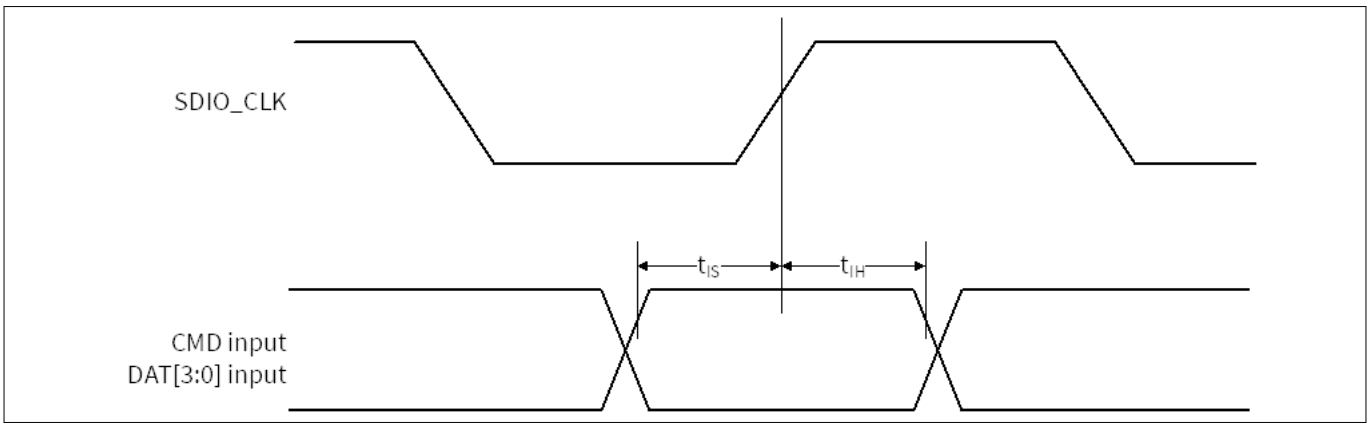


Figure 28 SDIO bus input timing (SDR modes)

Table 48 SDIO bus input timing parameters (SDR modes)

Symbol	Min	Max	Unit	Comments
SDR50 mode				
t_{IS}	3.00	–	ns	C_{CARD} = 10 pF, VCT = 0.975 V
t_{IH}	0.80			C_{CARD} = 5 pF, VCT = 0.975 V

Device output timing

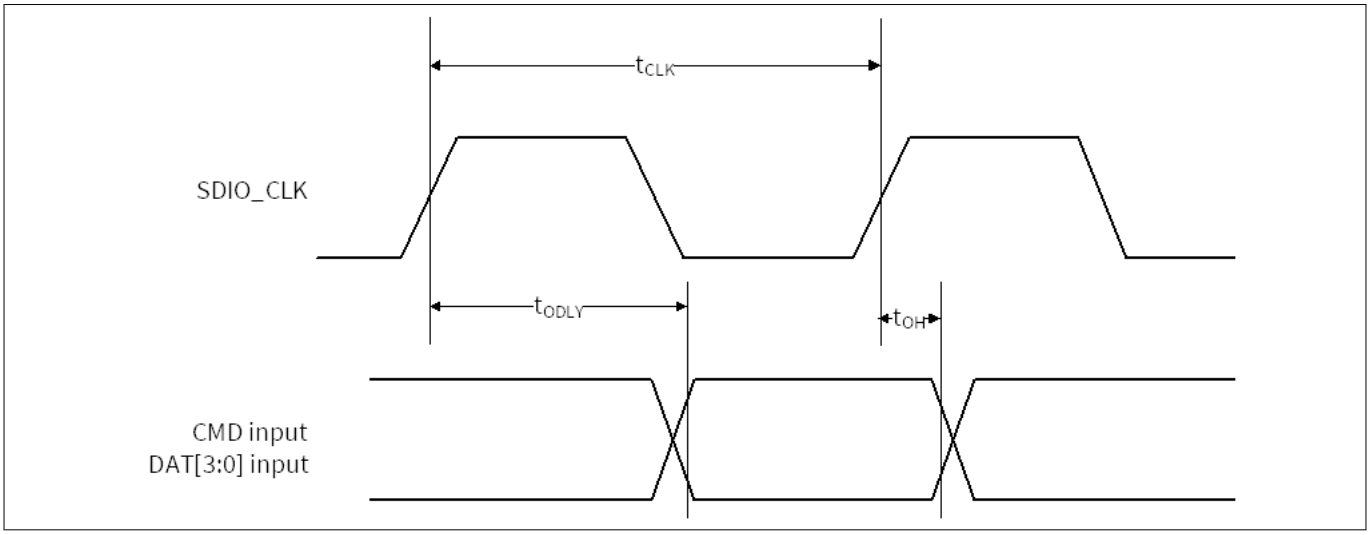


Figure 29 SDIO bus output timing (SDR modes up to 100 MHz)

Table 49 SDIO bus output timing parameters (SDR modes up to 100 MHz)

Symbol	Min	Max	Unit	Comments
t_{ODLY}	–	7.5	ns	t_{CLK} ≥ 10 ns C_L= 30 pF using driver type B for SDR50
t_{ODLY}		14.0		t_{CLK} ≥ 20 ns C_L= 40 pF using for SDR12, SDR25
t_{OH}	1.5	–		Hold time at the t_{ODLY} (min) C_L= 15 pF

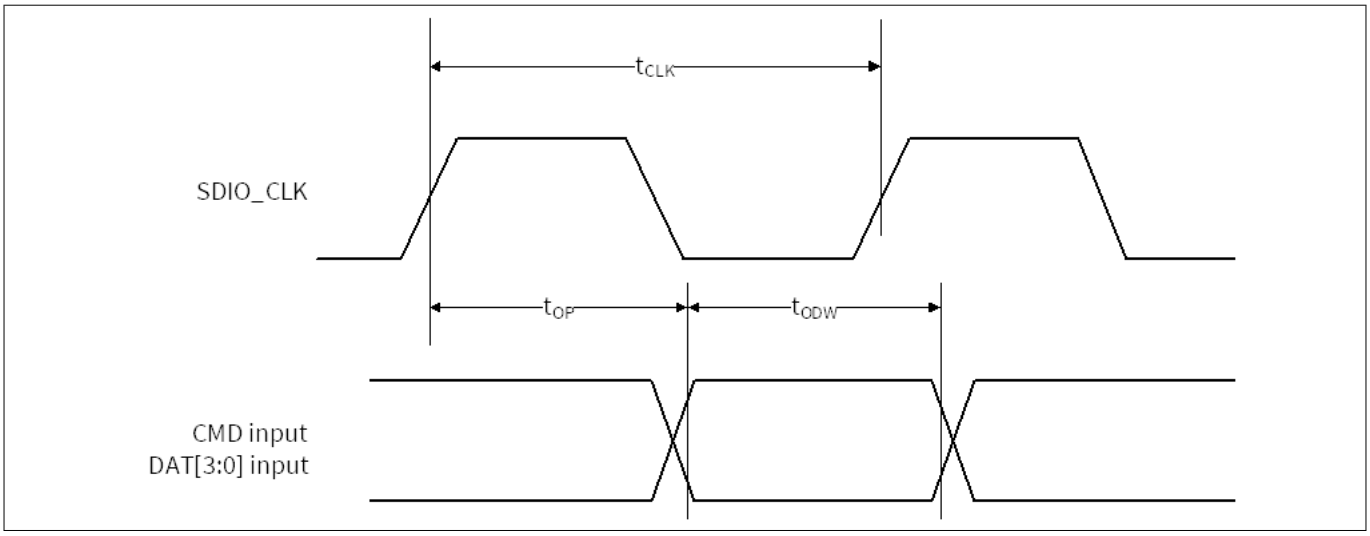


Figure 30 SDIO bus output timing (SDR modes 100 MHz to 208 MHz)

16.1.4 SDIO bus timing specifications in DDR50 mode

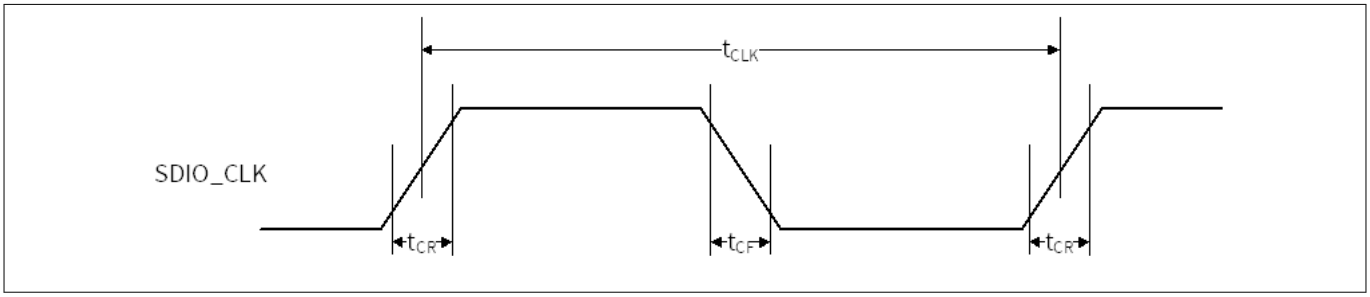


Figure 31 SDIO clock timing (DDR50 mode)

Table 50 SDIO bus clock timing parameters (DDR50 mode)

Parameter	Symbol	Min	Max	Unit	Comments
–	t_{CLK}	20.0	–	ns	DDR50 mode
	t_{CR},t_{CF}	–	0.2 × t_{CLK}		t_{CR}, t_{CF} < 4.00 ns (max) @50 MHz, C_{CARD} = 10 pF
Clock duty	–	45.0	55.0	%	–

Data timing, DDR50 mode

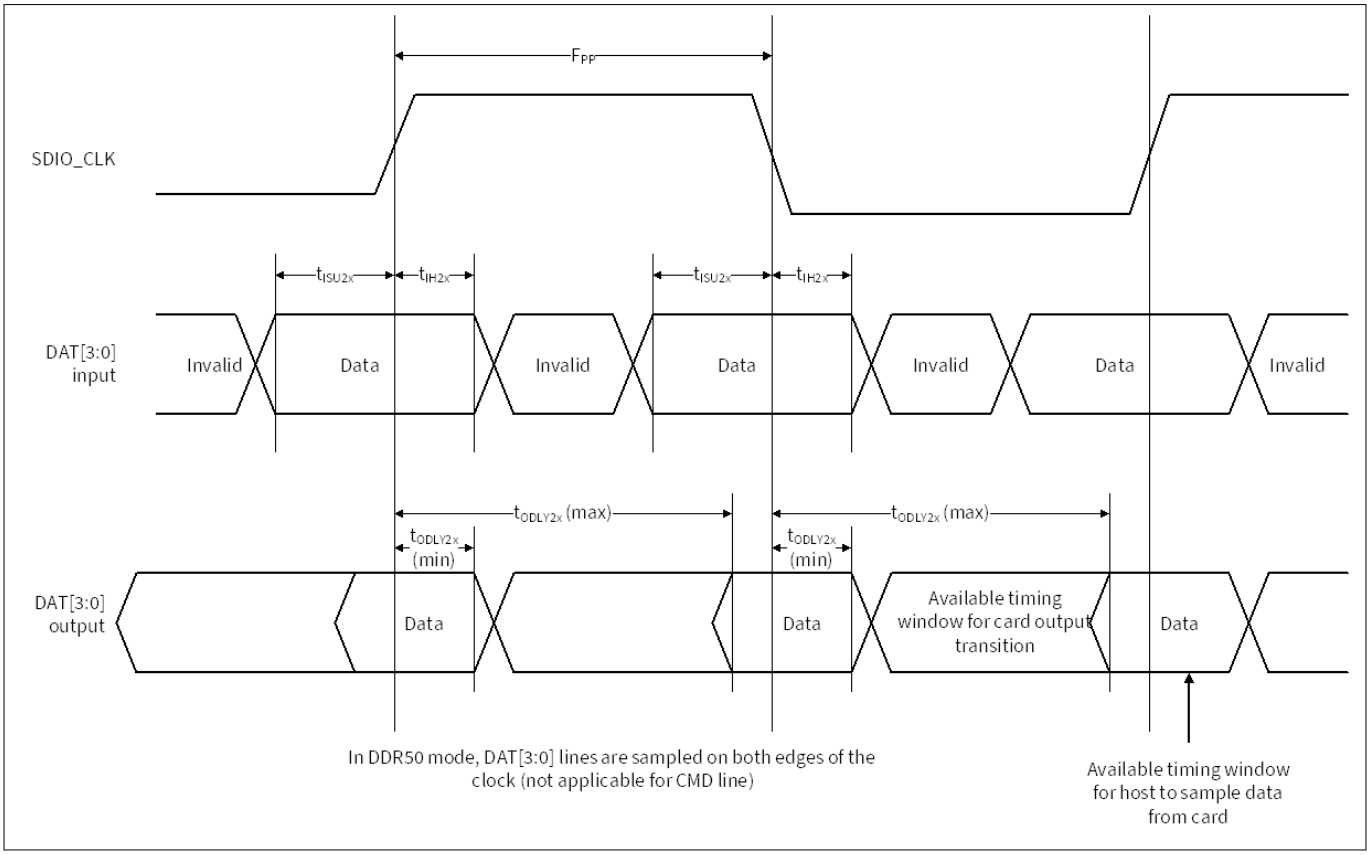


Figure 32 SDIO data timing (DDR50 mode)

Table 51 SDIO bus timing parameters (DDR50 mode)

Parameter	Symbol	Min	Max	Unit	Comments
Input CMD					
Input setup time	t_{ISU}	6.0	–	ns	C_{CARD} < 10 pF (1 Card)
Input hold time	t_{IH}	0.8			
Output CMD					
Output delay time	t_{ODLY}	–	13.7	ns	C_{CARD} < 30 pF (1 Card)
Output hold time	t_{OH}	1.5	–		C_{CARD} < 15 pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3.0	–	ns	C_{CARD} < 10 pF (1 Card)
Input hold time	t_{IH2x}	0.8			
Output DAT					
Output delay time	t_{ODLY2x}	–	7.5	ns	C_{CARD} < 25 pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	–		C_{CARD} < 15 pF (1 Card)

16.2 ΔΣ-ADC and low-power comparator

Table 52 ADC and low-power comparator

Parameter	Conditions	Min	Typ	Max	Unit
Analog supply voltage	External switching regulator	1.71	1.8	1.89	V
	Internal LDO	0.95	1.0	1.05	
Digital supply voltage		0.95	1.0	1.05	
Operating temperature	Die temperature	-40	25	125	°C
Current consumption	Total LPCOMPs and ADC	–	50	–	µA
Power down current	–		300		nA
Input multiplexer					
GPIO<7:0>	DC input signals	0	_	1	V
MIC	AC input signal through bypassing cap	-500	_	+500	mV
Low power comparator(LPCOMP)					
DC gain	Output is connected to negative input while positive input is shorted to VCM	–	120	–	dB
Input impedance	DC coupled	–	∞	–	–
	AC coupled	–	800	–	KΩ
Input referred mismatch	Output is connected to INP(-) INP(+) is shorted to VCM	–	851	–	mV
Input common mode	Voltage common mode (VCM), AC coupled	–	400	–	mV
Comparator ready	i_PD_LPCOMP_1 P8 = 0 at T = 0 s	–	25	–	ms
Propagation delay	Overdrive voltage = VCM ±0.25 mV	–	4	–	ms

(table continues...)

Table 52 (continued) ADC and low-power comparator

Parameter	Conditions	Min	Typ	Max	Unit
Noise threshold range	Comparator hysteresis window	0	_	60	mV
Noise threshold step	Comparator hysteresis adjustment step	_	4	_	mV
ADC					
ADC ready	i_PD_ADC_1P8 = 0 at T = 0 s	–	100	–	ms
Input clock frequency	i_ADC_CLK_IN_DIV2_Ctrl = 0	1024	–	2048	kHz
	i_ADC_CLK_IN_DIV2_Ctrl = 1	2048		4096	
	Duty cycle (÷2 = 0/1)	49.9/45	50.0	50.1/55	%
Sampling frequency		1024	–	2048	kHz
Input full scale	DC coupled	0	–	1	V
	AC coupled	–	1	–	Vpp
Input impedance	–		375		KΩ
Input common mode	Voltage common mode (VCM)		500		mV
Input bandwidth	DC mode/NTD mode	0/*	–	8000	Hz
Startup time	Output is within 0.5 dB	–		2	ms
PGA gain range	–	1		8	Linear
System gain error	NTD mode (@ 1 kHz)	–1	–	+1	dB
MIC bias	Directly/ unbuffered from 1.8 V supply	–	1.8	–	V

16.3 Serial memory interface specifications

Table 53 Serial memory interface specifications

Parameter	Conditions	Units	Min	Typ	Max	Mode
SMIF QSPI output clock frequency	–	MHz	–	–	96	SDR

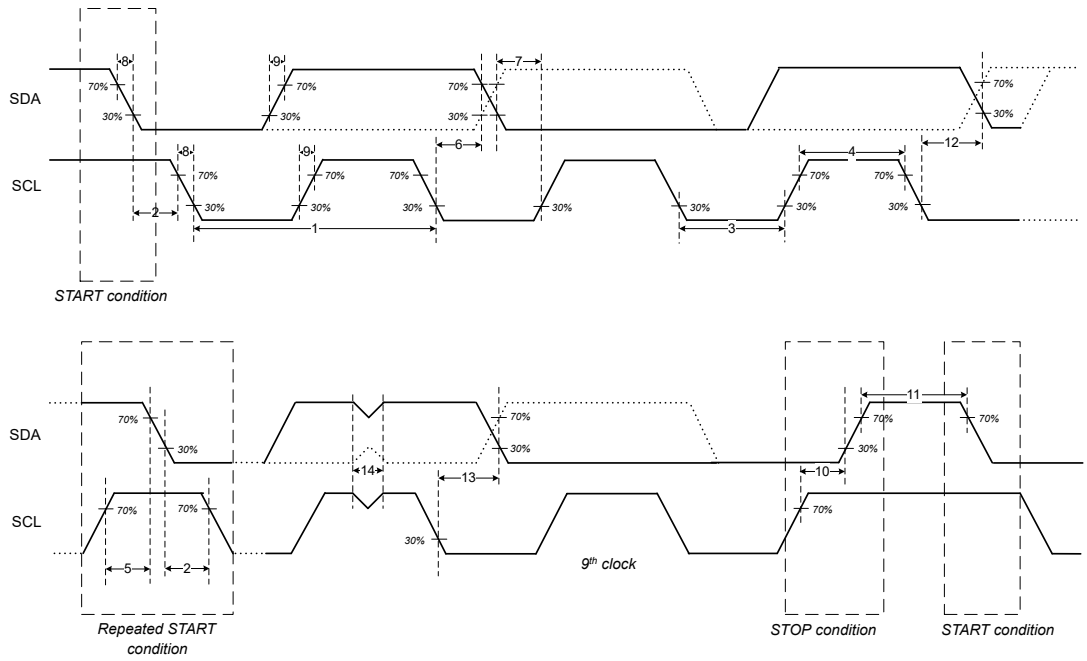
(table continues...)

Table 53 (continued) Serial memory interface specifications

Parameter	Conditions	Units	Min	Typ	Max	Mode
SMIF QSPI output clock frequency					75	DDR
SDR mode						
SDR_TCSH0 (CS# active hold to CK)	8 mA/10 mA/12 mA IO drives supported Input transition of data from flash 1.5 ns (max/min) C_L = 15 pF hys_en = 0 No delay line + inverted clock mode supported SELECT_SETUP_DELAY = 1, SELECT_HOLD_DELAY = 1 to meet chip select timing	ns	5	–	–	–
SDR_TCSS0 (CS# active setup to CK)						
SDR_TOUT_ SETUP_LF (Output setup time of DQ[3:0] to CK HIGH)			2			
SDR_TOUT_ HOLD_LF (Output hold time of DQ[3:0] to CK HIGH)			3			
SDR_TIN_V (CK low to DQ[3:0] input valid time)			–		7	
SDR_TIN_HO (CK low to DQ[3:0] input hold time)			0		–	
DDR mode						
DDR_TCSH0 (CS# active hold to CK)	8 mA/10 mA/12 mA IO drives supported Input transition of Data from flash 1.5 ns (max/min) C_L = 17 pF hys_en = 0 No delay line + Inverted clock mode supported SELECT_SETUP_DELAY = 1, SELECT_HOLD_DELAY = 1 to meet chip select timing	ns	5	–	–	–
DDR_TCSS0 (CS# active setup to CK)						
DDR_TOUT_ SETUP_LF (Output setup time of DQ[3:0] to CK HIGH/LOW)			1.5			
DDR_TOUT_ HOLD_LF (Output hold time of DQ[3:0] to CK HIGH/LOW)						
DDR_TIN_V (CK LOW/HIGH to DQ[3:0] input valid time)			–			
DDR_TIN_HO (CK LOW/HIGH to DQ[3:0] input hold time)			1			

16.4 Serial communication block (SCB) specifications

16.4.1 I2C specifications



1: SCL clock period = $1/f_{SCL}$
2: Hold time, START condition = $t_{HD;STA}$
3: LOW period of SCL = t_{LOW}
4: HIGH period of SCL = t_{HIGH}
5: Setup time for a repeated START = $t_{SU;STA}$
6: Data hold time, for receiver = $t_{HD;DAT}$
7: Data setup time = $t_{SU;DAT}$
8: Fall time of SCL and SDA = t_F
9: Rise time of SCL and SDA = t_R
10: Setup time for STOP = $t_{SU;STO}$
11: Bus-free time between START and STOP = t_{BUF}
12: Time for data signal from SCL LOW to SDA output = $t_{VD;DAT}$
13: Data valid acknowledge time = $t_{VD;ACK}$
14: Pulse width of spikes that must be suppressed by the input filter = t_{SP}

Figure 33 I2C specifications

Table 54 I2C specifications

Parameter	Description	Min	Typ	Max	Units
I2C Interface-Standard-mode					
fSCL	SCL clock frequency	–	–	100	kHz
tHD;STA	Hold time, START condition	4000	–	–	ns
tLOW	Low period of SCL	4700	–	–	ns

(table continues...)

Table 54 (continued) I2C specifications

Parameter	Description	Min	Typ	Max	Units
tHIGH	High period of SCL	4000	–	–	ns
tSU;STA	Setup time for a repeated START	4700	–	–	ns
tHD;DAT	Data hold time, for receiver	0	–	–	ns
tSU;DAT	Data setup time	250	–	–	ns
t_F	Fall time of SCL and SDA (Input and output)	–	–	300	ns
tSU;STO	Setup time for STOP	4000	–	–	ns
tBUF	Bus-free time between START and STOP	4700	–	–	ns
C_B	Capacitive load for each bus line	–	–	400	pF
tVD;DAT	Time for data signal from SCL LOW to SDA output	–	–	3450	ns
tVD;ACK	Data valid acknowledge time	–	–	3450	ns
fSCB	SCB operating frequency	–	–	100	MHz
I2C Interface-Fast-mode					
fSCL_F	SCL clock frequency	–	–	400	kHz
tHD;STA_F	Hold time, START condition	600	–	–	ns
tLOW_F	Low period of SCL	1300	–	–	ns
tHIGH_F	High period of SCL	600	–	–	ns
tSU;STA_F	Setup time for a repeated START	600	–	–	ns
tHD;DAT_F	Data hold time, for receiver	0	–	–	ns
tSU;DAT_F	Data setup time	100	–	–	ns

(table continues...)

Table 54 (continued) I2C specifications

Parameter	Description	Min	Typ	Max	Units
tF_F	Fall time of SCL and SDA (Detail/ Condition: Input and output, GPIO_ENH: slow mode, 400 pF load)	20 × (VDDD / 5.5)	–	300	ns
tSU;STO_F	Setup time for STOP (Detail/ Condition: Input and output)	600	–	–	ns
tBUF_F	Bus free time between START and STOP	1300	–	–	ns
CB_F	Capacitive load for each bus line	–	–	400	pF
tVD;DAT_F	Time for data signal from SCL LOW to SDA output	–	–	900	ns
tVD;ACK_F	Data valid acknowledge time	–	–	900	ns
tSP_F	Pulse width of spikes that must be suppressed by the input filter	–	–	50	ns
I2C Interface-Fast-Plus mode					
fSCL_FP	SCL clock frequency	–	–	1	MHz
tHD;STA_FP	Hold time, START condition	260	–	–	ns
tLOW_FP	Low period of SCL	500	–	–	ns
tHIGH_FP	High period of SCL	260	–	–	ns
tSU;STA_FP	Setup time for a repeated START	260	–	–	ns

(table continues...)

Table 54 (continued) I2C specifications

Parameter	Description	Min	Typ	Max	Units
tHD;DAT_FP	Data hold time, for receiver	0	–	–	ns
tSU;DAT_FP	Data setup time	50	–	–	ns
tF_FP	Fall time of SCL and SDA (Detail/ Condition: Input and output 20-pF load GPIO_ENH: slow mode)	20 × (VDDD /5.5)	–	160	ns
tSU;STO_FP	Setup time for STOP (Detail/ Condition: Input and output)	260	–	–	ns
tBUF_FP	Bus free time between START and STOP	500	–	–	ns
CB_FP	Capacitive load for each bus line	–	–	20	pF
tVD;DAT_FP	Time for data signal from SCL LOW to SDA output	–	–	450	ns
tVD;ACK_FP	Data valid acknowledge time	–	–	450	ns
tSP_FP	Pulse width of spikes that must be suppressed by the input filter	–	–	50	ns
SPI Interface Master (Full-clock mode: LATE_MISO_SAMPLE = 1) [Conditions: drive_sel<1:0>= 0x]					
fSPI	SPI operating frequency (Detail/ Condition: Do not use half-clock mode: LATE_MISO_SAMP LE = 0)	–	–	12	MHz

(table continues...)

Table 54 (continued) I2C specifications

Parameter	Description	Min	Typ	Max	Units
tDMO	SPI Master: MOSI valid after SCLK driving edge	–	–	15	ns
tDSI	SPI Master: MISO valid before SCLK capturing edge	5	–	–	ns
tHMO	SPI Master: Previous MOSI data hold time	0	–	–	ns
tW_SCLK_H_L	SPI SCLK pulse width HIGH or LOW	–	0.35 * 1/f_{SPI}	–	ns
tDHI	SPI Master: MISO hold time after SCLK capturing edge	0	–	–	ns
tEN_SETUP	SSEL valid, before the first SCK capturing edge (Detail/ Condition: Min is half clock period)	25	–	–	ns
tEN_SHOLD	SSEL hold, after the last SCK capturing edge (Detail/ Condition: Min is half clock period)	0.5 × t_{SCK}	–	–	ns
CSPIM_MS	SPI capacitive load	–	–	20	pF
SPI Interface Slave (internally clocked) [Conditions: drive_sel<1:0>= 0x]					
fSPI_INT	SPI operating frequency	–	–	12	MHz
tDMI_INT	SPI Slave: MOSI Valid before Sclock capturing edge	4	–	–	ns

(table continues...)

Table 54 (continued) I2C specifications

Parameter	Description	Min	Typ	Max	Units
tDSO_INT	SPI Slave: MISO Valid after Sclock driving edge, in the internal-clocked mode	–	–	30	ns
tHSP	SPI Slave: Previous MISO data hold time	5	–	–	ns
tEN_SETUP_INT	SPI Slave: SSEL valid to first SCK valid edge	20	–	–	ns
tEN_HOLD_INT	SPI Slave Select active (LOW) from last SCLK hold	20	–	–	ns
tEN_SET-UP_PRE	SPI Slave: from SSEL valid, to SCK falling edge before the first data bit	20	–	–	ns
tEN_HOLD_PRE	SPI Slave: from SCK falling edge before the first data bit, to SSEL invalid	20	–	–	ns
tEN_SETUP_CO	SPI Slave: from SSEL valid, to SCK falling edge in the first data bit	20	–	–	ns
tEN_HOLD_CO	SPI Slave: from SCK falling edge in the first data bit, to SSEL invalid	20	–	–	ns
tW_DIS_INT	SPI Slave Select inactive time	40	–	–	ns
tW_SCLKH_INT	SPI SCLK pulse width HIGH	20	–	–	ns
tW_SCLKL_INT	SPI SCLK pulse width LOW	20	–	–	ns
tSIH_INT	SPI MOSI hold from SCLK	12	–	–	ns

(table continues...)

Table 54 (continued) I2C specifications

Parameter	Description	Min	Typ	Max	Units
CSPIS_INT	SPI Capacitive Load	–	–	20	pF
SPI Interface Slave (externally clocked) [Conditions: drive_sel<1:0>= 0x]					
fSPI_EXT	SPI operating frequency	–	–	12	MHz
tDMI_EXT	SPI Slave: MOSI Valid before Sclock capturing edge	5	–	–	ns
tDSO_EXT	SPI Slave: MISO Valid after Sclock driving edge, in the external-clocked mode	–	–	32	ns
tHSO_EXT	SPI Slave: Previous MISO data hold time	3	–	–	ns
tEN_SET- UP_EXT	SPI Slave: SSEL valid to first SCK valid edge	40	–	–	ns
tEN_HOLD_EXT	SPI Slave Select active (LOW) from last SCLK hold	40	–	–	ns
tW_DIS_EXT	SPI Slave Select inactive time	80	–	–	ns
tW_SCLKH_EXT	SPI SCLK pulse width HIGH	34	–	–	ns
tW_SCLKL_EXT	SPI SCLK pulse width LOW	34	–	–	ns
tSIH_EXT	SPI MOSI hold from SCLK	20	–	–	ns
CSPIS_EXT	SPI Capacitive Load	–	–	10	pF
tVSS_EXT	SPI Slave: MISO valid after SSEL falling edge (CPHA = 0)	–	–	33	ns
fBPS	Data rate	–	–	10	Mbps

16.4.2 SPI interface master

Table 55 SPI interface master

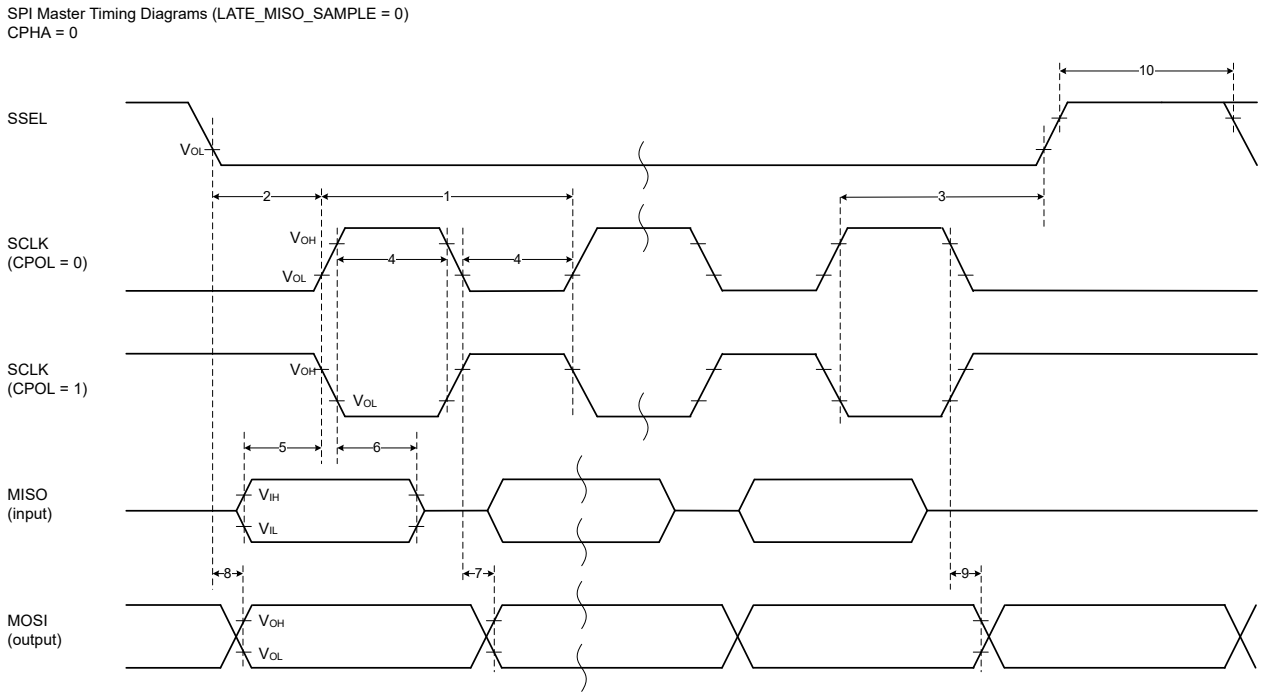
Parameter	Description	Min	Typ	Max	Units
(Full-clock mode: LATE_MISO_SAMPLE = 1) [Conditions: drive_sel<1:0>= 0x]					
fSPI	SPI operating frequency (Detail/Condition: Do not use half-clock mode: LATE_MISO_SAMP LE = 0)	–	–	12	MHz
tDMO	SPI Master: MOSI valid after SCLK driving edge	–	–	15	ns
tDSI	SPI Master: MISO valid before SCLK capturing edge	5	–	–	ns
tHMO	SPI Master: Previous MOSI data hold time	0	–	–	ns
tW_SCLK_H_L	SPI SCLK pulse width HIGH or LOW	–	0.35 * $1/f_{SPI}$	–	ns
tDHI	SPI Master: MISO hold time after SCLK capturing edge	0	–	–	ns
tEN_SETUP	SSEL valid, before the first SCK capturing edge (Detail/Condition: Min is half clock period)	25	–	–	ns
tEN_SHOLD	SSEL hold, after the last SCK capturing edge (Detail/Condition: Min is half clock period)	0.5 × t_{SCK}	–	–	ns
CSPIM_MS	SPI capacitive load	–	–	20	pF
SPI Interface Slave (internally clocked) [Conditions: drive_sel<1:0>= 0x]					
fSPI_INT	SPI operating frequency	–	–	12	MHz
tDMI_INT	SPI Slave: MOSI Valid before Sclock capturing edge	4	–	–	ns
tDSO_INT	SPI Slave: MISO Valid after Sclock driving edge, in the internal-clocked mode	–	–	30	ns
tHSP	SPI Slave: Previous MISO data hold time	5	–	–	ns
tEN_SETUP_INT	SPI Slave: SSEL valid to first SCK valid edge	20	–	–	ns
tEN_HOLD_INT	SPI Slave Select active (LOW) from last SCLK hold	20	–	–	ns
tEN_SET-UP_PRE	SPI Slave: from SSEL valid, to SCK falling edge before the first data bit	20	–	–	ns

(table continues...)

Table 55 (continued) SPI interface master

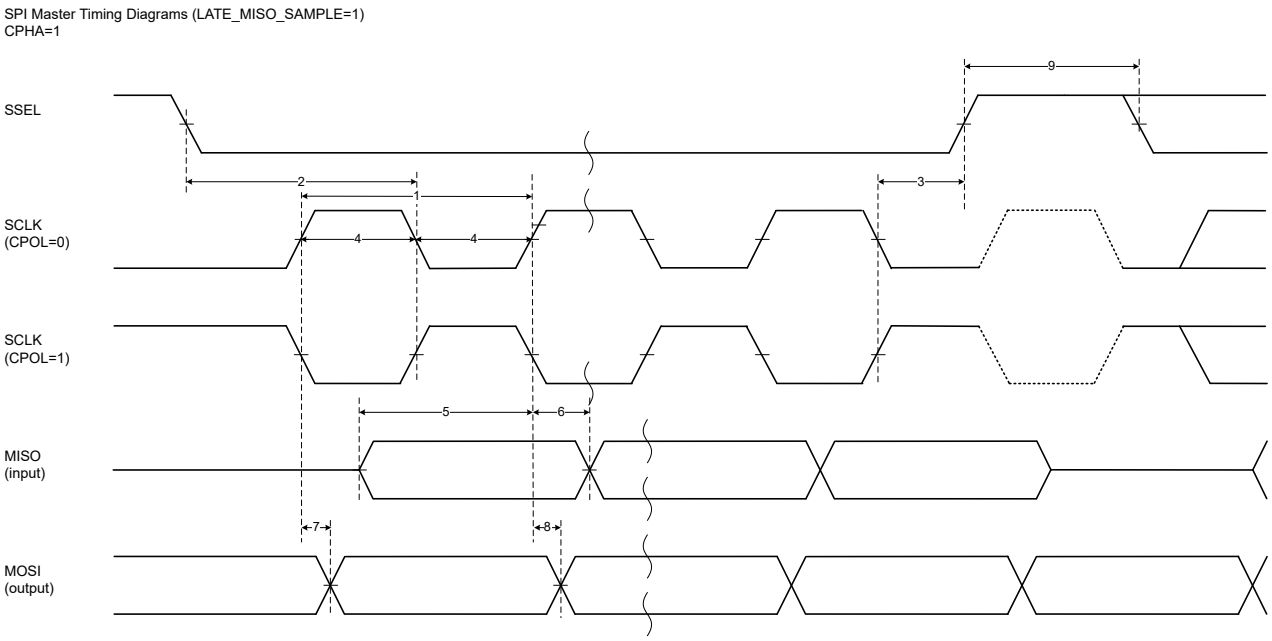
Parameter	Description	Min	Typ	Max	Units
tEN_HOLD_PRE	SPI Slave: from SCK falling edge before the first data bit, to SSEL invalid	20	–	–	ns
tEN_SETUP_CO	SPI Slave: from SSEL valid, to SCK falling edge in the first data bit	20	–	–	ns
tEN_HOLD_CO	SPI Slave: from SCK falling edge in the first data bit, to SSEL invalid	20	–	–	ns
tW_DIS_INT	SPI Slave Select inactive time	40	–	–	ns
tW_SCLKH_INT	SPI SCLK pulse width HIGH	20	–	–	ns
tW_SCLKL_INT	SPI SCLK pulse width LOW	20	–	–	ns
tSIH_INT	SPI MOSI hold from SCLK	12	–	–	ns
CSPIS_INT	SPI Capacitive Load	–	–	20	pF
SPI Interface Slave (externally clocked) [Conditions: drive_sel<1:0>= 0x]					
fSPI_EXT	SPI operating frequency	–	–	12	MHz
tDMI_EXT	SPI Slave: MOSI Valid before Sclock capturing edge	5	–	–	ns
tDSO_EXT	SPI Slave: MISO Valid after Sclock driving edge, in the external-clocked mode	–	–	32	ns
tHSO_EXT	SPI Slave: Previous MISO data hold time	3	–	–	ns
tEN_SET-UP_EXT	SPI Slave: SSEL valid to first SCK valid edge	40	–	–	ns
tEN_HOLD_EXT	SPI Slave Select active (LOW) from last SCLK hold	40	–	–	ns
tW_DIS_EXT	SPI Slave Select inactive time	80	–	–	ns
tW_SCLKH_EXT	SPI SCLK pulse width HIGH	34	–	–	ns
tW_SCLKL_EXT	SPI SCLK pulse width LOW	34	–	–	ns
tSIH_EXT	SPI MOSI hold from SCLK	20	–	–	ns
CSPIS_EXT	SPI Capacitive Load	–	–	10	pF
tVSS_EXT	SPI Slave: MISO valid after SSEL falling edge (CPHA = 0)	–	–	33	ns
fBPS	Data rate	–	–	10	Mbps

16.4.3 SPI specifications



1: SCLK period = 1 / f_{SPI}
2: Enable lead time (setup) = t_{EN_SETUP} = Depends on SPI_CTRL.SSEL_SETUP_DEL
3: Enable trail time (hold) = t_{EN_HOLD} = Depends on SPI_CTRL.SSEL_HOLD_DEL
4: SCLK high or low time = $t_{W\_SCLK\_H\_L}$
5: Input data setup time = t_{DSI}
6: Input data hold time = t_{DHI}
7: Output data valid after SCLK driving edge = t_{DMO}
8: Output data valid after SSEL falling edge (CPHA = 0) = t_{VSS}
9: Output data hold time = t_{HMO}
10: SSEL high pulse width = Depends on SPI_CTRL.SSEL_INTER_FRAME_DEL

Figure 34 SPI master timing diagrams with LOW clock phase



1: SCLK period = 1 / f_{SPI}
2: Enable lead time (setup) = t_{EN_SETUP} = Depends on SPI_CTRL.SSEL_SETUP_DEL
3: Enable trail time (hold) = t_{EN_HOLD} = Depends on SPI_CTRL.SSEL_HOLD_DEL
4: SCLK high or low time = $t_{W\_SCLK\_H\_L}$
5: Input data setup time = t_{DSI}
6: Input data hold time = t_{HDI}
7: Output data valid after SCLK driving edge = t_{DMO}
8: Output data hold time = t_{HMO}
9: SSEL high pulse width = Depends on SPI_CTRL.SSEL_INTER_FRAME_DEL

Figure 35 SPI master timing diagrams with HIGH clock phase

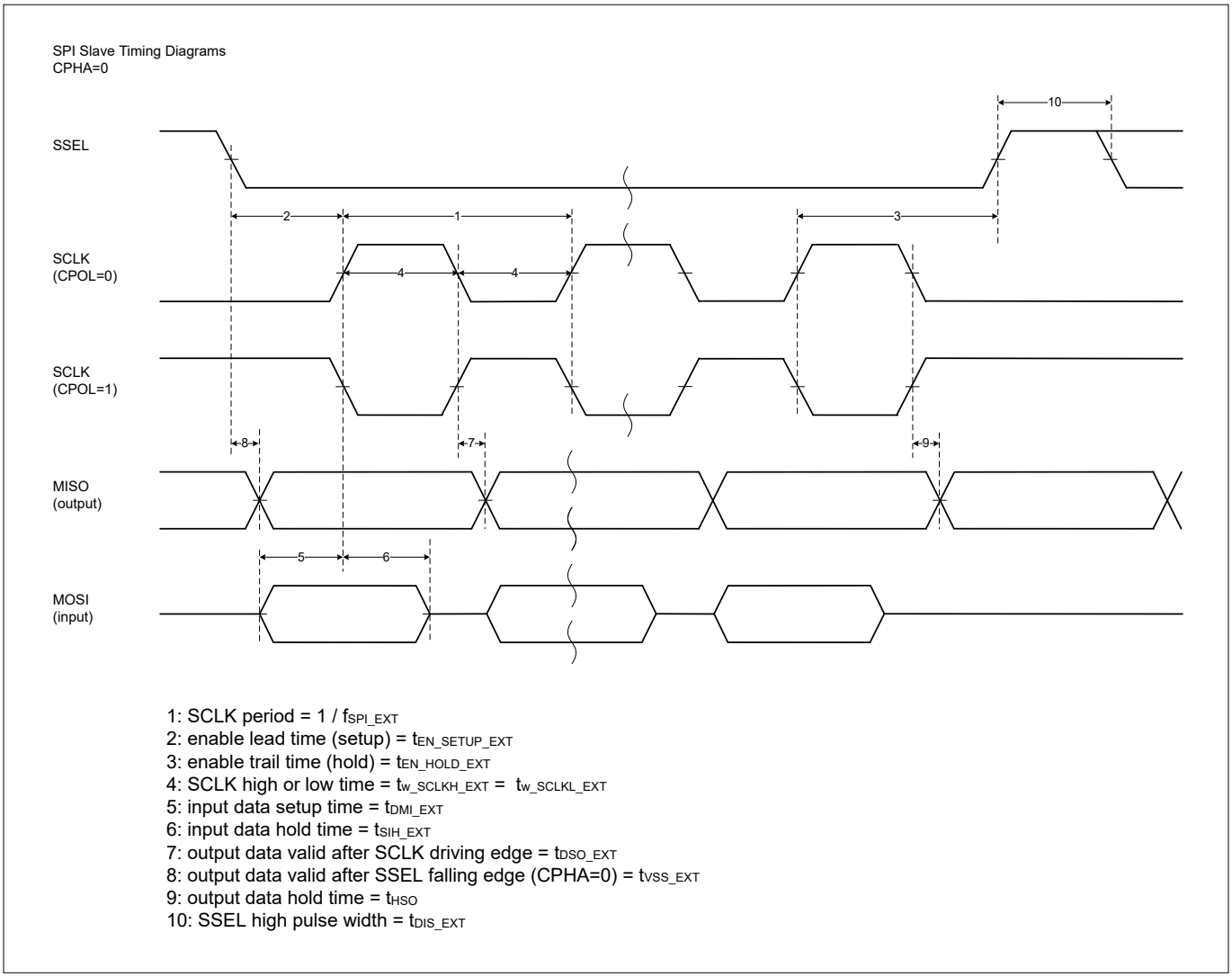


Figure 36 SPI slave timing diagrams with LOW clock phase

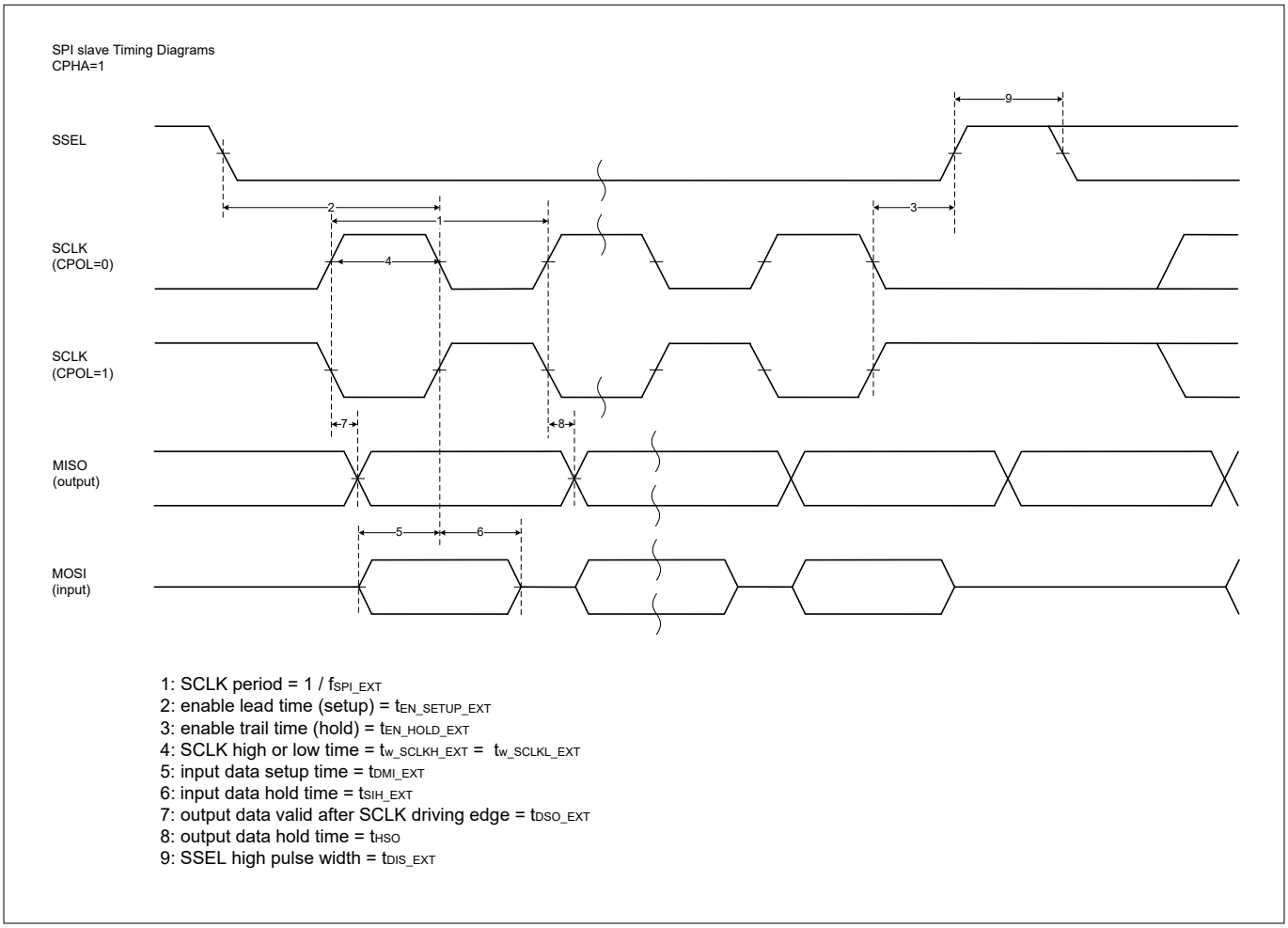


Figure 37 SPI slave timing diagrams with HIGH clock phase

16.5 TCPWM specifications

Table 56 TCPWM specifications

Unique spec ID	AC Parameter	Description	Results Min	Results Max	Unit
AC.1	Fmax	Synthesis clock frequency	–	125	MHz
AC.2	Twsync	Pulse width of synchronous input event (from internal source, e.g. DSI)	1	–	1/Fmax
C.3	TPWMENEXT	Pulse width of asynchronous input event (e.g. from GPIO)	2		
AC.4	TPWMEXT	Pulse width of output event (to GPIO)			
AC.5	QRES	Quadrature phase input resolution (from GPIO)			
AC.6	PWMRES	PWM output resolution (min. pulse width)	1		

16.6 TDM specifications

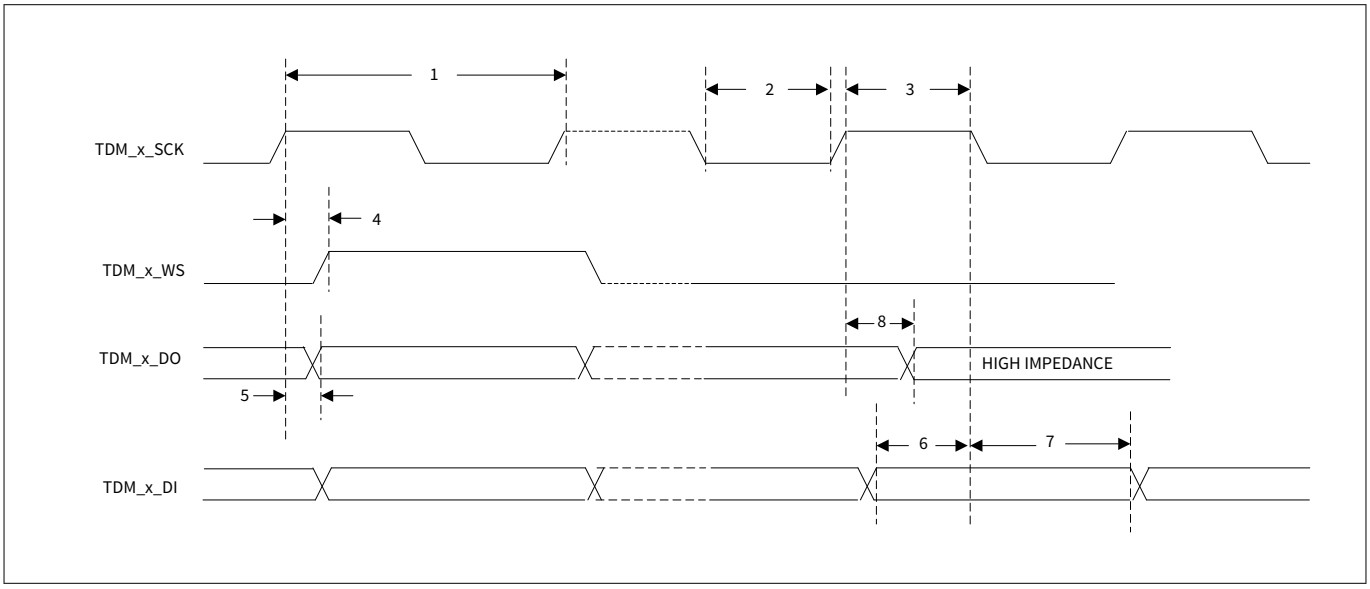


Figure 38 TDM interface timing (Short frame sync, master mode)

Table 57 TDM interface timing specifications (short frame sync, master mode)

Reference	Characteristics	Min	Typ	Max	Unit
1	TDM bit clock frequency	–	–	12.0	MHz
2	TDM bit clock LOW	41.0	–	–	ns
3	TDM bit clock HIGH	41.0	–	–	ns
4	TDM SYNC delay	0	–	25.0	ns
5	TDM_OUT delay	0	–	25.0	ns
6	TDM IN setup	8.0	–	–	ns
7	TDM IN hold	8.0	–	–	ns
8	Delay from the rising edge of TDM_CLK during the last bit period to TDM_OUT becoming HIGH-Z	0	–	25.0	ns

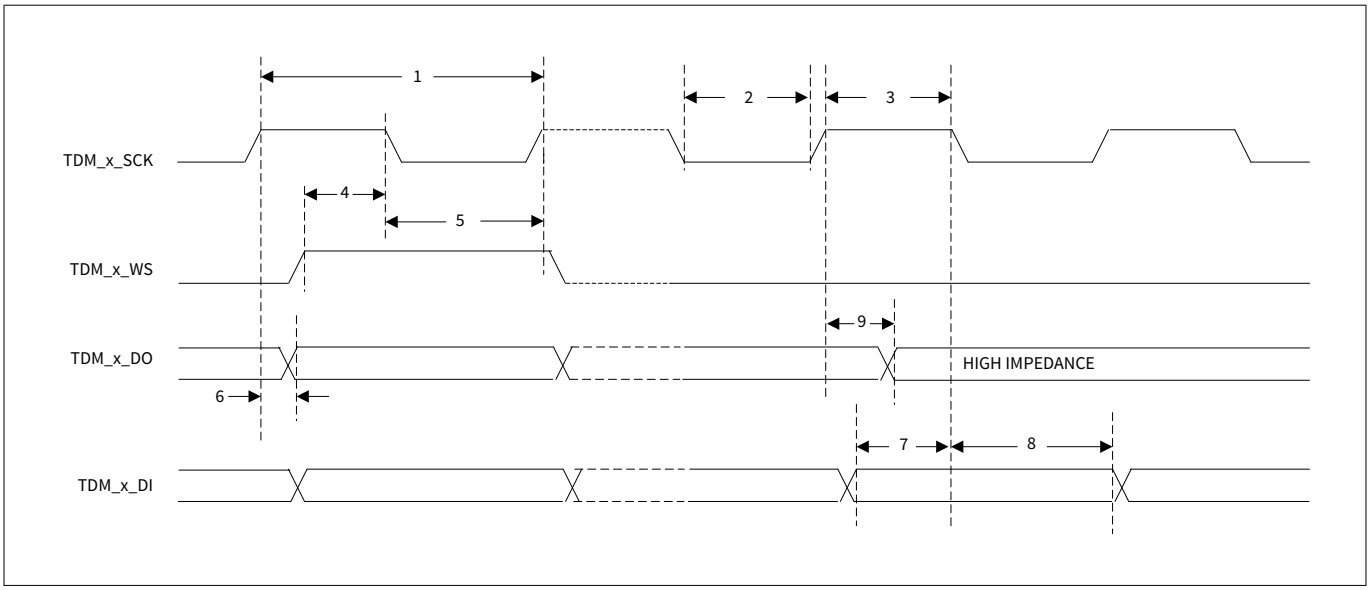


Figure 39 TDM interface timing (Short frame sync, slave mode)

Table 58 TDM interface timing specifications (short frame sync, slave mode)

Reference	Characteristics	Min	Typ	Max	Unit
1	TDM bit clock frequency	–	–	12.0	MHz
2	TDM bit clock LOW	41.0	–	–	ns
3	TDM bit clock HIGH	41.0	–	–	ns
4	TDM_SYNC setup	8.0	–	–	ns
5	TDM_SYNC hold	8.0	–	–	ns
6	TDM_OUT delay	0	–	25.0	ns
7	TDM_IN setup	8.0	–	–	ns
8	TDM_IN hold	8.0	–	–	ns
9	Delay from the rising edge of TDM_CLK during the last bit period to TDM_OUT becoming HIGH-Z	0	–	25.0	ns

16.7 JTAG interface

Table 59 JTAG interface

Signal name	Period	Output maximum	Output minimum	Setup	Hold
TCK	125 ns	–	–	–	–
TDI	–			20 ns	0 ns
TMS					
TDO		100 ns	0 ns	–	–
JTAG_RESET	250 ns	–	–		

17 Power up sequence and timing

Clock specifications

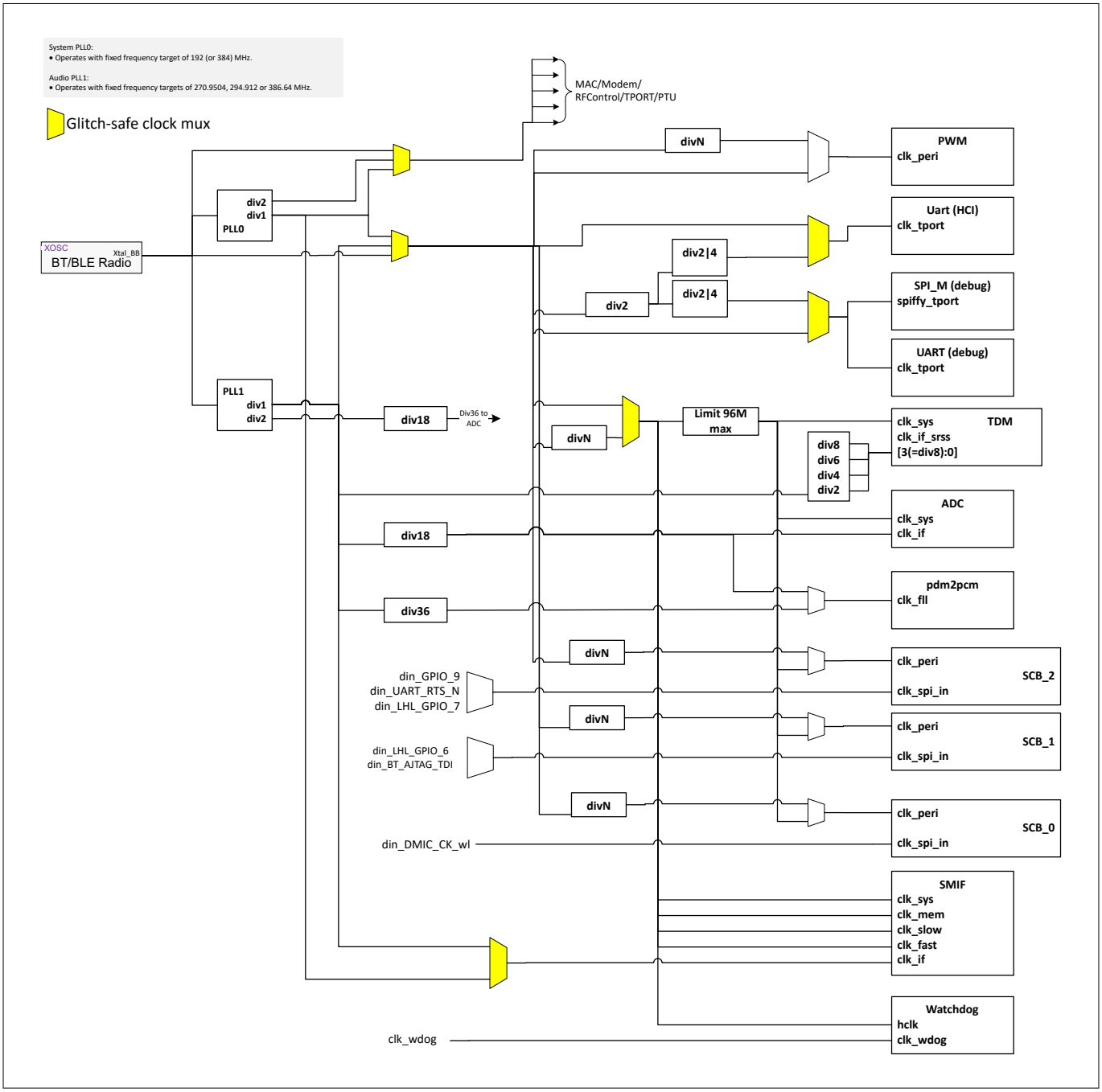


Figure 40 Clock specifications

17.1 MCU or Bluetooth® start up timing diagram

***Notes**:*

1. *VBAT and VDDIO should not rise 10%–90% faster than 40 microseconds.*
2. *VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.*

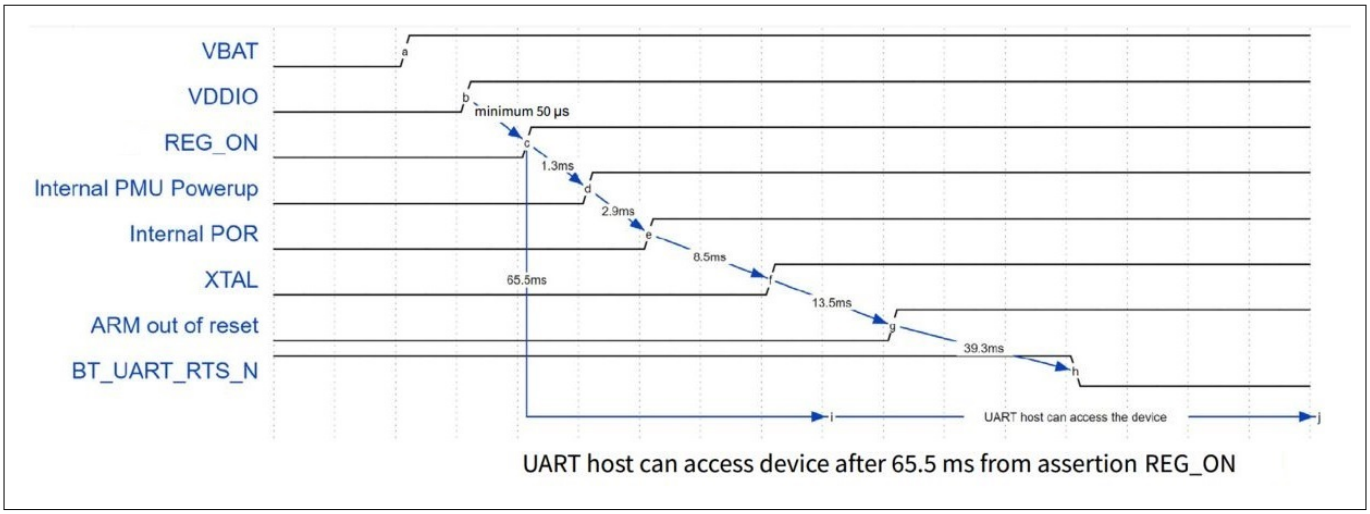
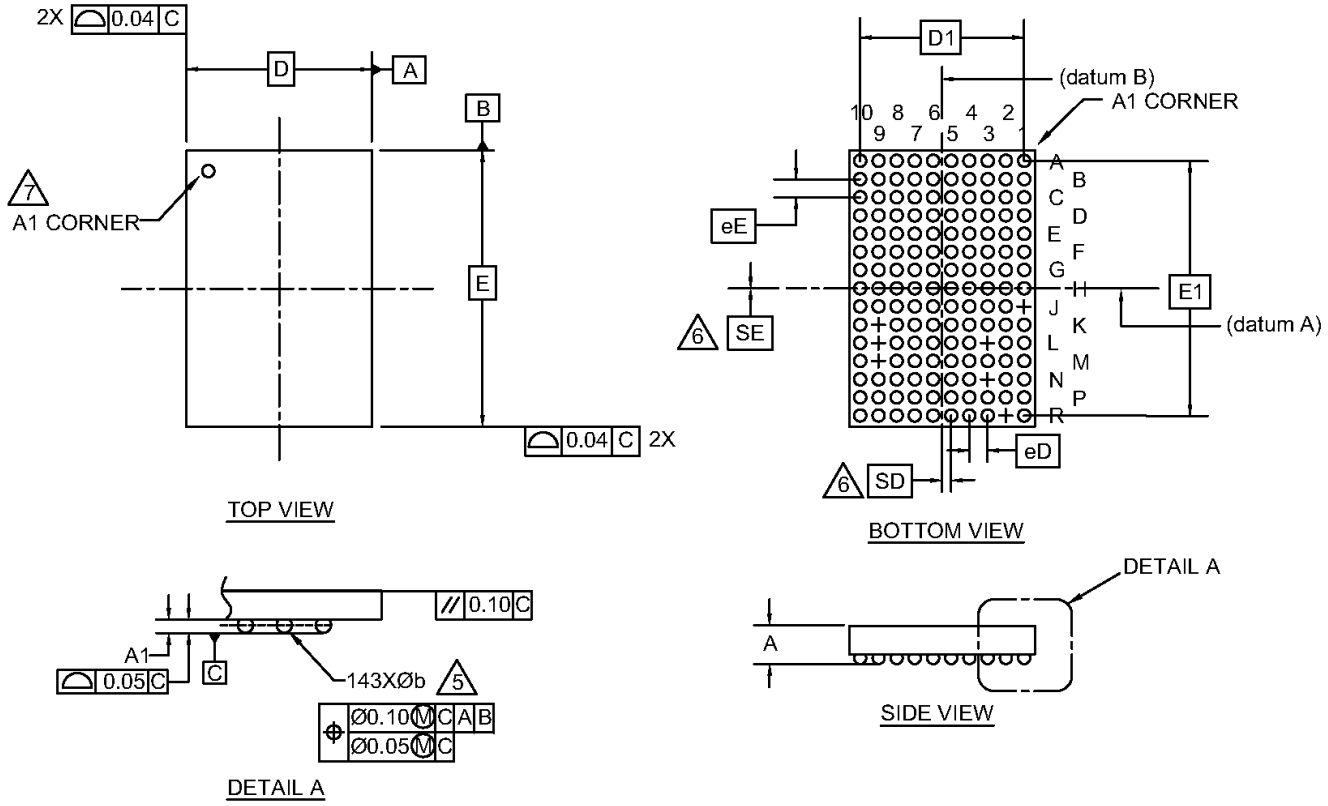


Figure 41 MCU/Bluetooth® subsystem start up timing diagram

18 Packaging information

18.1 Package diagram



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	0.45
A1	0.14	-	-
D		3.57 BSC	
E		5.32 BSC	
D1		3.15 BSC	
E1		4.90 BSC	
MD		10	
ME		15	
N		143	
Ø b	0.18	0.23	0.28
eD		0.35 BSC	
eE		0.35 BSC	
SD		0.175 BSC	
SE		0.00 BSC	

NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. SOLDER BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP-020.
3. "e" REPRESENTS THE SOLDER BALL GRID PITCH.
4. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE NUMBER OF POPULATED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

5. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.

6. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

7. A1 CORNER TO BE IDENTIFIED BY LASER MARK

8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED SOLDER BALLS.
9. JEDEC SPECIFICATION NO. REF. : N/A.

002-33373 *D

Figure 42 143-ball WLBGA 3.57 × 5.32 × 0.45 mm package outline

18.2 Package thermal characteristics

The information in Table 60 is based on absolute junction temperature 125°C limit is maintained through active thermal monitoring, throttling, and turning off one of the TX chains or both.

Table 60 WLBGA package thermal characteristics

Characteristic	WLBGA
θ_{JA} (°C/W) (value in still air)	21.1
θ_{JB} (°C/W)	7.3
θ_{JC} (°C/W)	0.1
Ψ_{JT} (°C/W)	0.02

The package thermal characterization parameter PSI_{JT} (Y_{JT}) yields a better estimation of actual junction temperature (T_J) than using the junction-to-case thermal resistance parameter $Theta_{JC}$ (q_{JC}). The reason for this is that q_{JC} is based on the assumption that all the power is dissipated through the top surface of the package case. In actual applications, however, some of the power is dissipated through the bottom and sides of the package. Y_{JT} takes into account the power dissipated through the top, bottom, and sides of the package. The equation for calculating the device junction temperature is:

$$T_J = T_T + P \times \psi_{JT}$$

where:

- T_J = Junction temperature at steady-state condition (°C)
- T_T = Package case top center temperature at steady-state condition (°C)
- P = Device power dissipation (Watts)
- Ψ_{JT} = Package thermal characteristics; no airflow (°C/W)

18.3 Environmental characteristics

For environmental characteristics data, see Table 28.

19 Ordering information

Table 61 Ordering information

Part number	Package	Description	Operating ambient temperature
CYW55913IUBGT	143-ball WLBGA (3.57 mm × 5.32 mm, 0.35 mm pitch)	1x1 802.11ax tri-band 2.4/5/6 GHz 20 MHz, Bluetooth® LE 5.4 combo and Connected MCU IC tape and reel	–40°C to 85°C
CYW55912IUBGT		1x1 802.11ax dual-band 2.4/5 GHz 20 MHz, Bluetooth® LE 5.4 combo and Connected MCU IC tape and reel	
CYW55911IUBGT		1x1 802.11ax single-band 2.4 GHz 20 MHz, Bluetooth® LE 5.4 combo and Connected MCU IC tape and reel	
CYW55903IUBGT		1x1 802.11ax tri-band 2.4/5/6 GHz 20 MHz Wi-Fi only and Connected MCU IC tape and reel	
CYW55902IUBGT		1x1 802.11ax dual-band 2.4/5 GHz 20 MHz Wi-Fi only and Connected MCU IC tape and reel	
CYW55901IUBGT		1x1 802.11ax single-band 2.4 GHz 20 MHz Wi-Fi only and Connected MCU IC tape and reel	

20 Acronyms

Table 62 Acronyms used in this document

Acronym	Description
AES	Advanced Encryption Standard
AMPDU	Aggregated MAC Protocol Data Unit
AMSDU	Aggregated MAC Service Data Unit
AP	access point
BA	Block Acknowledgment
BDR	basic data rate
BLE	Bluetooth® Low Energy
BSS	basic service set
BW	Band width
C	Celsius
Codec	coder decoder
Coex	coexistence
CTS	Clear To Send
dB	decibel
dBm	decibel-milliwatts
DSSS	direct sequence spread spectrum
EDR	enhanced data rate
EIRP	effective isotropic radiated power
GSPI	general serial peripheral interface
HCI	host controller interface
HE	High Efficiency
HFA	hands free profile
HFP	hands free profile
I2S	inter-IC sound
IEEE	Institute of electrical and electronics engineers
Kbps	kilobits per second
LC3	low complexity communication codec
LE	low-energy
LNA	low-noise amplifier
LTE	long term evolution
MAC	medium access controller
Mbps	mega-bits per second

(table continues...)

Table 62 (continued) Acronyms used in this document

Acronym	Description
MCS	Modulation and coding scheme
MIMO	multiple input multiple output
MU-MIMO	multi-user-multiple-input multiple-output
NAV	network allocation vector
OFDM	orthogonal frequency division multiplexing
OFDMA	orthogonal frequency division multiple access
OMI	operating mode indicator
PA	power amplifier
PCM	pulse code modulation
PDM	pulse density modulation
PHY	physical layer
PPDU	Physical Layer Protocol Data Unit
QAM	quadrature amplitude modulation
QOS	Quality of Service
RIFS	Reduced Interframe Space
ROM	read-only memory
RTS	Request To Send
RU	Resource Unit
SDIO	secure digital input output
SRAM	serial random access memory
STA	station
STBC	space time block codes
TDM	time division multiplexing
TKIP	temporal key integrity protocol
TWT	target wake time
UART	universal asynchronous receiver transmitter
WEP	wired equivalent privacy
WLAN	wireless local area network
WLBGA	wafer level ball grid array
WPA	Wi-Fi protected access

21 Document conventions

21.1 Units of measure

Table 63 Unit of measure

Symbol	Unit of measure
°C	degrees celsius
dB	decibel
fF	femto farad
Hz	hertz
KB	1024 bytes
kbps	kilobits per second
khr	kilohour
kHz	kilohertz
kW	kilo ohm
ksps	kilosamples per second
LSB	least significant bit
Mbps	megabits per second
MHz	megahertz
MΩ	mega-ohm
Msps	megasamples per second
µA	microampere
µF	microfarad
µH	microhenry
µs	microsecond
µV	microvolt
µW	microwatt
mA	milliampere
ms	millisecond
mV	millivolt
nA	nanoampere
ns	nanosecond
nV	nanovolt
Ω	ohm
pF	picofarad
ppm	parts per million

(table continues...)

Table 63 (continued) Unit of measure

Symbol	Unit of measure
ps	picosecond
s	second
sps	samples per second
sqrtHz	square root of hertz
V	volt

Revision history

Document revision	Date	Description of changes
*C	2024-10-30	Updated: Features Family block diagram Functional block diagram Standards compliance Security system (Arm® TrustZone CryptoCell 312) IEEE 802.11ax MAC Table 34 Table 37 Table 39 Table 40 Table 41 Table 44 Removed - Burst buffer operation Release to web
*D	2025-06-16	Updated Description Updated Features Updated Figure 2 Updated Power-down mode Updated Table 2 Updated GPIO Updated SPI interface Updated GPIO signal functions Updated WLAN 2.4 GHz Tx performance specifications Updated WLAN 5 GHz Tx performance specifications Updated WLAN 6 GHz Tx performance specifications Updated WLAN current consumption 2.4/5 GHz Updated WLAN current consumption - 6 GHz

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