Automotive 100BASE-T1/1000BASE-T1 Transceiver

Overview

The BRIGHTLANE™ 88Q2220[M]/88Q2221[M]/88Q120[0/1]M device is a single-pair Ethernet physical layer transceiver (PHY) that supports operation over unshielded twisted pair (UTP). The BRIGHTLANE™ 88Q2220[M]/88Q2221[M] transceiver implements the Ethernet physical layer portion of 1000BASE-T1 and 100BASE-T1 as defined by the IEEE 802.3bp and IEEE 802.3bw standards respectively and the BRIGHTLANE™ 88Q120[0/1]M transceiver implements the Ethernet physical layer portion of 100BASE-T1 as defined by the IEEE 802.3bw standard.

The device family supports reduced pin count GMII (RGMII) or SGMII for direct connection to a MAC/switch port. SGMII operates at 1.25 Gbps over a single differential pair, reducing power and number of I/Os used on the MAC interface.

The device integrates media dependent interface (MDI) termination resistors into the PHY. This resistor integration simplifies board layout and reduces board cost by reducing the number of external components.

The device has a linear regulator to generate all required voltages. The device can run off a single 3.3V supply. The device supports 1.8V, 2.5V, and 3.3V LVCMOS I/O standards.

The device incorporates the Advanced Virtual Cable Tester (VCT) feature, which uses time domain reflectometry (TDR) technology for the remote identification of potential cable malfunctions, reducing equipment returns and service calls. Using VCT, the device will also detect cable opens, shorts, or any impedance mismatch in the cable and report the distance to the fault accurately within one meter.

The device uses advanced mixed-signal processing to perform equalization, echo and crosstalk cancellation, data recovery, and error correction at a data rate of 1 Gbps. The device achieves robust performance and exceeds electromagnetic interference (EMI) requirements in noisy environments with very low power dissipation.

Features

- Interfaces
  - 1000BASE-T1, IEEE 802.3bp-compliant
  - 100BASE-T1, IEEE 802.3bw-compliant
  - MDC/MDIO management interface
  - SGMII interface
  - RGMII interface
    - 1.8V/2.5V/3.3V I/Os
- Four RGMII timing modes including integrated delays which eliminates the need for adding trace delays on the PCB
- Supports IEEE 802.1AE MACsec (BRIGHTLANE™ 88Q2220M/88Q2221M/88Q120[0/1]M only)
- Supports LVCMOS I/O standards on the RGMII interface
- Integrated MDI interface termination resistors which eliminate passive components
- Loopback modes for diagnostics
- Fully integrated digital adaptive equalizers, echo cancellers, and crosstalk cancellers
- Advanced digital baseline wander correction
- Automatic MDI polarity correction
- Supports both IEEE 802.3bp-compliant Auto-Negotiation mode and Link Synchronization mode
- Software programmable LED modes
- Supports Synchronous Ethernet (SyncE)
- Supports IEEE 802.1AS, 802.1AS-Rev– Precision Time Protocol (PTP)
- Supports 1-step PTP
- CRC checker, packet counter, and CRC preemption packet checking
- Advanced VCT for cable diagnostics
- Ultra-low power
- RGMII impedance calibration
- AEC-Q100 Automotive Grade 1 rated
- 40-pin QFN, 6.0 × 6.0 mm, 0.5 mm pitch
- Integrated temperature sensor
- TC10 Sleep/Wake

- Low power mode with energy detect at 45 µA

Table 1: Features

Features	BRIGHTLANE™ 88Q2220	BRIGHTLANE™ 88Q2220M	BRIGHTLANE™ 88Q2221	BRIGHTLANE™ 88Q2221M	BRIGHTLANE™ 88Q1200M	BRIGHTLANE™ 88Q1201M
RGMII to copper	Yes	Yes	–	–	Yes	–
SGMII to copper	–	–	Yes	Yes	–	Yes
100BASE-T1	Yes	Yes	Yes	Yes	Yes	Yes
1000BASE-T1	Yes	Yes	Yes	Yes	–	–
MACsec	No	Yes	No	Yes	Yes	Yes
Sleep/Wake	TC10, LPSD	TC10, LPSD	TC10, LPSD	TC10, LPSD	TC10, LPSD	TC10, LPSD
PTP	802.1AS-Rev	802.1AS-Rev	802.1AS-Rev	802.1AS-Rev	802.1AS-Rev	802.1AS-Rev
Fail Safe Mode	Yes	Yes	Yes	Yes	Yes	Yes
I/O Voltage (VDDO)	3.3V/2.5V/1.8V	3.3V/2.5V/1.8V	3.3V/2.5V/1.8V	3.3V/2.5V/1.8V	3.3V/2.5V/1.8V	3.3V/2.5V/1.8V
Package	40-pin QFN	40-pin QFN	40-pin QFN	40-pin QFN	40-pin QFN	40-pin QFN

Applications

- Automotive infotainment systems
- Advanced driver assist systems
- Automotive diagnostics
- Body electronics

Figure 1: BRIGHTLANE™ 88Q2221/88Q2221M Block Diagram

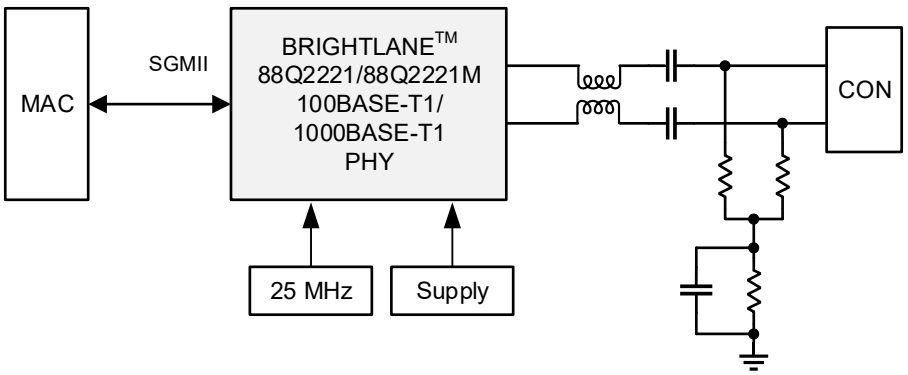


Figure 2: BRIGHTLANE™ 88Q2220/88Q2220M Block Diagram

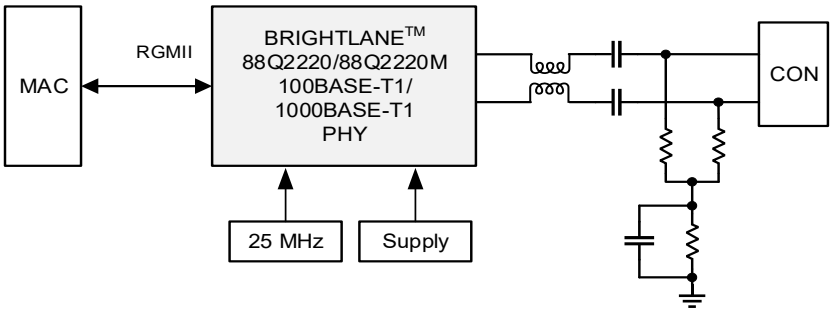


Figure 3: BRIGHTLANE™ 88Q1200M Block Diagram

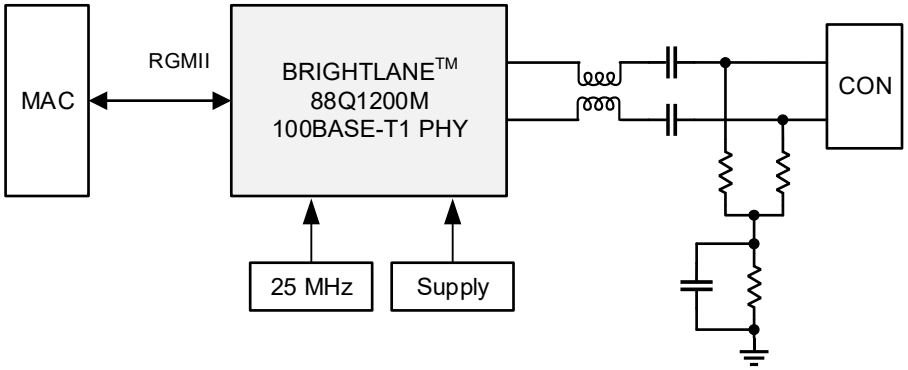
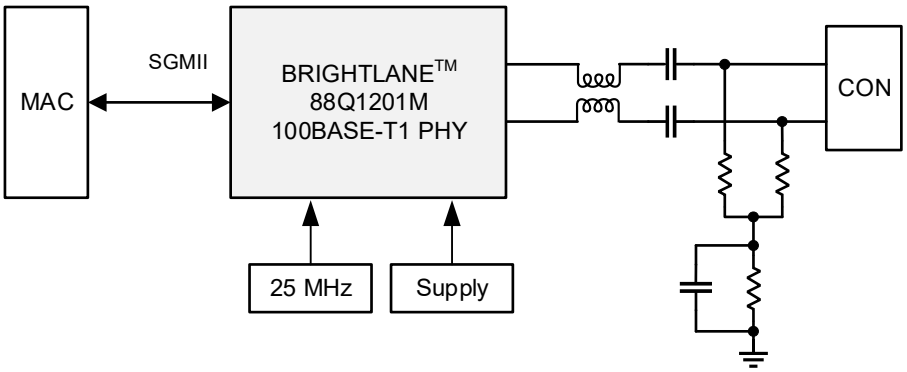


Figure 4: BRIGHTLANE™ 88Q1201M Block Diaram



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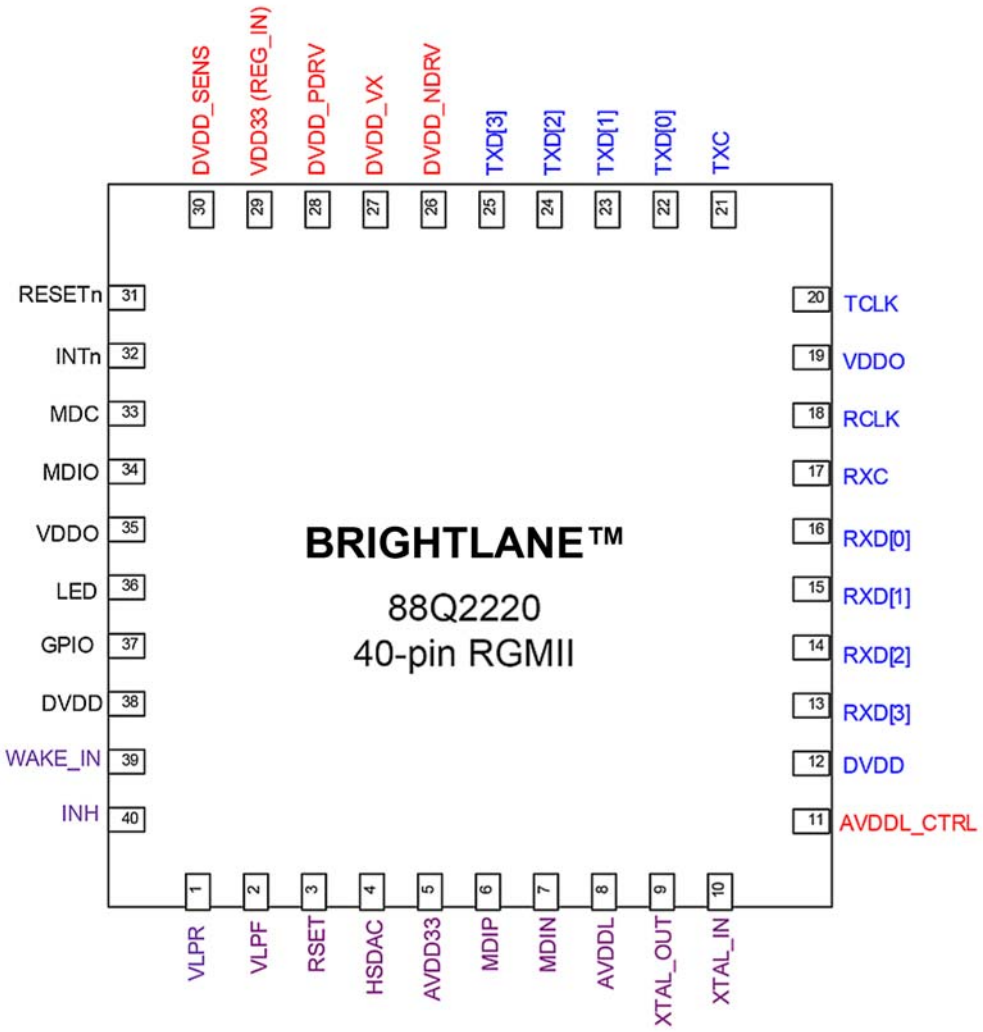
1 Signal Description

1.1 BRIGHTLANE™ 88Q2220/88Q2220M Pinout

The BRIGHTLANE™ 88Q2220/88Q2220M device is a 100BASE-T1/1000BASE-T1 Ethernet transceiver.

Figure 5: BRIGHTLANE™ 88Q2220/88Q2220M Device 40-pin RGMII Package (Top View)



1.2 BRIGHTLANE™ 88Q2220/88Q2220M Pin Descriptions

Table 2: BRIGHTLANE™ 88Q2220/88Q2220M Pin Type Definitions

Pin Type	Definition
A	Analog
H	Input with hysteresis
I/O	Input and output
I	Input only
O	Output only
PU	Internal pull-up
PD	Internal pull-down
D	Open drain output
Z	Tri-state output
mA	DC sink capability

1.2.1 BRIGHTLANE™ 88Q2220/88Q2220M Media Dependent Interface

Table 3: BRIGHTLANE™ 88Q2220/88Q2220M Media Dependent Interface

BRIGHTLANE™ 88Q2220/88Q2220M Pin #	Pin Name	Pin Type	During Reset	Description
7 6	MDIN MDIP	I/O	I	Media Dependent Interface. In 100/1000BASE-T1, MDIN/P are used for transmit and receive.

1.2.2 BRIGHTLANE™ 88Q2220/88Q2220M Host Interfaces

The host interfaces support 100BASE-T1 and 1000BASE-T1 modes of operation.

Table 4: BRIGHTLANE™ 88Q2220/88Q2220M Host Interfaces

BRIGHTLANE™ 88Q2220/88Q2220M Pin #	Pin Name	Pin Type	During Reset	Description
20	TCLK	I	I	When RGMII is used, this pin is an input. • 100BASE-T1 mode: This pin must be driven with a 25 MHz clock with ±50 ppm tolerance. • 1000BASE-T1 mode: This pin must be driven with a 125 MHz clock with ±50 ppm tolerance.
21	TXC	I	I	When RGMII is used, this pin's signal must be presented according to the RGMII timing mode requirements.

Table 4: BRIGHTLANE™ 88Q2220/88Q2220M Host Interfaces (Continued)

BRIGHTLANE™ 88Q2220/88Q2220M Pin #	Pin Name	Pin Type	During Reset	Description
25 24 23 22	TXD [3] TXD [2] TXD [1] TXD [0]	I	I	When RGMII is used, the signal for these pins must be presented according to the RGMII timing mode requirements. • 100BASE-T1 mode: Data is presented for sampling with the rising edge of TCLK only. • 1000BASE-T1 mode: Data is presented for sampling with both edges of TCLK.
18	RCLK/CONFIG5	O	Tri-state	When RGMII is used, this pin is an output. • 100BASE-T1 mode: This pin is an output that drives out a 25 MHz clock with ±50 ppm tolerance. • 1000BASE-T1 mode: This pin is an output that drives out a 125 MHz clock with ±50 ppm tolerance. Hardware configuration pin, CONFIG5
17	RXC/CONFIG4	O	Tri-state	When RGMII is used, this pin's signal must be presented according to the RGMII timing mode requirements. Hardware configuration pin, CONFIG4
13 14 15 16	RXD[3]/CONFIG3 RXD[2]/CONFIG2 RXD[1]/CONFIG1 RXD[0]/CONFIG0	O	Tri-state	When RGMII is used, the signal for these pins must be presented according to the RGMII timing mode requirements. • 100BASE-T1 mode: Data is presented for sampling with the rising edge of RCLK only. • 1000BASE-T1 mode: Data is presented for sampling with both edges of RCLK. Hardware configuration pins, CONFIG3, CONFIG2, CONFIG1, and CONFIG0

1.2.3 BRIGHTLANE™ 88Q2220/88Q2220M Management Interface

Table 5: BRIGHTLANE™ 88Q2220/88Q2220M Management Interface

BRIGHTLANE™ 88Q2220/88Q2220M Pin #	Pin Name	Pin Type	During Reset	Description
33	MDC	I	I	Management Interface Clock. A continuous clock stream is not required for MDC; Maximum frequency is 12.5 MHz.
34	MDIO	I/O	I	Management Interface Data. This pin requires a pull-up resistor with a resistance from 1.5 kΩ to 10 kΩ.

1.2.4 BRIGHTLANE™ 88Q2220/88Q2220M TX_ ENABLE/GPIO/Interrupt Interface

Table 6: BRIGHTLANE™ 88Q2220/88Q2220M TX_ENABLE/GPIO/Interrupt Interface

BRIGHTLANE™ 88Q2220/88Q2220M Pin #	Pin Name	Pin Type	During Reset	Description
36	LED/TX_ ENABLE	I/O	Tri-state with PU	Tx Enable/GPIO/LED. This pin is an input by default and used to implement a feature that allows blocking Tx packets. For details, see Section 2.2.3, Tx Disable Feature. This pin can be used as an GPIO/LED.
37	GPIO	I/O	Tri-state with PU	GPIO/LED Output/SyncE Recovered Clock Output. For hardware configuration details, see Section 2.19.1, Hardware Configuration.
32	INTn	O, D	Tri-state	Interrupt Output.

1.2.5 BRIGHTLANE™ 88Q2220/88Q2220M Clock/Configuration/Reset/I/O

Table 7: BRIGHTLANE™ 88Q2220/88Q2220M Clock/Configuration/Reset/I/O

BRIGHTLANE™ 88Q2220/88Q2220M Pin #	Pin Name	Pin Type	During Reset	Description
10	XTAL_IN	I	I	Reference Clock. 25 MHz ±100 ppm tolerance crystal reference or oscillator input. When XTAL_IN is driven directly from the oscillator or clock buffer, this pin must be AC coupled with a 0.1 nF capacitor.
9	XTAL_OUT	O	Independent of Reset	Reference Clock. 25 MHz ±100 ppm tolerance crystal reference. When the XTAL_OUT pin is not connected to a crystal, it must be connected to ground through a 0.1 µF ceramic capacitor.
31	RESETn	I	Low	Hardware reset, active-low. 0 = Reset 1 = Normal operation

1.2.6 BRIGHTLANE™ 88Q2220/88Q2220M Control and Reference

Table 8: BRIGHTLANE™ 88Q2220/88Q2220M Control and Reference

BRIGHTLANE™ 88Q2220/88Q2220M Pin #	Pin Name	Pin Type	During Reset	Description
3	RSET	I, A	A	Constant Voltage Reference. For this pin, an external 4.99 kΩ, 1% resistor connection to VSS is required.

1.2.7 BRIGHTLANE™ 88Q2220/88Q2220M Test

Table 9: BRIGHTLANE™ 88Q2220/88Q2220M Test

BRIGHTLANE™ 88Q2220/88Q2220M Pin #	Pin Name	Pin Type	During Reset	Description
4	HSDAC	A, O	Tri-state	Analog AC Test Positive This pin can be left floating if not used.

1.2.8 BRIGHTLANE™ 88Q2220/88Q2220M Low Power Signal Detect

Table 10: BRIGHTLANE™ 88Q2220/88Q2220M Low Power Signal Detect

BRIGHTLANE™ 88Q2220/88Q2220M Pin #	Pin Name	Pin Type	During Reset	Description
39	WAKE_IN	A, I	I	Analog Wake Input This is used for local wake-up. This pin must be left floating when Low Power Signal Detect is not used.
1	VLPR	A	Analog Power	This is the regulated supply derived from battery. B0: May be left floating B2: Must be connected to a voltage per Table 51, LPSD Electrical Characteristics, on page 77.
2	VLPF	A	A	Connect to the external battery circuit. Refer the LPSD block diagram in Figure 22, LPSD Block Diagram — Option 1, on page 76. This pin must be left floating when LPSD circuit is not used.
40	INH	A, O	O	Output collector to control enable of the external regulator. To draw minimal current in deep sleep, INH has two states. ‘HIGH’ to drive the external regulator(s) enables signal (on), and tristate when in deep sleep. An external 10 kΩ pull-down is required at INH. This pin must be left floating when LPSD is not used.

1.2.9 BRIGHTLANE™ 88Q2220/88Q2220M Power, Ground, and Internal Regulators

Table 11: BRIGHTLANE™ 88Q2220/88Q2220M Power, Ground, and Internal Regulators

BRIGHTLANE™ 88Q2220/88Q2220M Pin #	Pin Name	Pin Type	During Reset	Description
8	AVDDL	Power	Analog Power	Analog Supply – 1.2V[1] AVDDL can be supplied externally with 1.2V or via the internal regulator generated 1.2V.
11	AVDDL_ CTRL	A, O	Analog	AVDDL Regulator Control, connect to the external PNP. If the 1.2V regulator option is not used, then this pin must be left floating, no connect.
30	DVDD_ Sense	Power	Power	DVDD_Sense input Connect the 0.75V[3] generated from external FET after inductor to DVDD_Sense. If the 0.75V[3] regulator option is not used, then this pin must be left floating, no connect.
28	DVDD_ PDRV	Power	Power	Gate Driving Signal of External PFET If the 0.75V[3] regulator option is not used, then this pin must be left floating, no connect.
27	DVDD_Vx	Power	Power	Power Switch Sense If the 0.75V[3] regulator option is not used, then this pin must be left floating, no connect.
26	DVDD_ NDRV	Power	Power	Gate Driving Signal of External NFET If the 0.75V[3] regulator option is not used, then this pin must be left floating, no connect.
5	AVDD33	Power	Power	Analog Supply – 3.3V
29	VDD33 (REG_IN)	Power	Power	Analog Supply for the Internal Regulator – 3.3V If the internal regulator is not used, then this pin must be left floating (No Connect). Leave regulator control pins floating when regulators not used. **CAUTION:** If the internal regulator is not used, then this pin must be left floating. Connecting this pin to either another power supply or to ground will damage the device.
19	VDDO	Power	Power	1.8V, 2.5V, or 3.3V I/O Supply[2]
35	VDDO	Power	Power	1.8V, 2.5V, or 3.3V I/O Supply[2]
38, 12	DVDD	Power	Power	Digital Supply – 0.75V[3]
E-PAD	VSS	GND	GND	Ground to Device. The 40-pin QFN package has an exposed die pad (E-PAD) at its base. This E-PAD must be soldered to VSS. For the exact location and dimensions of the E-PAD, see Section 5, Package Mechanical Dimensions.

1. AVDDL supplies the XTAL_IN and XTAL_OUT pins.

2. VDDO supplies the MDC, MDIO, RESETn, INTn, GPIO, TEST, and the RGMII interface pins.
3. 0.75V applies for Rev B0/B1. 0.80V applies for Rev B2.

1.3 BRIGHTLANE™ 88Q2220/88Q2220M Pin Assignment List — Alphabetical by Signal Name

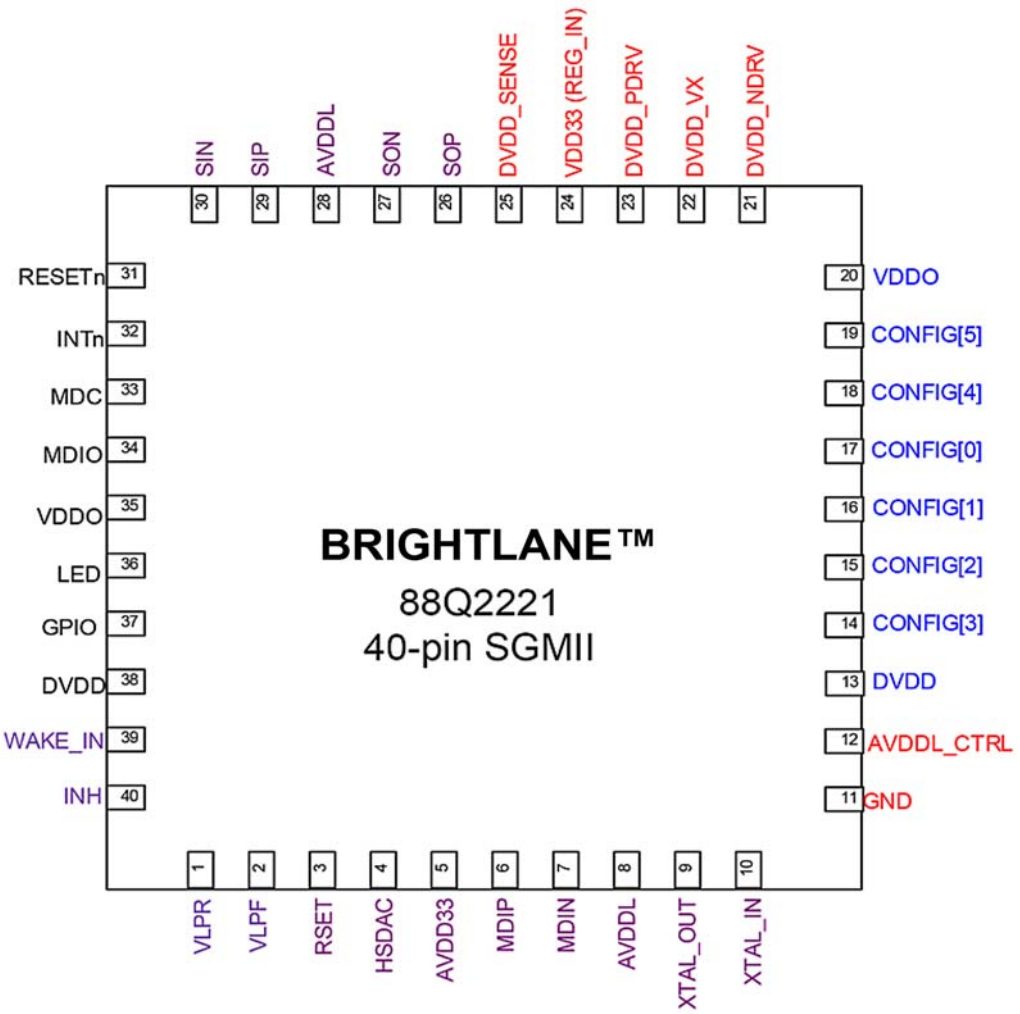
Table 12: BRIGHTLANE™ 88Q2220/88Q2220M 40-pin QFN Pin Assignment List — Alphabetical by Signal Name

Pin #	Pin Name	Pin #	Pin Name
5	AVDD33	3	RSET
8	AVDDL	17	RXC/CONFIG4
11	AVDDL_CTRL	13	RXD[3/CONFIG3
38	DVDD	14	RXD[2]/CONFIG2
26	DVDD_NDRV	16	RXD[0]/CONFIG0]
28	DVDD_PDRV	20	TCLK
30	DVDD_Sense	21	TXC
27	DVDD_Vx	22	TXD[0]
12	DVDD	15	RXD[1]/CONFIG1
37	GPIO	23	TXD[1]
4	HSDACP	24	TXD[2]
40	INH	25	TXD[3]
32	INTn	2	VLPF
36	LED	1	VLPR
33	MDC	29	VDD33 (REG_IN)
7	MDIN	19	VDDO
34	MDIO	35	VDDO
6	MDIP	E-PAD	VSS
18	RCLK/CONFIG5	39	WAKE_IN
31	RESETn	10	XTAL_IN
		9	XTAL_OUT

1.4 BRIGHTLANE™ 88Q2221/88Q2221M Pinout

The BRIGHTLANE™ 88Q2221/88Q2221M device is a 100BASE-T1/1000BASE-T1 Ethernet transceiver.

Figure 6: BRIGHTLANE™ 88Q2221/88Q2221M Device 40-pin SGMII Package (Top View)



1.5 BRIGHTLANE™ 88Q2221/88Q2221M Pin Descriptions

Table 13: BRIGHTLANE™ 88Q2221/88Q2221M Pin Type Definitions

Pin Type	Definition
A	Analog
H	Input with hysteresis
I/O	Input and output
I	Input only
O	Output only
PU	Internal pull-up
PD	Internal pull-down
D	Open drain output
Z	Tri-state output
mA	DC sink capability

1.5.1 BRIGHTLANE™ 88Q2221/88Q2221M Media Dependent Interface

Table 14: BRIGHTLANE™ 88Q2221/88Q2221M Media Dependent Interface

BRIGHTLANE™ 88Q2221/88Q2221M Pin #	Pin Name	Pin Type	During Reset	Description
7 6	MDIN MDIP	I/O	Tri-state	Media Dependent Interface. In 100/1000BASE-T1, MDIN/P are used for transmit and receive.

1.5.2 BRIGHTLANE™ 88Q2221/88Q2221M Host Interfaces

The host interfaces support 100BASE-T1 and 1000BASE-T1 modes of operation.

Table 15: BRIGHTLANE™ 88Q2221/88Q2221M Host Interfaces

BRIGHTLANE™ 88Q2221/88Q2221M Pin #	Pin Name	Pin Type	During Reset	Description
19	CONFIG5	O	Tri-state	Hardware configuration pin, CONFIG5
18	CONFIG4	O	Tri-state	Hardware configuration pin, CONFIG4
17 16 15 14	CONFIG0 CONFIG1 CONFIG2 CONFIG3	O	Tri-state	Hardware configuration pins, CONFIG3, CONFIG2, CONFIG1, and CONFIG0
27	SON	A, O	Tri-state	SGMII Out Negative
26	SOP	A, O	Tri-state	SGMII Out Positive
30	SIN	A, I	Tri-state	SGMII In Negative
29	SIP	A, I	Tri-state	SGMII In Positive

1.5.3 BRIGHTLANE™ 88Q2221/88Q2221M Management Interface

Table 16: BRIGHTLANE™ 88Q2221/88Q2221M Management Interface

BRIGHTLANE™ 88Q2221/88Q2221M Pin #	Pin Name	Pin Type	During Reset	Description
33	MDC	I	I	Management Interface Clock. A continuous clock stream is not required for MDC; Maximum frequency is 12.5 MHz.
34	MDIO	I/O	I	Management Interface Data. This pin requires a pull-up resistor with a resistance from 1.5 kΩ to 10 kΩ.

1.5.4 BRIGHTLANE™ 88Q2221/88Q2221M TX_ ENABLE/GPIO/Interrupt Interface

Table 17: BRIGHTLANE™ 88Q2221/88Q2221M TX_ENABLE/GPIO/Interrupt Interface

BRIGHTLANE™ 88Q2221/88Q2221M Pin #	Pin Name	Pin Type	During Reset	Description
36	LED/TX_ ENABLE	I/O	Tri-state with PU	Tx Enable/GPIO/LED. This pin is an input by default and used to implement a feature that allows blocking Tx packets. For details, see Section 2.2.3, Tx Disable Feature. This pin can be used as an GPIO/LED.
37	GPIO	I/O	Tri-state with PU	GPIO/LED Output/SyncE Recovered Clock Output. For hardware configuration details, see Section 2.19.1, Hardware Configuration.
32	INTn	O	Tri-state	Interrupt Output. By default, INTn is active LOW and will be in tri-state when inactive, so this requires an external pull-up (1.5 kΩ to 10 kΩ). This pin is programmable to be active high and will be in tristate when inactive, so this requires an external an external pull-down (1.5 kΩ to 10 kΩ) Refer to Section 2.17, Interrupt Interrupt for details.

1.5.5 BRIGHTLANE™ 88Q2221/88Q2221M Clock/Configuration/Reset/I/O

Table 18: BRIGHTLANE™ 88Q2221/88Q2221M Clock/Configuration/Reset/I/O

BRIGHTLANE™ 88Q2221/88Q2221M Pin #	Pin Name	Pin Type	During Reset	Description
10	XTAL_IN	I	I	Reference Clock. 25 MHz ±100 ppm tolerance crystal reference or oscillator input. When XTAL_IN is driven directly from the oscillator or clock buffer, this pin must be AC coupled with a 0.1 nF capacitor.
9	XTAL_OUT	O	Independent of Reset	Reference Clock. 25 MHz ±100 ppm tolerance crystal reference. When the XTAL_OUT pin is not connected to a crystal, it must be connected to ground through a 0.1 µF ceramic capacitor.
31	RESETn	I	Low	Hardware reset, active-low. 0 = Reset 1 = Normal operation

1.5.6 BRIGHTLANE™ 88Q2221/88Q2221M Control and Reference

Table 19: BRIGHTLANE™ 88Q2221/88Q2221M Control and Reference

BRIGHTLANE™ 88Q2221/88Q2221M Pin #	Pin Name	Pin Type	During Reset	Description
3	RSET	I, A	A	Constant Voltage Reference. For this pin, an external 4.99 kΩ, 1% resistor connection to VSS is required.

1.5.7 BRIGHTLANE™ 88Q2221/88Q2221M Test

Table 20: BRIGHTLANE™ 88Q2221/88Q2221M Test

BRIGHTLANE™ 88Q2221/88Q2221M Pin #	Pin Name	Pin Type	During Reset	Description
4	HSDAC	A, O	Tri-state	Analog AC Test Positive This pin can be left floating if not used.

1.5.8 BRIGHTLANE™ 88Q2221/88Q2221M Low Power Signal Detect

Table 21: BRIGHTLANE™ 88Q2221/88Q2221M Low Power Signal Detect

BRIGHTLANE™ 88Q2221/88Q2221M Pin #	Pin Name	Pin Type	During Reset	Description
39	WAKE_IN	A, I	I	Analog Wake Input This is used for local wake-up. This pin must be left floating when Low Power Signal Detect is not used.
1	VLPR	A	Analog	This is the regulated supply derived from battery. B0: May be left floating B2: Must be connected to a voltage per Table 51, LPSD Electrical Characteristics, on page 77.
2	VLPF	A	Analog	Connect to the external battery circuit. Refer the LPSD block diagram in Figure 22, LPSD Block Diagram — Option 1, on page 76. This pin must be left floating when LPSD circuit is not used.
40	INH	A, O	O	Output collector to control enable of the external regulator. To draw minimal current in deep sleep, INH has two states. ‘HIGH’ to drive the external regulator(s) enables signal (on), and tristate when in deep sleep. An external 10 kΩ pull-down is required at INH. This pin must be left floating when LPSD is not used.

1.5.9 BRIGHTLANE™ 88Q2221/88Q2221M Power, Ground, and Internal Regulators

Table 22: BRIGHTLANE™ 88Q2221/88Q2221M Power, Ground, and Internal Regulators

BRIGHTLANE™ 88Q2221/ 88Q2221M Pin #	Pin Name	Pin Type	During Reset	Description
8	AVDDL	Power	Analog Power	Analog Supply – 1.2V[1] AVDDL can be supplied externally with 1.2V or via the internal regulator generated 1.2V.
28	AVDDL	Power	Analog Power	Analog SERDES Supply – 1.2V AVDDL can be supplied externally with 1.2V or via the internal regulator generated 1.2V.
11	GND	Power	GND	Must be connected to GND.
12	AVDDL_CTRL	A, O	Analog	AVDDL Regulator Control, connect to external PNP. If the 1.2V regulator option is not used, then this pin must be left floating, no connect.
25	DVDD_Sense	I	I	DVDD_Sense input Connect the 0.75V[3] generated from external FET after inductor to DVDD_Sense. If the 0.75V[3] regulator option is not used, then this pin must be left floating, no connect.
23	DVDD_PDRV	O		Gate Driving Signal of External PFET If the 0.75V[3] regulator option is not used, then this pin must be left floating, no connect.
22	DVDD_Vx	I	I	Power Switch Sense If the 0.75V[3] regulator option is not used, then this pin must be left floating, no connect.
21	DVDD_NDRV	O		Gate Driving Signal of External NFET If the 0.75V[3] regulator option is not used, then this pin must be left floating, no connect.
5	AVDD33	Power	Analog Power	Analog Supply – 3.3V
24	VDD33 (REG_IN)	Power	Analog Power	Analog Supply for the Internal Regulator – 3.3V If the internal regulator is not used, then this pin must be left floating (No Connect). **CAUTION:** If the internal regulator is not used, then this pin must be left floating. Connecting this pin to either another power supply or to ground will damage the device.
20	VDDO	Power	Power	1.8V, 2.5V, or 3.3V I/O Supply[2]
35	VDDO	Power	Power	1.8V, 2.5V, or 3.3V I/O Supply[2]
13	DVDD	Power	Power	Digital Supply – 0.75V[3]
38	DVDD	Power	Power	Digital Supply – 0.75V[3]
E-PAD	VSS	GND	GND	Ground to Device. The 40-pin QFN package has an exposed die pad (E-PAD) at its base. This E-PAD must be soldered to VSS. For the exact location and dimensions of the E-PAD, see Section 5, Package Mechanical Dimensions.

1. AVDDL supplies the XTAL_IN and XTAL_OUT pins.

2. VDDO supplies the MDC, MDIO, RESETn, INTn, GPIO, TEST, and the host interface pins.
3. 0.75V applies for Rev B0/B1. 0.80V applies for Rev B2.

1.6 BRIGHTLANE™ 88Q2221/88Q2221M Pin Assignment List — Alphabetical by Signal Name

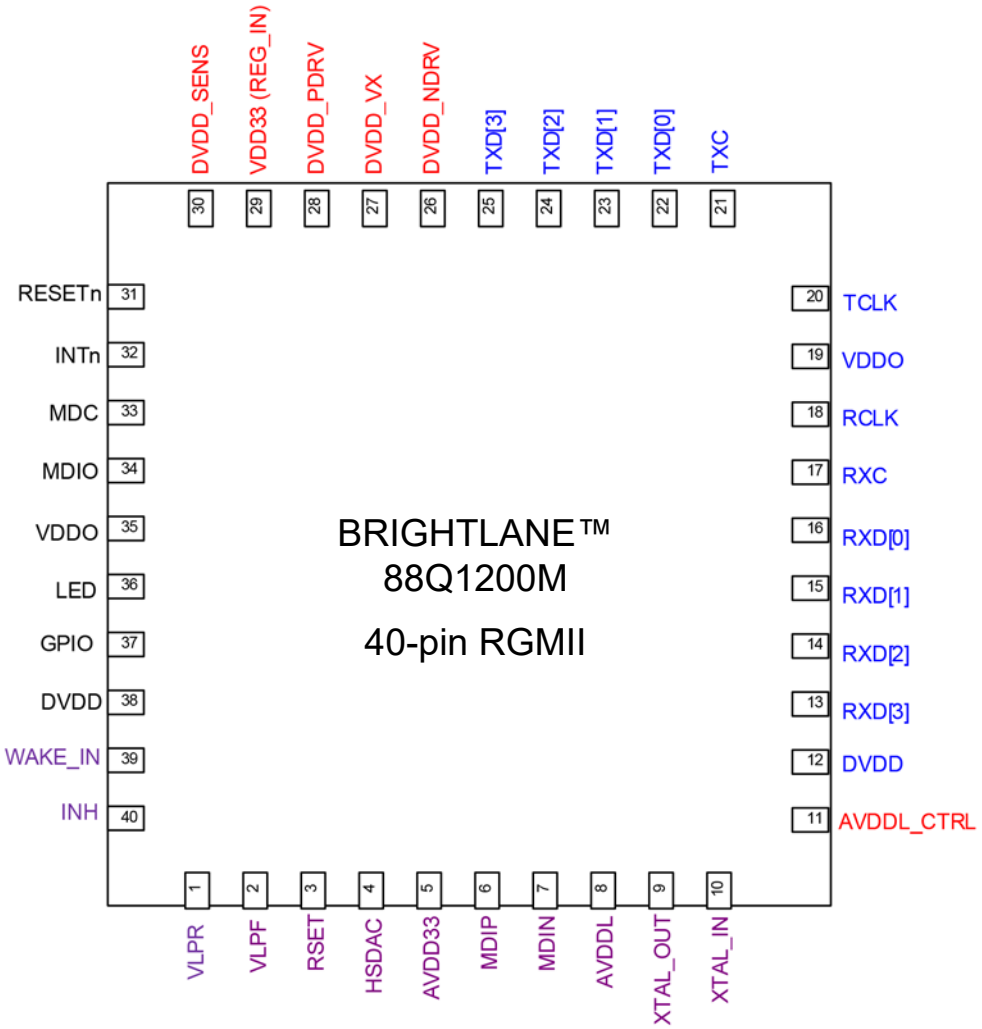
Table 23: BRIGHTLANE™ 88Q2221/88Q2221M 40-pin QFN Pin Assignment List — Alphabetical by Signal Name

Pin #	Pin Name	Pin #	Pin Name
5	AVDD33	19	RCLK
8	AVDDL	31	RESETn
28	AVDDL	3	RSET
12	AVDDL_CTRL	18	RXC/CONFIG4
11	GND	17	RXD[0]/CONFIG0
13	DVDD	16	RXD[1]/CONFIG1
38	DVDD	15	RXD[2]/CONFIG2
21	DVDD_NDRV	14	RXD[3/CONFIG3
23	DVDD_PDRV	30	SIN
25	DVDD_Sense	29	SIP
22	DVDD_Vx	27	SON
37	GPIO	26	SOP
4	HSDAC	2	VLPF
40	INH	1	VLPR
32	INTn	24	VDD33 (REG_IN)
36	LED	35	VDDO
33	MDC	20	VDDO
7	MDIN	E-PAD	VSS
34	MDIO	39	WAKE_IN
6	MDIP	10	XTAL_IN
		9	XTAL_OUT

1.7 BRIGHTLANE™ 88Q1200M Pinout

The BRIGHTLANE™ 88Q1200M device is a 100BASE-T1 Ethernet transceiver.

Figure 7: BRIGHTLANE™ 88Q1200M Device 40-pin RGMII Package (Top View)



1.8 BRIGHTLANE™ 88Q1200M Pin Descriptions

Table 24: BRIGHTLANE™ 88Q1200M Pin Type Definitions

Pin Type	Definition
A	Analog
H	Input with hysteresis
I/O	Input and output
I	Input only
O	Output only
PU	Internal pull-up
PD	Internal pull-down
D	Open drain output
Z	Tri-state output
mA	DC sink capability

1.8.1 BRIGHTLANE™ 88Q1200M Media Dependent Interface

Table 25: BRIGHTLANE™ 88Q1200M Media Dependent Interface

BRIGHTLANE™ 88Q1200M Pin #	Pin Name	Pin Type	During Reset	Description
7 6	MDIN MDIP	I/O	I	Media Dependent Interface. In 100BASE-T1, MDIN/P are used for transmit and receive.

1.8.2 BRIGHTLANE™ 88Q1200M Host Interfaces

The host interfaces support a 100BASE-T1 mode of operation.

Table 26: BRIGHTLANE™ 88Q1200M Host Interfaces

BRIGHTLANE™ 88Q1200M Pin #	Pin Name	Pin Type	During Reset	Description
20	TCLK	I	I	When RGMII is used, this pin is an input. • 100BASE-T1 mode: This pin must be driven with a 25 MHz clock with ±50 ppm tolerance.
21	TXC	I	I	When RGMII is used, this pin's signal must be presented according to the RGMII timing mode requirements.
25 24 23 22	TXD [3] TXD [2] TXD [1] TXD [0]	I	I	When RGMII is used, the signal for these pins must be presented according to the RGMII timing mode requirements. • 100BASE-T1 mode: Data is presented for sampling with the rising edge of TCLK only.
18	RCLK/CONFIG5	O	Tri-state	When RGMII is used, this pin is an output. • 100BASE-T1 mode: This pin is an output that drives out a 25 MHz clock with ±50 ppm tolerance. Hardware configuration pin, CONFIG5

Table 26: BRIGHTLANE™ 88Q1200M Host Interfaces (Continued)

BRIGHTLANE™ 88Q1200M Pin #	Pin Name	Pin Type	During Reset	Description
17	RXC/CONFIG4	O	Tri-state	When RGMII is used, this pin's signal must be presented according to the RGMII timing mode requirements. Hardware configuration pin, CONFIG4
13 14 15 16	RXD[3]/CONFIG3 RXD[2]/CONFIG2 RXD[1]/CONFIG1 RXD[0]/CONFIG0	O	Tri-state	When RGMII is used, the signal for these pins must be presented according to the RGMII timing mode requirements. • 100BASE-T1 mode: Data is presented for sampling with the rising edge of RCLK only. Hardware configuration pins, CONFIG3, CONFIG2, CONFIG1, and CONFIG0

1.8.3 BRIGHTLANE™ 88Q1200M Management Interface

Table 27: BRIGHTLANE™ 88Q1200M Management Interface

BRIGHTLANE™ 88Q1200M Pin #	Pin Name	Pin Type	During Reset	Description
33	MDC	I	I	Management Interface Clock. A continuous clock stream is not required for MDC; Maximum frequency is 12.5 MHz.
34	MDIO	I/O	I	Management Interface Data. This pin requires a pull-up resistor with a resistance from 1.5 kΩ to 10 kΩ.

1.8.4 BRIGHTLANE™ 88Q1200M TX_ENABLE/GPIO/Interrupt Interface

Table 28: BRIGHTLANE™ 88Q1200M TX_ENABLE/GPIO/Interrupt Interface

BRIGHTLANE™ 88Q1200M Pin #	Pin Name	Pin Type	During Reset	Description
36	LED/TX_ENABLE	I/O	Tri-state with PU	Tx Enable/GPIO/LED. This pin is an input by default and used to implement a feature that allows blocking Tx packets. For details, see Section 2.2.3, Tx Disable Feature. This pin can be used as an GPIO/LED.
37	GPIO	I/O	Tri-state with PU	GPIO/LED Output/SyncE Recovered Clock Output. For hardware configuration details, see Section 2.19.1, Hardware Configuration.
32	INTn	O, D	Tri-state	Interrupt Output.

1.8.5 BRIGHTLANE™ 88Q1200M Clock/Configuration/Reset/I/O

Table 29: BRIGHTLANE™ 88Q1200M Clock/Configuration/Reset/I/O

BRIGHTLANE™ 88Q1200M Pin #	Pin Name	Pin Type	During Reset	Description
10	XTAL_IN	I	I	Reference Clock. 25 MHz ±100 ppm tolerance crystal reference or oscillator input. When XTAL_IN is driven directly from the oscillator or clock buffer, this pin must be AC coupled with a 0.1 nF capacitor.
9	XTAL_OUT	O	Independent of Reset	Reference Clock. 25 MHz ±100 ppm tolerance crystal reference. When the XTAL_OUT pin is not connected to a crystal, it must be connected to ground through a 0.1 µF ceramic capacitor.
31	RESETn	I	Low	Hardware reset, active-low. 0 = Reset 1 = Normal operation

1.8.6 BRIGHTLANE™ 88Q1200M Control and Reference

Table 30: BRIGHTLANE™ 88Q1200M Control and Reference

BRIGHTLANE™ 88Q1200M Pin #	Pin Name	Pin Type	During Reset	Description
3	RSET	I, A	A	Constant Voltage Reference. For this pin, an external 4.99 kΩ, 1% resistor connection to VSS is required.

1.8.7 BRIGHTLANE™ 88Q1200M Test

Table 31: BRIGHTLANE™ 88Q1200M Test

BRIGHTLANE™ 88Q1200M Pin #	Pin Name	Pin Type	During Reset	Description
4	HSDAC	A, O	Tri-state	Analog AC Test Positive This pin can be left floating if not used.

1.8.8 BRIGHTLANE™ 88Q1200M Low Power Signal Detect

Table 32: BRIGHTLANE™ 88Q1200M Low Power Signal Detect

BRIGHTLANE™ 88Q1200M Pin #	Pin Name	Pin Type	During Reset	Description
39	WAKE_IN	A, I	I	Analog Wake Input This is used for local wake-up. This pin must be left floating when Low Power Signal Detect is not used.
1	VLPR	A	Analog Power	This is the regulated supply derived from battery. B0: May be left floating B2: Must be connected to a voltage per Table 51, LPSD Electrical Characteristics, on page 77.
2	VLPF	A	A	Connect to the external battery circuit. Refer the LPSD block diagram in Figure 22, LPSD Block Diagram — Option 1, on page 76. This pin must be left floating when LPSD circuit is not used.
40	INH	A, O	O	Output collector to control enable of the external regulator. To draw minimal current in deep sleep, INH has two states. ‘HIGH’ to drive the external regulator(s) enables signal (on), and tristate when in deep sleep. An external 10 kΩ pull-down is required at INH. This pin must be left floating when LPSD is not used.

1.8.9 BRIGHTLANE™ 88Q1200M Power, Ground, and Internal Regulators

Table 33: BRIGHTLANE™ 88Q1200M Power, Ground, and Internal Regulators

BRIGHTLANE™ 88Q1200M Pin #	Pin Name	Pin Type	During Reset	Description
8	AVDDL	Power	Analog Power	Analog Supply – 1.2V[1] AVDDL can be supplied externally with 1.2V or via the internal regulator generated 1.2V.
11	AVDDL_ CTRL	A, O	Analog	AVDDL Regulator Control, connect to external PNP. If the 1.2V regulator option is not used, then this pin must be left floating, no connect.
30	DVDD_ Sense	Power	Power	DVDD_Sense input Connect the 0.75V[3] generated from external FET after inductor to DVDD_Sense. If the 0.75V[3] regulator option is not used, then this pin must be left floating, no connect.
28	DVDD_ PDRV	Power	Power	Gate Driving Signal of External PFET If the 0.75V[3] regulator option is not used, then this pin must be left floating, no connect.
27	DVDD_Vx	Power	Power	Power Switch Sense If the 0.75V[3] regulator option is not used, then this pin must be left floating, no connect.
26	DVDD_ NDRV	Power	Power	Gate Driving Signal of External NFET If the 0.75V[3] regulator option is not used, then this pin must be left floating, no connect.
5	AVDD33	Power	Power	Analog Supply – 3.3V.
29	VDD33 (REG_IN)	Power	Power	Analog Supply for the Internal Regulator – 3.3V If the internal regulator is not used, then this pin must be left floating (No Connect). Leave regulator control pins floating when regulators not used. **CAUTION:** If the internal regulator is not used, then this pin must be left floating. Connecting this pin to either another power supply or to ground will damage the device.
19	VDDO	Power	Power	1.8V, 2.5V, or 3.3V I/O Supply[2]
35	VDDO	Power	Power	1.8V, 2.5V, or 3.3V I/O Supply[2]
38, 12	DVDD	Power	Power	Digital Supply – 0.75V[3]
E-PAD	VSS	GND	GND	Ground to Device. The 40-pin QFN package has an exposed die pad (E-PAD) at its base. This E-PAD must be soldered to VSS. For the exact location and dimensions of the E-PAD, see Section 5, Package Mechanical Dimensions.

1. AVDDL supplies the XTAL_IN and XTAL_OUT pins.
2. VDDO supplies the MDC, MDIO, RESETn, INTn, GPIO, TEST, and the host interface pins.
3. 0.75V applies for Rev B0/B1. 0.80V applies for Rev B2.

1.9 BRIGHTLANE™ 88Q1200M Pin Assignment List — Alphabetical by Signal Name

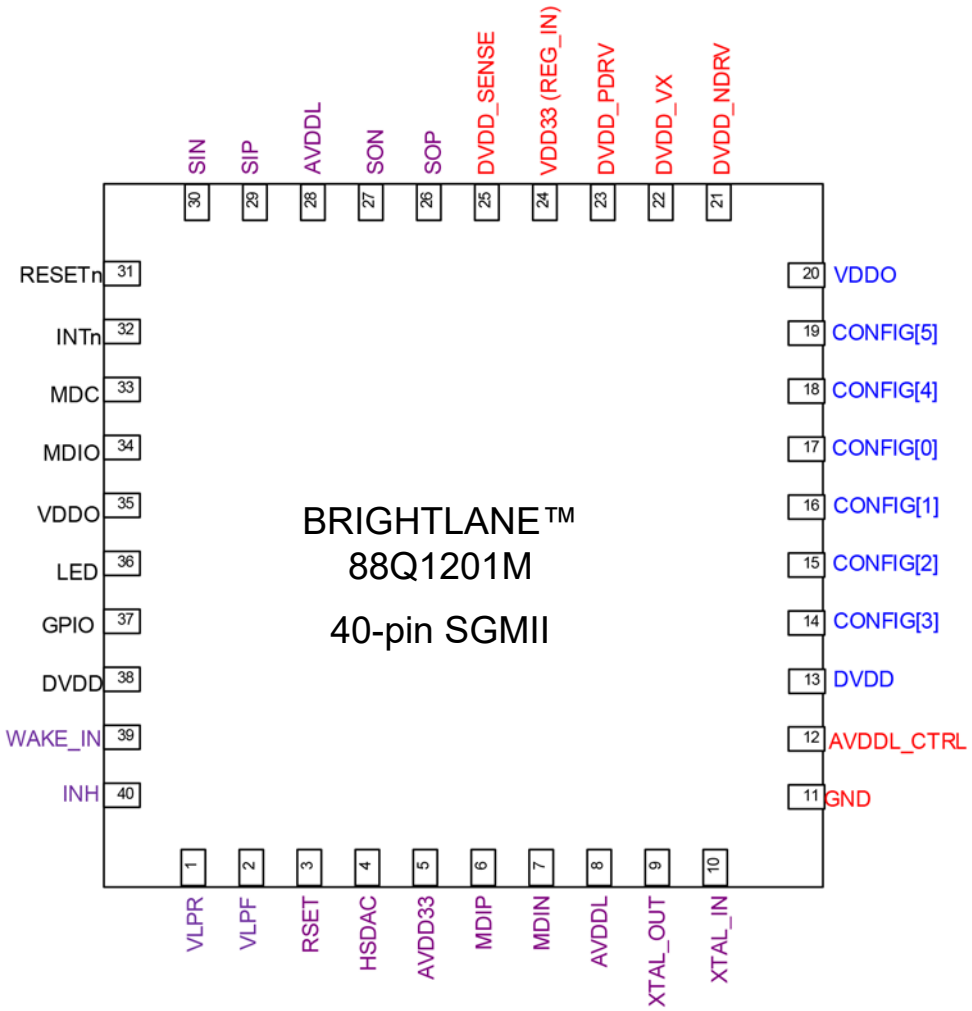
Table 34: BRIGHTLANE™ 88Q1200M 40-pin QFN Pin Assignment List — Alphabetical by Signal Name

Pin #	Pin Name	Pin #	Pin Name
5	AVDD33	3	RSET
8	AVDDL	17	RXC/CONFIG4
11	AVDDL_CTRL	13	RXD[3/CONFIG3
38	DVDD	14	RXD[2]/CONFIG2
26	DVDD_NDRV	16	RXD[0]/CONFIG0]
28	DVDD_PDRV	20	TCLK
30	DVDD_Sense	21	TXC
27	DVDD_Vx	22	TXD[0]
37	GPIO	15	RXD[1]/CONFIG1
37	GPIO	23	TXD[1]
4	HSDACP	24	TXD[2]
40	INH	25	TXD[3]
32	INTn	2	VLPF
36	LED	1	VLPR
33	MDC	29	VDD33 (REG_IN)
7	MDIN	19	VDDO
34	MDIO	35	VDDO
6	MDIP	E-PAD	VSS
18	RCLK/CONFIG5	39	WAKE_IN
31	RESETn	10	XTAL_IN
		9	XTAL_OUT

1.10 BRIGHTLANE™ 88Q1201M Pinout

The BRIGHTLANE™ 88Q1201M device is a 100BASE-T1 Ethernet transceiver.

Figure 8: BRIGHTLANE™ 88Q1201M Device 40-pin SGMII Package (Top View)



1.11 BRIGHTLANE™ 88Q1201M Pin Descriptions

Table 35: BRIGHTLANE™ 88Q1201M Pin Type Definitions

Pin Type	Definition
A	Analog
H	Input with hysteresis
I/O	Input and output
I	Input only
O	Output only
PU	Internal pull-up
PD	Internal pull-down
D	Open drain output
Z	Tri-state output
mA	DC sink capability

1.11.1 BRIGHTLANE™ 88Q1201M Media Dependent Interface

Table 36: BRIGHTLANE™ 88Q1201M Media Dependent Interface

BRIGHTLANE™ 88Q1201M Pin #	Pin Name	Pin Type	During Reset	Description
7 6	MDIN MDIP	I/O	Tri-state	Media Dependent Interface. In 100BASE-T1, MDIN/P are used for transmit and receive.

1.11.2 BRIGHTLANE™ 88Q1201M Host Interfaces

The host interfaces supports a 100BASE-T1 mode of operation.

Table 37: BRIGHTLANE™ 88Q1201M Host Interfaces

BRIGHTLANE™ 88Q1201M Pin #	Pin Name	Pin Type	During Reset	Description
19	CONFIG5	O	Tri-state	Hardware configuration pin, CONFIG5
18	CONFIG4	O	Tri-state	Hardware configuration pin, CONFIG4
17 16 15 14	CONFIG0 CONFIG1 CONFIG2 CONFIG3	O	Tri-state	Hardware configuration pins, CONFIG3, CONFIG2, CONFIG1, and CONFIG0
27	SON	A, O	Tri-state	SGMII Out Negative
26	SOP	A, O	Tri-state	SGMII Out Positive
30	SIN	A, I	Tri-state	SGMII In Negative
29	SIP	A, I	Tri-state	SGMII In Positive

1.11.3 BRIGHTLANE™ 88Q1201M Management Interface

Table 38: BRIGHTLANE™ 88Q1201M Management Interface

BRIGHTLANE™ 88Q1201M Pin #	Pin Name	Pin Type	During Reset	Description
33	MDC	I	I	Management Interface Clock. A continuous clock stream is not required for MDC; Maximum frequency is 12.5 MHz.
34	MDIO	I/O	I	Management Interface Data. This pin requires a pull-up resistor with a resistance from 1.5 kΩ to 10 kΩ.

1.11.4 BRIGHTLANE™ 88Q1201M TX_ENABLE/GPIO/Interrupt Interface

Table 39: BRIGHTLANE™ 88Q1201M TX_ENABLE/GPIO/Interrupt Interface

BRIGHTLANE™ 88Q1201M Pin #	Pin Name	Pin Type	During Reset	Description
36	LED/TX_ ENABLE	I/O	Tri-state with PU	Tx Enable/GPIO/LED. This pin is an input by default and used to implement a feature that allows blocking Tx packets. For details, see Section 2.2.3, Tx Disable Feature. This pin can be used as an GPIO/LED.
37	GPIO	I/O	Tri-state with PU	GPIO/LED Output/SyncE Recovered Clock Output. For hardware configuration details, see Section 2.19.1, Hardware Configuration.
32	INTn	O	Tri-state	Interrupt Output. By default, INTn is active LOW and will be in tri-state when inactive, so this requires an external pull-up (1.5 kΩ to 10 kΩ). This pin is programmable to be active high and will be in tristate when inactive, so this requires an external an external pull-down (1.5 kΩ to 10 kΩ) Refer to Section 2.17, Interrupt Interrupt for details.

1.11.5 BRIGHTLANE™ 88Q1201M Clock/Configuration/Reset/I/O

Table 40: BRIGHTLANE™ 88Q1201M Clock/Configuration/Reset/I/O

BRIGHTLANE™ 88Q1201M Pin #	Pin Name	Pin Type	During Reset	Description
10	XTAL_IN	I	I	Reference Clock. 25 MHz ±100 ppm tolerance crystal reference or oscillator input. When XTAL_IN is driven directly from the oscillator or clock buffer, this pin must be AC coupled with a 0.1 nF capacitor.
9	XTAL_OUT	O	Independent of Reset	Reference Clock. 25 MHz ±100 ppm tolerance crystal reference. When the XTAL_OUT pin is not connected to a crystal, it must be connected to ground through a 0.1 µF ceramic capacitor.
31	RESETn	I	Low	Hardware reset, active-low. 0 = Reset 1 = Normal operation

1.11.6 BRIGHTLANE™ 88Q1201M Control and Reference

Table 41: BRIGHTLANE™ 88Q1201M Control and Reference

BRIGHTLANE™ 88Q1201M Pin #	Pin Name	Pin Type	During Reset	Description
3	RSET	I, A	A	Constant Voltage Reference. For this pin, an external 4.99 kΩ, 1% resistor connection to VSS is required.

1.11.7 BRIGHTLANE™ 88Q1201M Test

Table 42: BRIGHTLANE™ 88Q1201M Test

BRIGHTLANE™ 88Q1201M Pin #	Pin Name	Pin Type	During Reset	Description
4	HSDAC	A, O	Tri-state	Analog AC Test Positive This pin can be left floating if not used.

1.11.8 BRIGHTLANE™ 88Q1201M Low Power Signal Detect

Table 43: BRIGHTLANE™ 88Q1201M Low Power Signal Detect

BRIGHTLANE™ 88Q1201M Pin #	Pin Name	Pin Type	During Reset	Description
39	WAKE_IN	A, I	I	Analog Wake Input This is used for local wake-up. This pin must be left floating when Low Power Signal Detect is not used.
1	VLPR	A	Analog	This is the regulated supply derived from battery. B0: May be left floating B2: Must be connected to a voltage per Table 51, LPSD Electrical Characteristics, on page 77.
2	VLPF	A	Analog	Connect to the external battery circuit. Refer the LPSD block diagram in Figure 22, LPSD Block Diagram — Option 1, on page 76. This pin must be left floating when LPSD circuit is not used.
40	INH	A, O	O	Output collector to control enable of the external regulator. To draw minimal current in deep sleep, INH has two states. ‘HIGH’ to drive the external regulator(s) enables signal (on), and tristate when in deep sleep. An external 10 kΩ pull-down is required at INH. This pin must be left floating when LPSD is not used.

1.11.9 BRIGHTLANE™ 88Q1201M Power, Ground, and Internal Regulators

Table 44: BRIGHTLANE™ 88Q1201M Power, Ground, and Internal Regulators

BRIGHTLANE™ 88Q1201M Pin #	Pin Name	Pin Type	During Reset	Description
8	AVDDL	Power	Analog Power	Analog Supply – 1.2V[1] AVDDL can be supplied externally with 1.2V or via the internal regulator generated 1.2V.
28	AVDDL	Power	Analog Power	Analog SERDES Supply – 1.2V AVDDL can be supplied externally with 1.2V or via the internal regulator generated 1.2V.
11	GND	A, O	GND	Must be connected to GND.
12	AVDDL_CTRL	A, O	Analog	AVDDL Regulator Control, connect to external PNP. If the 1.2V regulator option is not used, then this pin must be left floating, no connect.
25	DVDD_Sense	Power	Power	DVDD_Sense input Connect the 0.75V[3] generated from external FET after inductor to DVDD_Sense. If the 0.75V regulator option is not used, then this pin must be left floating, no connect.
23	DVDD_PDRV	Power	Power	Gate Driving Signal of External PFET If the 0.75V[3] regulator option is not used, then this pin must be left floating, no connect.
22	DVDD_Vx	Power	Power	Power Switch Sense If the 0.75V[3] regulator option is not used, then this pin must be left floating, no connect.
21	DVDD_NDRV	Power	Power	Gate Driving Signal of External NFET If the 0.75V[3] regulator option is not used, then this pin must be left floating, no connect.
5	AVDD33	Power	Analog Power	Analog Supply – 3.3V.
24	VDD33 (REG_IN)	Power	Analog Power	Analog Supply for the Internal Regulator – 3.3V. If the internal regulator is not used, then this pin must be left floating (No Connect). **CAUTION:** If the internal regulator is not used, then this pin must be left floating. Connecting this pin to either another power supply or to ground will damage the device.
20	VDDO	Power	Power	1.8V, 2.5V, or 3.3V I/O Supply[2]
35	VDDO	Power	Power	1.8V, 2.5V, or 3.3V I/O Supply[2]
13	DVDD	Power	Power	Digital Supply – 0.75V[3]

Table 44: BRIGHTLANE™ 88Q1201M Power, Ground, and Internal Regulators (Continued)

BRIGHTLANE™ 88Q1201M Pin #	Pin Name	Pin Type	During Reset	Description
38	DVDD	Power	Power	Digital Supply – 0.75V[3]
E-PAD	VSS	GND	GND	Ground to Device. The 40-pin QFN package has an exposed die pad (E-PAD) at its base. This E-PAD must be soldered to VSS. For the exact location and dimensions of the E-PAD, see Section 5, Package Mechanical Dimensions.

1. AVDDL supplies the XTAL IN and XTAL OUT pins.
2. VDDO supplies the MDC, MDIO, RESETn, INTn, GPIO, TEST, and the host interface pins.
3. 0.75V applies for Rev B0/B1. 0.80V applies for Rev B2.

1.12 BRIGHTLANE™ 88Q1201M Pin Assignment List — Alphabetical by Signal Name

Table 45: BRIGHTLANE™ 88Q1201M 40-pin QFN Pin Assignment List — Alphabetical by Signal Name

Pin #	Pin Name	Pin #	Pin Name
5	AVDD33	19	RCLK
8	AVDDL	31	RESETn
28	AVDDL	3	RSET
12	AVDDL_CTRL	18	RXC/CONFIG4
11	GND	17	RXD[0]/CONFIG0
13	DVDD	16	RXD[1]/CONFIG1
38	DVDD	15	RXD[2]/CONFIG2
21	DVDD_NDRV	14	RXD[3/CONFIG3
23	DVDD_PDRV	30	SIN
25	DVDD_Sense	29	SIP
22	DVDD_Vx	27	SON
37	GPIO	26	SOP
4	HSDACP	2	VLPF
40	INH	1	VLPR
32	INTn	24	VDD33 (REG_IN)
36	LED	35	VDDO
33	MDC	20	VDDO
7	MDIN	E-PAD	VSS
34	MDIO	39	WAKE_IN
6	MDIP	10	XTAL_IN
		9	XTAL_OUT

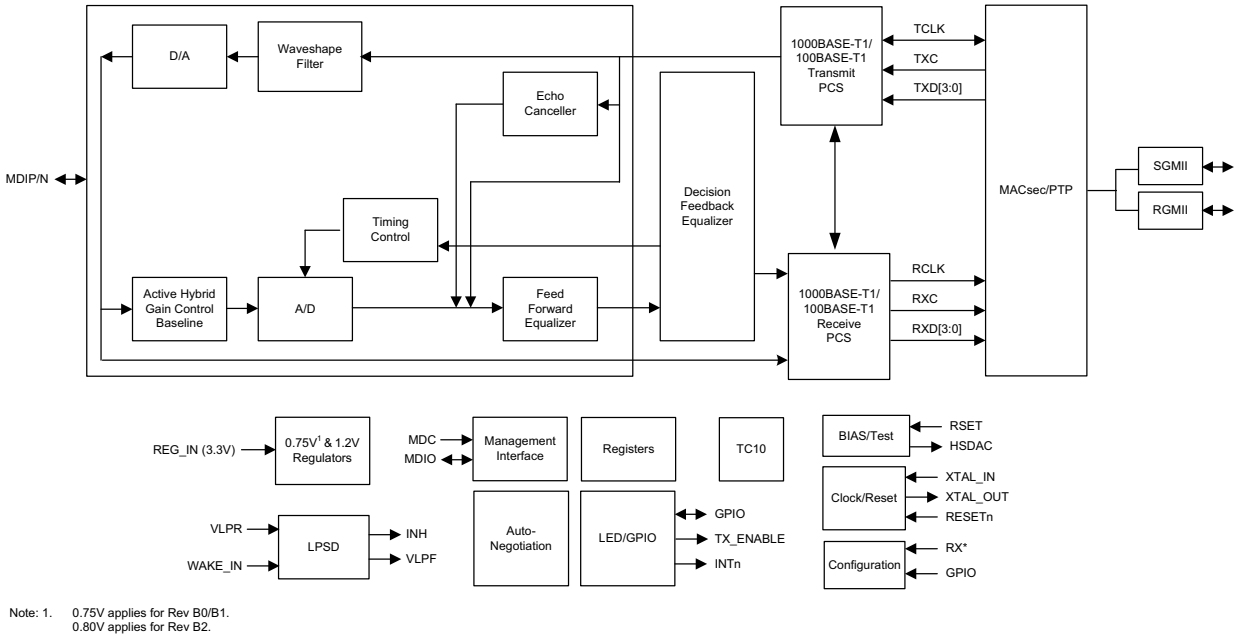
2 PHY Functional Specifications

The device is a 100BASE-T1/1000BASE-T1 Ethernet transceiver. Figure 9 shows the functional block diagrams of the BRIGHTLANE™ 88Q2220M/88Q2221M and Figure 10 shows BRIGHTLANE™ 88Q2220/88Q2221 devices. Figure 11 shows the functional block diagram of the BRIGHTLANE™ 88Q1200M device and Figure 12 shows the functional block diagram of the BRIGHTLANE™ 88Q1201M device.

Note

Refer to the Product Overview for a list of features supported by the devices.

Figure 9: BRIGHTLANE™ 88Q2220M/88Q2221M Functional Block Diagram

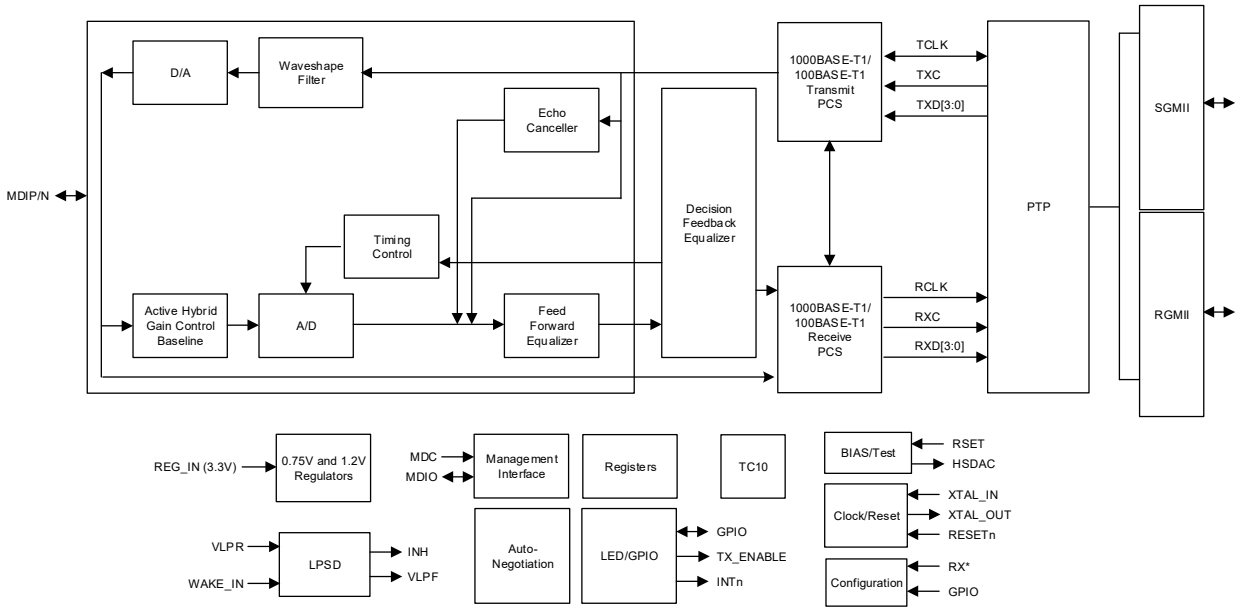


Note: 1. 0.75V applies for Rev B0/B1.
0.80V applies for Rev B2.

Note

RGMII is only available in the BRIGHTLANE™ 88Q2220/88Q2220M devices and SGMII is only available in the BRIGHTLANE™ 88Q2221/88Q2221M devices.

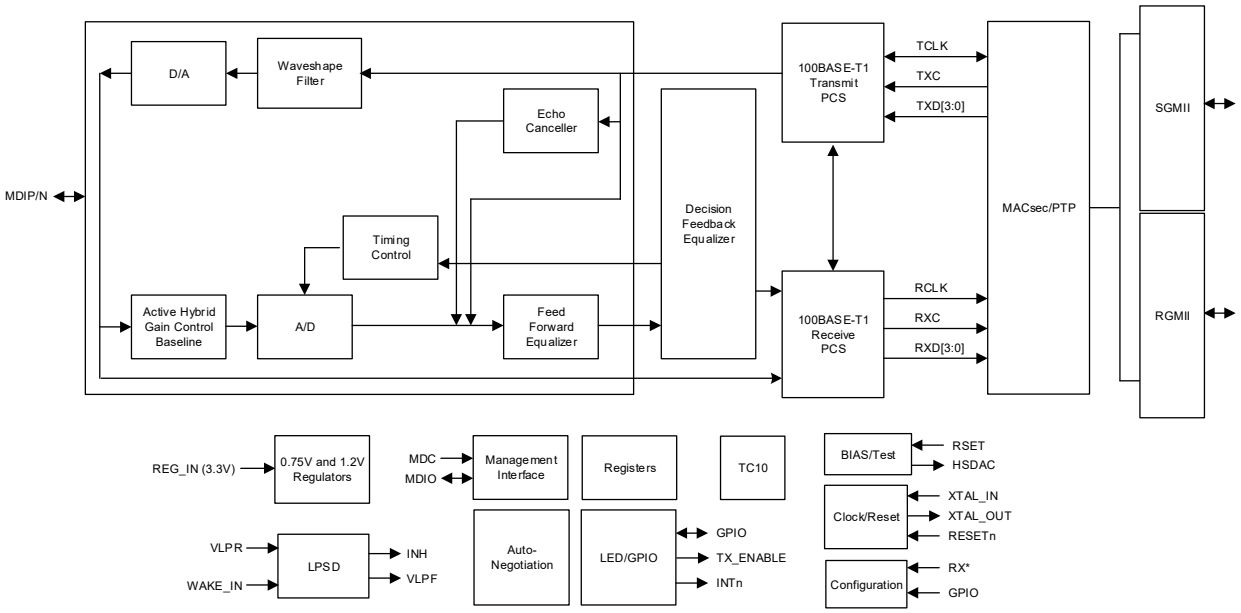
Figure 10: BRIGHTLANE™ 88Q2220/88Q2221 Functional Block Diagram



Note

RGMII is only available in the BRIGHTLANE™ 88Q2220/88Q2220M devices and SGMII is only available in the BRIGHTLANE™ 88Q2221/88Q2221M devices.

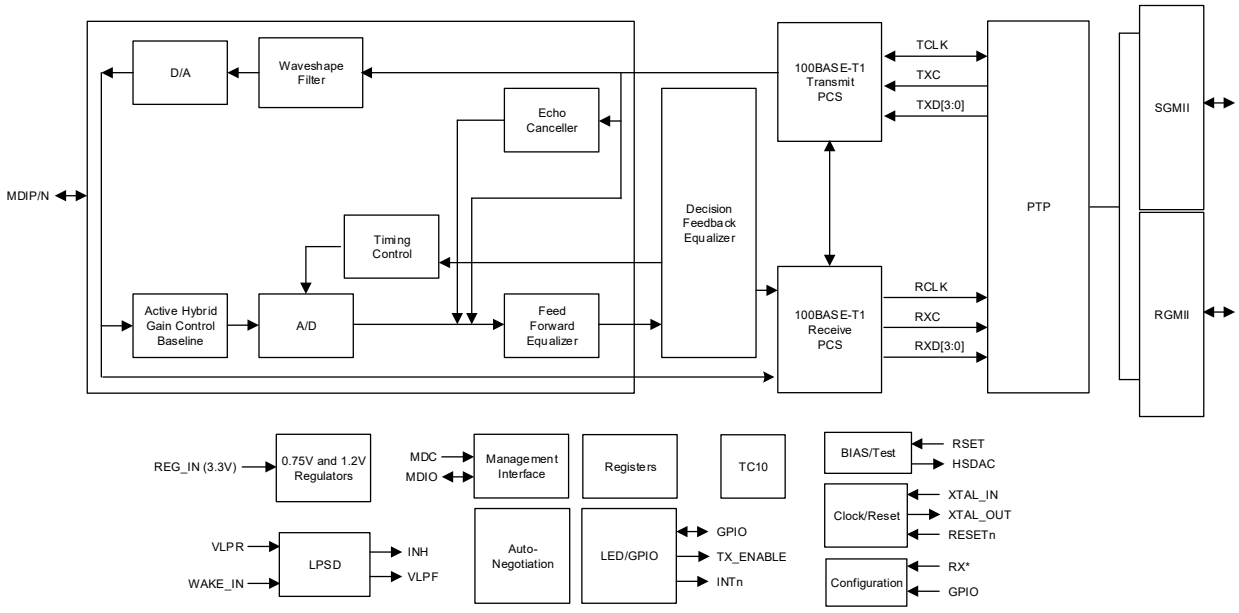
Figure 11: BRIGHTLANE™ 88Q1200M Functional Block Diagram



Note

RGMII is only available in the BRIGHTLANE™ 88Q1200M devices and SGMII is only available in the BRIGHTLANE™ 88Q1201M devices.

Figure 12: BRIGHTLANE™ 88Q1201 Functional Block Diagram



Note

RGMII is only available in the BRIGHTLANE™ 88Q1200M devices and SGMII is only available in the BRIGHTLANE™ 88Q1201M devices.

2.1 Copper Media Interface

The copper interface consists of the MDIP/N pins that connect to the physical media for 100BASE-T1/1000BASE-T1 mode of operation.

The device integrates MDI interface termination resistors. The IEEE 802.3 specification requires that both sides of a link have termination resistors to prevent reflections. Traditionally, these resistors and additional capacitors are placed on the board between a PHY device and the connector. The resistors must be very accurate to meet the strict IEEE return loss requirements. Typically, ±1% accuracy resistors are used on the board. These additional components between the PHY and the connector complicates board layout. Integrating the resistors has many advantages, including component cost savings, better in-circuit test (ICT) yield, board reliability improvements, board area savings, improved layout, and signal integrity improvements.

2.1.1 Transmit Side Network Interface

2.1.1.1 Multi-mode Tx Digital-to-Analog Converter

The device incorporates a transmit DAC to generate filtered 3-level pulse amplitude modulation (PAM3) symbols. The transmit DAC performs signal wave shaping to reduce EMI. The transmit DAC is designed for very low parasitic loading capacitances to improve the return loss requirement.

2.1.1.2 Slew Rate Control and Waveshaping

Slew rate control is used to minimize high-frequency EMI.

2.1.2 Encoder

2.1.2.1 100/1000BASE-T1

The transmit data nibbles are organized into groups of three bits. These 3-bit symbols are scrambled and encoded into two PAM3 symbols. This prevents link partners from outputting the same sequence during idle to help reduce EMI.

2.1.3 Receive Side Network Interface

2.1.3.1 Analog-to-Digital Converter

The device incorporates an advanced high-speed ADC on the receive channel. Higher resolution ADC results in better SNR, and lower error rates. Patented architectures and design techniques result in high differential and integral linearity, high power-supply noise rejection, and low metastability error rate.

2.1.3.2 Analog Active Hybrid

The device employs a sophisticated on-chip hybrid to substantially reduce the near-end echo, which is the super-imposed transmit signal on the receive signal. The hybrid minimizes the echo to reduce the precision requirement of the digital echo canceller. The on-chip hybrid allows both the transmitter and receiver to be coupled to and share the twisted pair cable, which reduces the cost of the overall system.

2.1.3.3 Digital Echo Canceller

Residual echo not removed by the hybrid and echo due to patch cord impedance mismatch, patch panel discontinuity, and variations in cable impedance along the twisted pair cable result in drastic SNR degradation on the receive signal. The device employs a fully developed digital echo canceller to adjust for echo impairments from more than 15 meters of cable. The echo canceller is fully adaptive to compensate for the time varying nature of channel conditions.

2.1.3.4 Digital Adaptive Equalizer

The digital adaptive equalizer removes inter-symbol interference at the receiver. The digital adaptive equalizer takes unequalized signals from the ADC output and uses a combination of feed-forward equalizer (FFE) and decision feedback equalizer (DFE) for the best-optimized signal-to-noise ratio (SNR).

2.1.3.5 Digital Phase-Locked Loop

The slave transmitter must use the exact receive clock frequency it sees on the receive signal. Any slight long-term frequency phase jitter (frequency drift) on the receive signal must be tracked and duplicated by the slave transmitter; otherwise, the receivers of both the slave and master physical layer devices have difficulty resolving receive symbols due to unreliable synchronization; this results in higher bit error rates. In the device, an advanced digital phase-locked loop (DPLL) is used to recover and track the clock timing information from the receive signal. This DPLL has very low long-term phase jitter of its own which maximizes the achievable SNR.

2.1.3.6 Link Monitor

The link monitor is responsible for determining if a link is established with a link partner. Link is established by scrambled idles.

2.1.4 Decoder

The receive idle stream is analyzed so that the scrambler seed and the polarity of the pair can be accounted for. When calibrated, the PAM3 symbols are converted to 2-bit symbols, which are then descrambled and sent to the host side. If the descrambler loses lock due to excessive Reed-Solomon uncorrectable errors in 1000BASE-T1 or high CRC mismatch count in 100BASE-T1 mode, then the link is brought down and calibration is restarted.

2.2 MAC Interfaces

2.2.1 RGMII Interface

The device supports an RGMII interface. Four RGMII timing modes with different receive clock to data timing and transmit clock to data timing can be programmed by setting register 4.A001.15:14. For timing details, see Section 4.9.2, RGMII Delay Timing for Different RGMII Modes, on page 472.

Table 46: RGMII Signal Mapping

Device Pin Name	RGMII Specification Pin Name	Description
TCLK	TXC	125 MHz transmit clock with ±50 ppm tolerance.
TXC	TX_CTL	Transmit Control Signals. TX_EN is encoded on the rising edge of TCLK. TX_ER XOR'ed with TX_EN is encoded on the falling edge of TCLK.
TXD [3:0]	TD [3:0]	For 1000BASE-T1 mode, TXD [3:0] are synchronous with the rising and falling edge of TCLK. For 100BASE-T1 mode, TXD [3:0] are synchronous with the rising edge of TCLK.
RCLK	RXC	125 MHz receive clock derived from the received data stream.
RXC	RX_CTL	Receive Control Signals. RX_DV is encoded on the rising edge of RCLK. RX_ER XOR'ed with RX_DV is encoded on the falling edge of RCLK.
RXD [3:0]	RD [3:0]	For 1000BASE-T1 mode, RXD [3:0] are synchronous with the rising and falling edge of RCLK. For 100BASE-T1 mode, RXD [3:0] are synchronous with the rising edge of RCLK.

The default 4.A001.15:14 as defined in Table 47; the delay of TCLK and RCLK is based on the value set in this register. For optimal design flexibility, the delay of TCLK and RCLK can also be controlled by reprogramming register 4.A001.15:14. For a detailed timing requirement for all modes, see Section 4.9, MAC Interface Timing, on page 471.

Table 47: Modes

Mode	Description	4.A001.15:14
RGMII	TCLK (input) transitions when TXD/TXC is stable. RCLK (output) transitions when RXD/RXC is stable. TCLK and RCLK are 25 MHz or 125 MHz. This is a DDR interface.	11

2.2.2 SGMII Interface

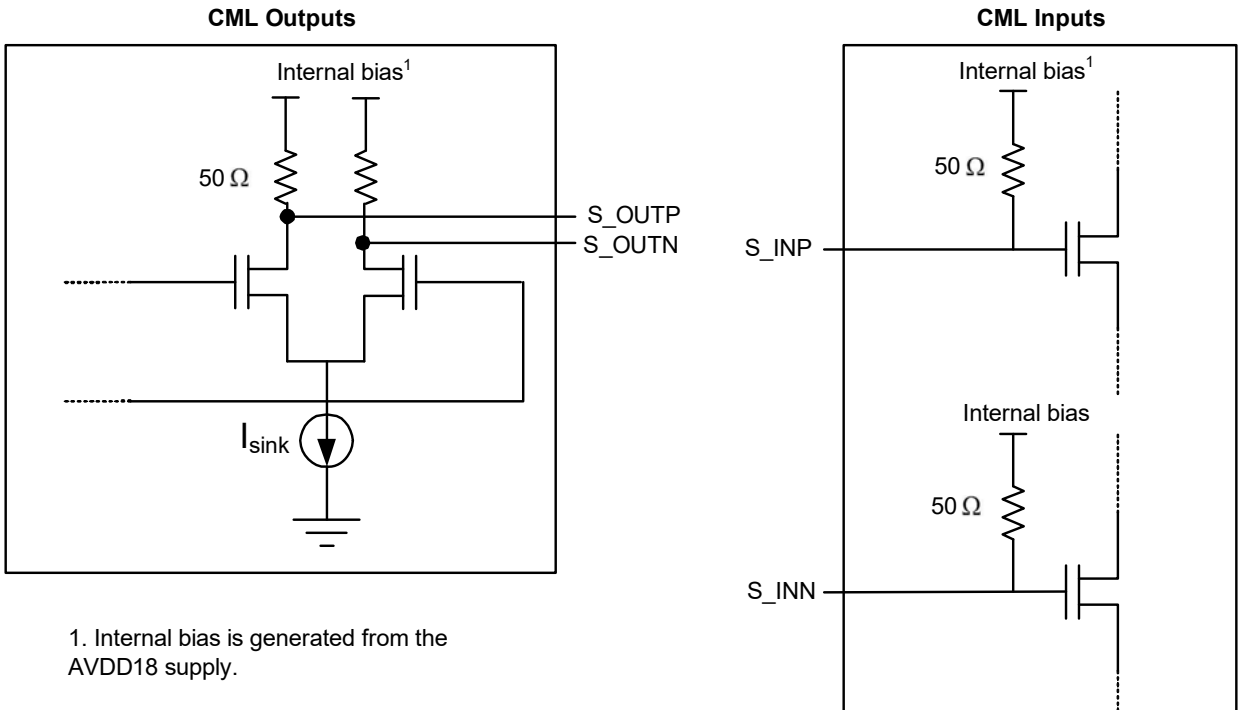
The device supports the SGMII specification revision 1.8, except for the carrier extension block that must be carried out in software. This interface supports 100BASE-T1 and 1000 Mbps mode of operation.

2.2.2.1 1.25 GHz SERDES Interface

The 1.25 GHz SERDES interface can be configured as an SGMII to be hooked up to a MAC.

The input and output buffers of the 1.25 GHz SERDES interface are internally terminated by 50Ω impedance. No external terminations are required. The output swing can be adjusted by internal registers within the SerDes block. The 1.25 GHz SERDES I/Os are current mode logic (CML) buffers. CML I/Os can be used to connect to other components with PECL or LVDS I/Os.

Figure 13: CML I/Os



1. Internal bias is generated from the AVDD18 supply.

2.2.2.2 SGMII Speed and Link

Two registers are available to determine whether the SGMII achieved link and sync. Status Register 4.8011.5 indicates that the SERDES locked onto the incoming KDKDKD… sequence. Register 4.8011.10 indicates whether a link is established on the SERDES. If SGMII Auto-Negotiation is disabled, then register 4.8011.10 has the same meaning as register 4.8011.5. If SGMII Auto-Negotiation is enabled, then register 4.8011.10 indicates whether SGMII Auto-Negotiation successfully established the link.

2.2.2.3 SGMII TRR Blocking

When the SGMII receives a packet with odd number of bytes, a single symbol of carrier extension will be passed on and transmitted onto 1000BASE-T1. This carrier extension may cause problems with full-duplex MACs that incorrectly handle the carrier extension symbols. When register 4.8010.13 is set to 1, all carrier extend and carrier extend with error symbols received by the SGMII will be converted to idle symbols when operating in full duplex. Carrier extend and carrier extend with error symbols will not be blocked when operating in half duplex or if register 4.8010.13 is set to 0. Symbol errors will continue to be propagated regardless of the setting of register 4.8010.13.

2.2.3 Tx Disable Feature

The device supports a Tx Disable feature (TX_ENABLE pin). If the pin input is LOW, then Tx packets will be stopped after link up, but Rx packets are still received normally. The link will stay up and only idles will be sent out the Tx media side. There is an internal pull-up, which will disable this feature if the pin is left floating. A HIGH value from the pull-up or if driven externally will allow packets to flow by default.

To disable this feature completely and use this pin for LED or GPIO functions, write register 3.8000.3 = 0. This will change the pin to an output and the link status will light up the LED without additional programming. For the register description, see Table 105, Reset and Control Register, on page 143.

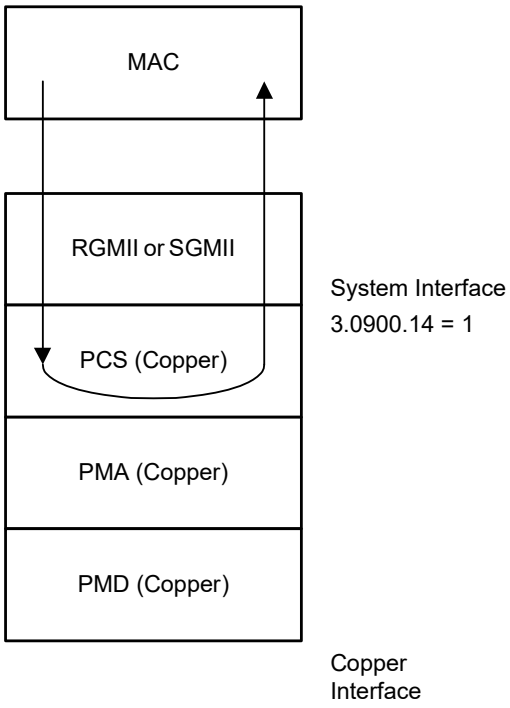
2.3 Loopback

The device implements various different loopback paths.

2.3.1 System Interface Loopback

The functionality, timing, and signal integrity of the system interface can be tested by placing the device in system interface loopback mode. This can be accomplished by setting register 3.0900.14 = 1.

Figure 14: MAC Interface Loopback Diagram — Copper Media Interface

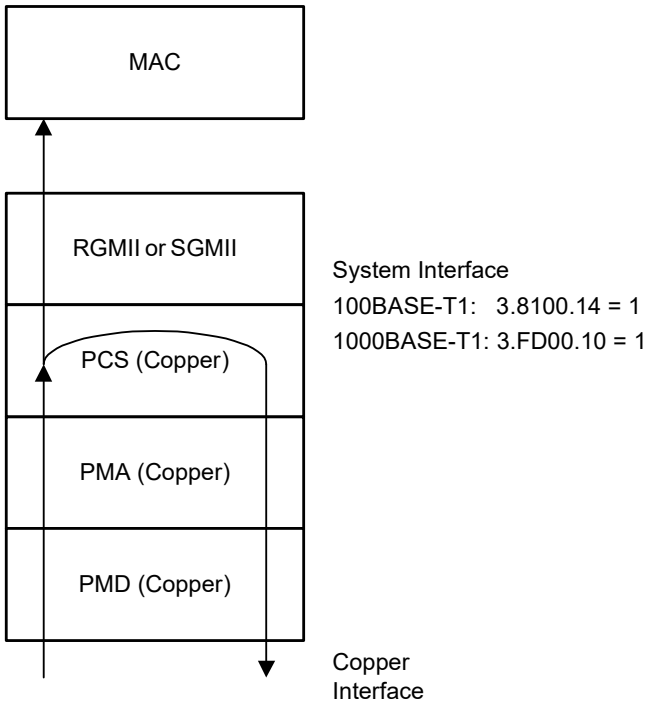


2.3.2 Line Loopback

Line loopback allows a link partner to send frames into the device to test the transmit and receive data path. Frames from a link partner received by the PHY, before reaching the MAC interface pins, are looped back and sent out on the line. They are also sent to the MAC. The packets received from the MAC are ignored during line loopback. This allows the link partner to receive its own frames.

Prior to enabling the line loopback feature, the PHY must first establish a link to another PHY link partner. When the link is established, the line loopback mode can be enabled by setting register 3.FD00.10 = 1. In 100BASE-T1 mode, it is register 3.8100.14 = 1.

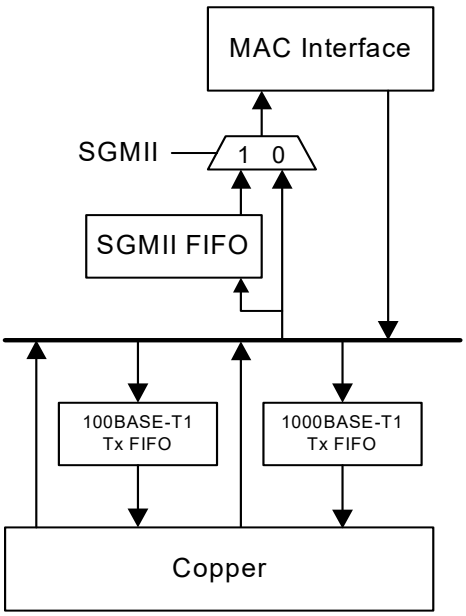
Figure 15: Copper Line Loopback Data Path



2.4 Synchronizing FIFO

The FIFO depths can be increased in length to support longer frames. The device can handle jumbo frame sizes up to 25 KB with up to ±100 ppm clock jitter for SGMII. The deeper the FIFO depth is, the higher the latency will be.

Figure 16: FIFO Locations



The SGMII FIFO status bits can generate interrupt on the register bit 4.8013.7 with an enable bit in register 4.8012.7. The 1000BASE-T1 FIFO status for either underflow or overflow are reported in register 3.0008.11.

2.5 Resets

In addition to the hardware reset pin (RESETn), there are several software reset bits as summarized in Table 48.

The copper circuit is reset via any of the registers 1.0900.15, 3.0900.15, or 7.0200.15. The SGMII circuit is reset via register 4.8000.15. The RGMII circuit is reset via register 3.8000.15. The reset in one circuit does not directly affect another circuit.

All reset registers except RGMII are self-clear.

Table 48: Reset Control Bits

Reset Register	Register Effect	Functional Block
1.0900.15	Software Reset for Registers in Device 1	Copper
3.0900.15	Software Reset for Registers in Device 3	Copper
3.8000.15	Software Reset for Registers in Device 3	RGMII
7.0200.15	Software Reset for Registers in Device 7	Copper
4.8000.15	Software Reset for Registers in Device 4	SGMII

2.6 Power Management

The device supports several advanced power management modes that conserve power, with the following three low power modes

- IEEE Power Down mode
- Passive mode
- OPEN Alliance TC10 Sleep mode

2.6.1 IEEE Power Down Mode

The standard IEEE Power Down mode is entered by setting register 1.0900.11 or 3.0000.11. In this mode, the PHY does not respond to any system interface (that is, RGMII/SGMII) signals except the MDC/MDIO. It also does not respond to any activity on the copper media.

In this Power Down mode, the PHY cannot wake up on its own by detecting activity on the media. It can only wake up by setting registers 1.0900.11 and 3.0000.11 = 0.

The automatic PHY power management can be overridden by setting the power down control bits. These bits have priority over the PHY power management in that the circuit can not be powered up by the power management when its associated power down bit is set to 1. When a circuit is power back up by setting the bit to 0, a software reset is also automatically sent to the corresponding circuit.

Table 49: Power Down Control Bits

Power Down Register	Register Effect
1.0900.11	Copper Power Down
3.0000.11	Copper Power Down

2.6.2 Passive Mode

During power reset, if RXC/CONFIG[4] pin is set to Low and TC10 is enabled, then the device will start in Passive mode.

In Passive mode, the device remains in a halt state refraining from proceeding to link training. One of the differences between IEEE Power Down mode and Passive mode is that in the Passive mode, the transmitter is enabled while in IEEE Power Down mode, the transmitter is disabled. Another difference is that in this halt state device will respond to following TC10 transactions.

- The device will be able to receive wake request and transmit WUP and it should be able to detect WUP and forward to other devices in the network through WAKE_OUT pin.
- In Passive mode, when a TC10 transaction is completed device will not proceed to link training, it will remain in a halt state with the ability to respond to TC10 transactions.

To switch to IEEE power down mode from Passive mode, when register write becomes available, write register to enter IEEE mode and write register to disable Passive mode.

There are two options to exit Passive mode: either set 3.8022[5]=0 (1000BT1 mode)/3.8702[5]=0 (100BT1 mode) or enable Passive mode exit (3.8022[3]/3.8702[3]) upon any wake event.

2.6.3 OPEN Alliance Sleep Mode

For additional information, refer to Section 2.7, OPEN Alliance TC10 Sleep Mode.

2.7 OPEN Alliance TC10 Sleep Mode

The BRIGHTLANE™ 88Q2220/88Q2220M/88Q2221/88Q2221M device can operate in a low power sleep mode with minimal standby current from the battery voltage with the main supply shut off. During this mode, the device can continuously monitor for a pulse presented at the local wake-up pin, and respond to this wake-up pulse command as specified in OPEN Alliance Sleep/Wake Specification.

2.7.1 TC10 Sleep/Wake Configurations

- **Stand-alone TC10-capable PHY to Stand-alone TC10-capable PHY**
  The Sleep/Wake between two TC10-capable stand-alone PHYs, such as the BRIGHTLANE™ 88Q2220/88Q2220M/88Q2221/88Q2221M device, are accomplished through MDI. Either of the devices can initiate a sleep request via register write.

Figure 17: BRIGHTLANE™ 88Q222x[M] TC10 Sleep/Wake

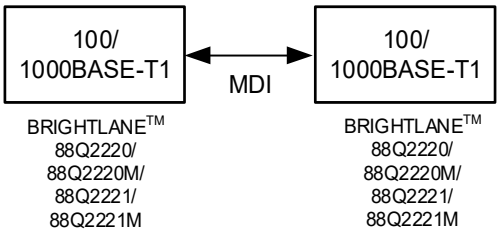
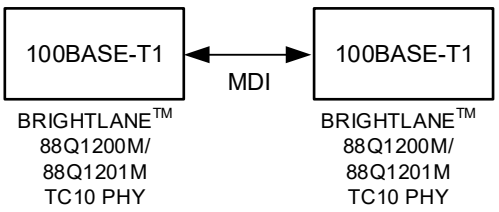
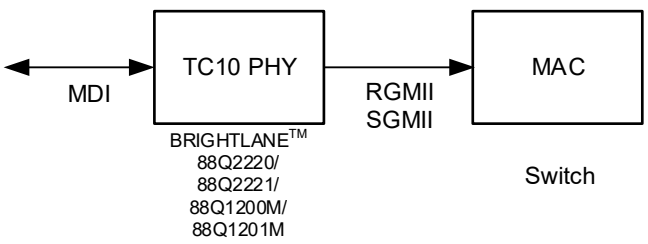


Figure 18: BRIGHTLANE™ 88Q120xM TC10 Sleep/Wake



- External TC10-capable PHY with TC10-capable MAC (Switch)
  For extended applications of PHYs connected with a Infineon automotive switch, the switch level awareness of the Sleep/Wake events are required so that the switch can determine if the switch is ready to allow itself to enter sleep. The in-band communication from PHY to MAC (for example, switch) to convey-sleep state is available to achieve this notification.

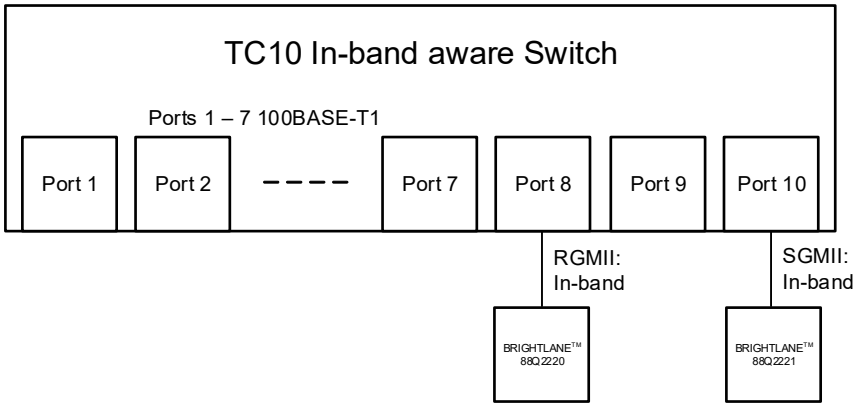
Figure 19: In-band TC10 Relay to MAC (Switch) Interface



- **Multiple TC10-capable PHYs Integrated/External in a Switch Application**
  In the case of a switch application, although a port and its link partner may agree to enter TC10 deep sleep state (where power to the device is totally removed), the switch and remaining PHY ports may not be ready to enter the deep sleep state. So, the PHY port will enter a low power state similar to IEEE power down while the remaining switch and others stay active.

  When all ports have agreed to enter the TC10 Deep Sleep state with their link partner, the switch can then decide to enter the Deep Sleep state taking away power to the switch.

Figure 20: MAC (Switch) Interface In-band TC10 Relay



2.7.2 Sleep and Wake-up

As an IEEE and OPEN Alliance TC10-compliant Ethernet PHY, the device supports wake-up and sleep signaling over dedicated I/O pins, as well as through Wake-up Pulse (WUP), Wake-up Request (WUR) and Low Power Sleep (LPS) commands.

2.7.2.1 Wake-up

The device can be woken up by a local wake-up pin, a wake-up request command or a from a link partner. Upon detection, a wake-up interrupt may be generated, and the wake-up source is flagged in the Wake-up Status Register. The source bits are cleared when device is in reset mode.

2.7.2.1.1 Local Wake-up

When the device is in low power mode, a positive pulse presented at the WAKE_IN pin meeting the minimum duration time ($t_{localwkup}$) triggers a local wake-up.

2.7.2.1.2 Remote Wake-up Indication During Link-up by Wake-Up Request (WUR)

In 100BT mode, a WUR command is encoded in the scrambler stream, when a wake request is received after link up, so the device is not in a low power mode. A minimum of 64 bits of WUR-encoded idles are required for a successful detection and passing of the wake request to the other parts of the network. In 1000BT1 mode, a WUR command is encoded in D5 of symbol 0 of OAM frame. A WUR command is transmitted by a single OAM frame with the respective bit set.

2.7.2.2 Enter Sleep Modes

There are two low power or sleep modes.

- The traditional LPSD mode, known as the Deep Sleep Mode, where the device has supply power completely removed.
- The T1 Port Sleep Mode where the device still has power, but in a low power state (similar to IEEE power down).

The following are methods to request that the PHY device power down in the T1 Port Sleep Mode:

1. The link partner sends a low power sleep command (LPS). In 100BT1, this is a specific scrambled idle included within the normal idles. In 1000BT1, an LPS message is sent through specified OAM bit. This initiates a sleep handshake with it to confirm both must be in the T1 Port Sleep Mode low power state. A register bit (3.8702.0 for 100BT1 and 3.8022.0 for 1000BT1) is programmed to 1 to initiate a sleep request, which will initiate a sleep handshake with the link partner.
2. A sleep request is received at the host interface from the switch, which initiates the sleep handshake with the link partner. This can be the result of a sleep request being forwarded from one port to the another port.
3. Write register bit 3.8020.0 to 1 to enable an LPSD power down. Changing 3.8020.0 to 1 puts the device into TC10 sleep mode without performing a TC10 sleep handshake with the link partner.

Note

To put the DUT in LPSD Power Down mode, the LP should either be disconnected or the LP should be in a mode where it is not transmitting.

To request a Deep Sleep Entry, use any of the previously described T1 Port Sleep Mode methods that best suits the use case. After entering T1 Power Sleep Mode, write a ‘1’ to 4.FD21.4 to enter Deep Sleep Mode.

A sleep handshake may be aborted if register 3.8702.4 for 100BT1 and 3.8022.4 for 1000BT1is set. If a sleep request is received when the PHY and its copper link partner have link up, then the PHY will send an LPS to the link partner and try to initiate a sleep handshake. If the link is not up and the PHY is not in a low power state, then the PHY will wait for link to be up prior to sending the sleep request (LPS). The wait time is 195 ms by default. After this time, the sleep request in dropped.

2.7.2.2.1 Low Power Sleep

In 100BT mode, an LPS is encoded in the scrambler stream, 64 bits of LPS-encoded idles must be sent for a sleep request to be successfully detected by the link partner. In 1000BT1 mode, an LPS command is encoded in D4 of symbol 0 of OAM frame. An LPS command is transmitted by a single OAM frame with the respective bit set.

2.7.2.3 Sleep/Wake Forward Through Host Interface By Command Idle Codegroup (CIC)

The Open Alliance (OA) specification defines how Sleep/Wake commands are communicated through the T1 Physical layer. However, how the commands forward through multiple port or host interfaces is not in the OA spec's scope. In the case where this device is connected to a Infineon switch as an external T1 PHY through the host interface, Infineon has a proprietary method to embed the sleep/wake commands and status in the RGMII or SGMII Idles. The in-band message conveyed in one idle group is known as a command idle codegroup (CIC). Note that MII and RMII do not support this. The in-band messaging can be sent through the RGMII/SGMII interface only. An

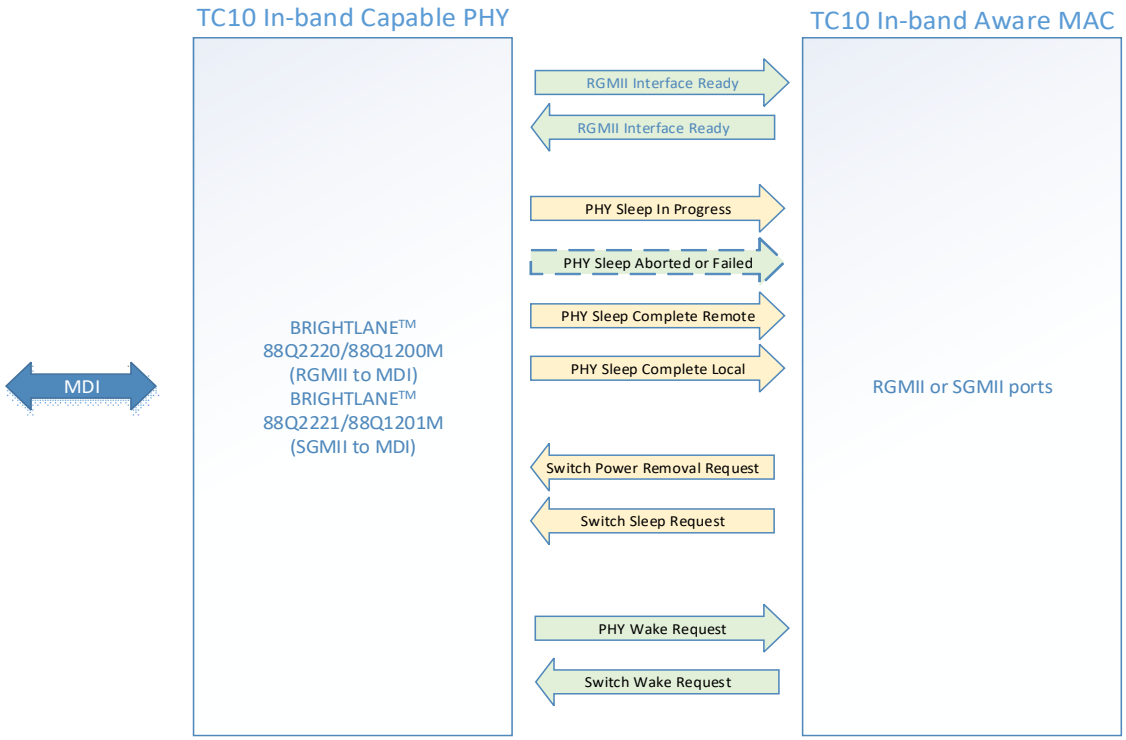
example of the usage of CICs involves one of the switch's T1 port receiving a WUP from its remote link partner to trigger a wake-up of the T1 port. This wake command can be forwarded inside the switch, according to the Wake Forwarding Vector, to an RGMII/SGMII host port that connects to an external T1 PHY such as this device. The external PHY can then also wake up from T1 Port Sleep mode, send a WUP, and wake up its link partner as well.

The following CICs are defined for each host interface:

1. RGMII- two 4-bit nibbles presented at each clock edge that are paired together to form a byte.
2. SGMII- one KD idle codegroup if the disparity following these is negative and two KD idle codegroups if the disparity following the first is positive.

The CIC feature can be enabled or disabled per RGMII or SGMII ports.

Figure 21: In-band Communication Transaction



2.7.2.3.1 Messages in CIC

CICs can be used in two-way forwarding of sleep or wake commands, as well as traffic control during a PHY LPS handshake. Table 50 lists all commands and functions of the CICs.

Table 50: CIC Commands and Functions

Commands	Direction	Function
Switch Wake Request	Switch to an external PHY	Forwards a Wake Request from the switch to an external PHY. The external PHY should wake up and send a WUP/WUR to the T1 Link Partner.
PHY Wake Request	External PHY to the switch	After an external PHY receives WUP/WUR from the Link Partner, the wake commands are passed to the switch by this CIC. A Wake Command is further forwarded to applicable ports in the switch according to the Wake Forwarding Vector.
Switch Sleep Request	Switch to an external PHY	Forwards a Sleep Request from the switch to an external PHY. The external PHY should initiate LPS handshake to the T1 Link Partner.
PHY Sleep In Progress	External PHY to the switch	PHY uses this CIC to notify the switch that a sleep handshake with the Link Partner is in progress, and that the switch should stop the traffic to the PHY and prepare for the PHY's sleep.
PHY Sleep Complete Remote	External PHY to the switch	PHY notifies the switch that the PHY has successfully completed a sleep handshake initiated by the Link Partner and the PHY is in a sleep state.
PHY Sleep Complete Local	External PHY to the switch	PHY notifies the switch that the PHY has successfully completed a sleep handshake initiated by the switch or PHY, and the PHY is in sleep state.
PHY Sleep Abort or Failed	External PHY to the switch	PHY notifies the switch that the PHY's sleep handshake with the Link Partner is aborted or failed, and the PHY is not in a sleep state.
Switch Power Removal Request	Switch to an external PHY	After the PHY is in the T1 port sleep state, the switch uses this CIC to ask the PHY to go to deep sleep (power will be removed).
RGMII Interface Ready	Both	To indicate RGMII interface is stable and ready to pass/receive CICs.

2.7.3 TC10 Sleep/Wake-up Enable

The TC10 Sleep/Wake-up feature for the device is enabled via the configuration pin. If the RCLK pin floats, then an internal pull-up will enable this feature. An external pull-down will disable the feature.

2.7.4 WAKE_OUT to WAKE_IN Pin or INH Pin

This device supports the WAKE_OUT feature/pin. This feature is disabled by default and can be enabled by programming register 3.802C.14:13 to 2'b10 (WAKE_IN pin as WAKE_OUT and WAKE_IN signals) or 2'b01 (INH pin as WAKE_OUT signal) and then programming register 3.8021.15 to 1 for the setting to take effect.

When register 3.802C.14:13 is programmed to 2'b10, the WAKE_IN pin functions as a bidirectional WAKE_IN and WAKE_OUT signals. When register 3.802C.14:13 is programmed to 2'b01, the INH pin functions as a WAKE_OUT signal. In this case, the INH pin cannot be used to control the power supply.

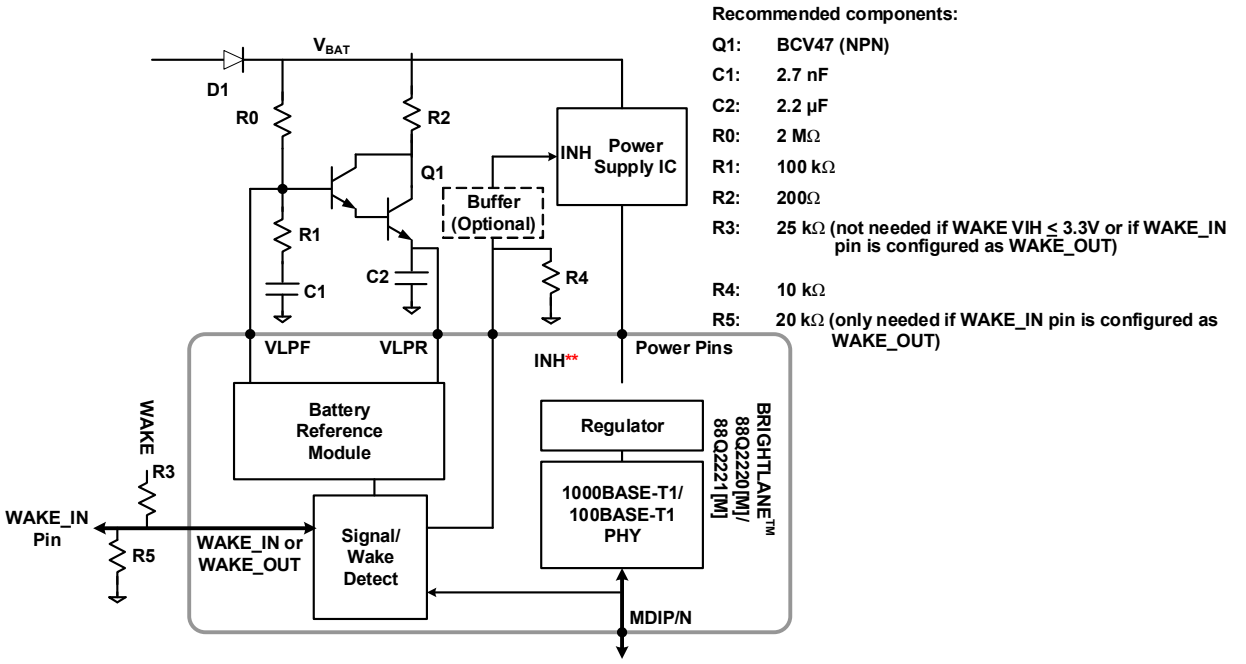
The wake out pulse width is defined in Register 3.8021.7:6.

2.7.5 Low Power Signal Detect (LPSD)

The device can operate in a low power sleep mode with minimal standby current from the battery voltage with the main supply shut off. During this mode, the device can continuously monitor the WAKE_IN pin, and respond to wake-up pulse command as specified in OPEN Alliance Sleep/Wake-up Specification. Figure 22 and Figure 23 shows the Low Power Signal Detect (LPSD) schematic.

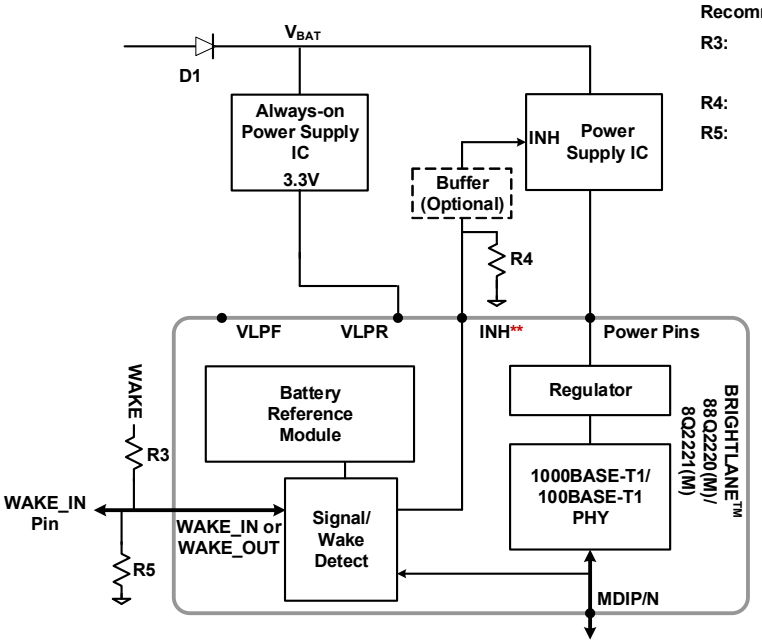
2.7.5.1 LPSD Option

Figure 22: LPSD Block Diagram — Option 1



** If INH is configured as WAKE_OUT then INH cannot be used to control the power supply.

Figure 23: LPSD Block Diagram — Option 2 (only Applicable in Rev. B2)



Recommended components:

R3: 25 k Ω (not needed if WAKE VIH ≤ 3.3V or if WAKE_IN pin is configured as WAKE_OUT)

R4: 10 k Ω

R5: 20 k Ω (only needed if WAKE_IN pin is configured as WAKE_OUT)

** If INH is configured as WAKE_OUT then INH cannot be used to control the power supply.

2.7.5.2 LPSD Electrical Characteristics

Table 51: LPSD Electrical Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{BAT}	Battery Voltage	–	6	12	28	V
$I_{STANDBY}$	Standby Current	Battery voltage = 12V	–	–	35[1]	µA
I_{INH}	INH Pin Source Current	V_{INH} = 1.9V with 10K Pull-Down	–	–	0.23[2]	mA
$I_{WAKEOUT}$	WAKE_OUT Pin Source Current	V_{INH} = 1.9V with 10K Pull-Down	–	–	0.23[2]	mA
V_{INH}	INH Pin Output High Voltage	Pull-down 10 kΩ Additional load: 40 µA	1.5	–	3.465[2]	V
V_{LPR}	VLPR Pin Input voltage[3]	Externally supplied	2.7	3.3	3.465[2]	V
VIH_WAKE_IN	WAKE_IN pin Input High Voltage	–	1.87	–	3.465[2]	V
VIL_WAKE_IN	WAKE_IN pin Input Low Voltage	–	–	–	0.5	V

Table 51: LPSD Electrical Characteristics (Continued)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
VIH_WAKE_OUT	WAKE_OUT pin Output High Voltage	Pull-down 10 kΩ Additional load: 40 µA	1.9	–	–	V
		Pull-down: 100 kΩ Driving BRIGHTLANE™ devices. See Note 1.	1.9	–	–	V
$T_{MDI,LAT}$	Latency from MDI Signals to INH Assertion	Normal link	–	–	20	µs
$T_{WAKE,PW}$	WAKE_IN Pin Pulse Width to Wake-up LPSD	–	40[4]	–	–	µs
$T_{WAKEOUT,PW}$	WAKE_IN is configured as WAKE_OUT[4]	–	42[4]	–	160	µs

1. For battery voltage ~24V & temperature > 70°C, max standby current may go up to 45 µA. Default value.

2. 10 kΩ typ load current is 190 µA, Additional available load is 40 µA.
   - INH, WAKE_IN and WAKE_OUT pins can tolerate max of 3.465V.

3. For LPSD closed loop connection, employ Option 1[Section 2.7.5.1] of the Darlington pair circuit recommended by Infineon.

4. TWAKE,PW and TWAKEOUT,PW values are based on default register settings defined in register 3.8021.

Note 1: Driving one or two WAKE_IN pins of BRIGHTLANE™ devices and pull-down resistor. The device can support a bi-directional WAKE_IN_OUT pin; internally, the chip connects WAKE_OUT and WAKE_IN to a single pin. In this scenario, WAKE_OUT is already driving one WAKE_IN.

2.7.5.3 LPSD Application Notes

- WAKE bus voltage

  a) If WAKE bus is running on 3.3V supply, then WAKE bus direct hooks up to WAKE_IN pin is OK.

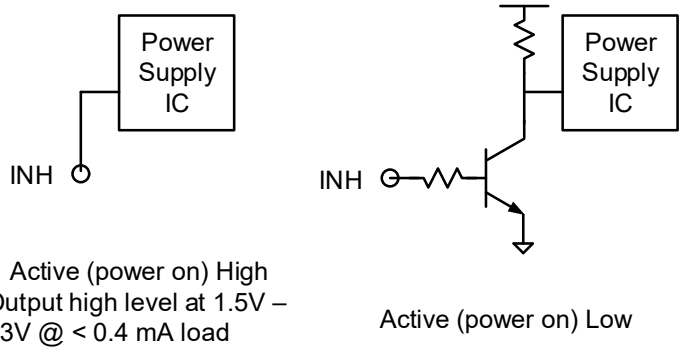
  b) If WAKE bus is running on battery supply, then an external series 25 kΩ resistor is required to drive WAKE_IN pin.

- INH output

  The power supply IC EN/INH pin can be driven by the INH pin in typical cases. For example configurations, see Figure 24.

  If the on-chip regulator not used, then the INH output must control the EN input of all power supply ICs that power the device.

Figure 24: INH Output Example Configurations



- Wake-up application scenarios – four cases of wake-up schemes can be supported:
  - Case 1: Local wake-up and remote wake-up.
    WAKE_IN from host controller. 3.3V or VBAT level can be accepted.
    For VLPR, VLPF, and INH, see Figure 22 or Figure 23.
  - Case 2: No local wake-up. Remote wake-up support.
    WAKE_IN = VSS. For VLPR, VLPF, and INH, see Figure 22 or Figure 23.
    Or use case 1 configuration, but use registers to program.
  - Case 3: Local wake-up only. No remote wake-up.
    Use case 1 configuration. Use register programming to disable remote wake-up.
  - Case 4: No local wake-up. No remote wake-up.
    (WAKE_IN = VSS or NC. VLPF and INH = NC. VLPR = 2.7~3.6V)

2.8 Status of Functional Blocks in Each Device Mode

Table 52: Status of Functional Block in Each Mode

Functional Block Pin(s)	Reset	Operation (normal)	T1 Port Sleep	OPEN Alliance Sleep	IEEE Copper Low Down	IEEE SGMII Low Down
RGMII	Reset[1]	On	On[2]	Off	On[2]	On
SGMII	Reset	On	On[2]	Off	On[2]	Low Power
Refclk	Reset[3]	On	On	Off	On	On
Regulator	On	On	On	Off	On	On
RESETn	Functional	Functional	Functional	Disable	Functional	Functional
MDC/MDIO	Disable	Functional	Functional	Disable	Functional	Functional
TX_DISABLE	Disable	Functional	Functional	Disable	Functional	Functional
WAKE_IN	Disable	Functional	Functional	Functional	Disable	Functional
INH	Functional	Functional	Functional	De-asserted	Functional	Functional

Table 52: Status of Functional Block in Each Mode (Continued)

Functional Block Pin(s)	Reset	Operation (normal)	T1 Port Sleep	OPEN Alliance Sleep	IEEE Copper Low Down	IEEE SGMII Low Down
LPSD WUP Detect	Disable	Functional	Functional	Functional	Functional	Functional
INTn	De-asserted	Functional	Functional	Off - floating	Functional	Functional

1. RGMII output must be tri-state during reset.
2. SGMII/RGMII in T1 port sleep or IEEE Copper Low Power, it will be put in Low Power mode if CIC is not enabled and will be kept on if CIC is enabled.
3. Refclk is reset, supll is reset, external crystal is active, but internal crystal output is not active with no supply.

2.9 Auto-Negotiation

The optional Auto-Negotiation is based on Clause 98 of the IEEE 802.3 specification. It is used to negotiate speed and master/slave.

Auto-Negotiation is disabled by default, it can be enabled via register 7.0200.12. When Auto-Negotiation is enabled, the abilities that are advertised can be changed via registers 7.0202 to 7.0204. Changes to these registers do not take effect unless one of the following occurs:

- There is a software reset (1.0900.15, 3.0000.15, or 7.0200.15).
- A Restart Auto-Negotiation is asserted (7.0200.9).
- There is a transition from power down to power up (1.0900.11 or 3.0000.11).
- The Auto-Negotiation Enable bit toggles (7.0200.12).
- The copper link goes down.

Registers 7.0202 to 7.0204 are internally latched once every time the Auto-Negotiation enters the Ability Detect state in the arbitration state machine. So, a write to registers 7.0202 to 7.0204 has no effect when the PHY begins to transmit differential Manchester encoding (DME) pages. This guarantees that sequences of DME pages transmitted are consistent with one another.

If additional next pages are not required, then the next page bit (7.0202.15) can be set to 0 (default) and no further action is required by the user. When a link partner indicates a next page will be sent, where 7.020B.15 = 1, a null next page (IEEE 802.3 Annex 98C) is automatically generated and sent back to the link partner. If next pages are required, then the user can set register 7.0202.15 to 1. Additional next pages can be transmitted and received via registers 7.0208 to 7.020A and 7.021B to 7.021D, respectively.

When the PHY completes Auto-Negotiation, it updates the various status in registers 7.0201 and 7.0205 to 7.0207.

2.10 Advanced Virtual Cable Tester

The device’s Advanced VCT feature uses time domain reflectometry (TDR) to determine the quality of the cables, shorts, cable impedance mismatch, bad connectors, and termination mismatch. The device transmits a signal of known amplitude (+1V) down the single pair of an attached cable. It will conduct the cable diagnostic test on MDIP/MDIN. The transmitted signal will continue down the cable until it reflects off of a cable imperfection.

2.10.1 VCT Configuration

The VCT test is configured by setting the following register bits:

- Register 3.FEDE = 0x0058 (Offset cutoff point)
- Register 3.FEDA = 0x00EB (Offset value for long cable)
- Register 3.FED9 = 0x010e (Offset value for short cable)

- VCT Start:
  - Register 3.FECA bit 12 to 0 (Remove Reset from VCT Block)
  - Register 3.FEDD bit 1 to 1 (Start test)
- Reading Results:
  - Read Register 3.FEDD[1:0]
    - 2'b10: VCT Active
    - 2'b01: VCT DONE
  - Read Register 3.FEDD[7:4]
    - 0011: Short
    - 1110: Harness Open
    - 0111: Cable OK
    - 1000: Test in progress
    - 0101: Noise
  - Read Register 3.FEDD[13:8] Distance in meters

The VCT test is initiated by setting register 3.FEDD bit 1 to 1. Register 3.FEDD bit 0 will be set to 1 indicating that the is done and the results are available. Each time the VCT test is enabled the results seen on the single channel are reported in register 3.FEDD bit [7:4] and [13:8] as defined in register definition.

2.10.2 Pulse Amplitude and Pulse Width

The transmitted pulse amplitude and pulse width can be adjusted via register 3.FEC3 bits 11 to 7 and register 3.FEC3 bits 1 to 0, respectively. These bits must be set to full amplitude and full pulse width.

2.11 Packet Generator and Packet Checker

2.11.1 CRC Error Counter and Frame Counter

The cyclic redundancy check (CRC) counter and packet counters that are normally found in MACs are available in the device. The error counter and packet counter features are enabled through register writes, and each counter is stored in eight register bits.

To enable the packet counter in two different write commands, first enable the counter 3.FD07.0 and then start the count sequence via 3.FD07.2.

To read the CRC counter and packet counter, read register 3.FD08:

- 3.FD08.7:0 (Frame count is stored in these bits)
- 3.FD08.15:8 (CRC error count is stored in these bits)

The CRC counter and packet counter do not clear on a read command. To clear the counters, write register 3.FD07. 3 = 1 (this bit is a self-clear bit). Disabling the counters by writing register 3.FD07.2 = 0 will also reset the counters. In addition to having a CRC checker and packet counter, the BRIGHTLANE™ 88Q2220/88Q2220M/88Q2221/88Q2221M features CRC preemption packet checking.

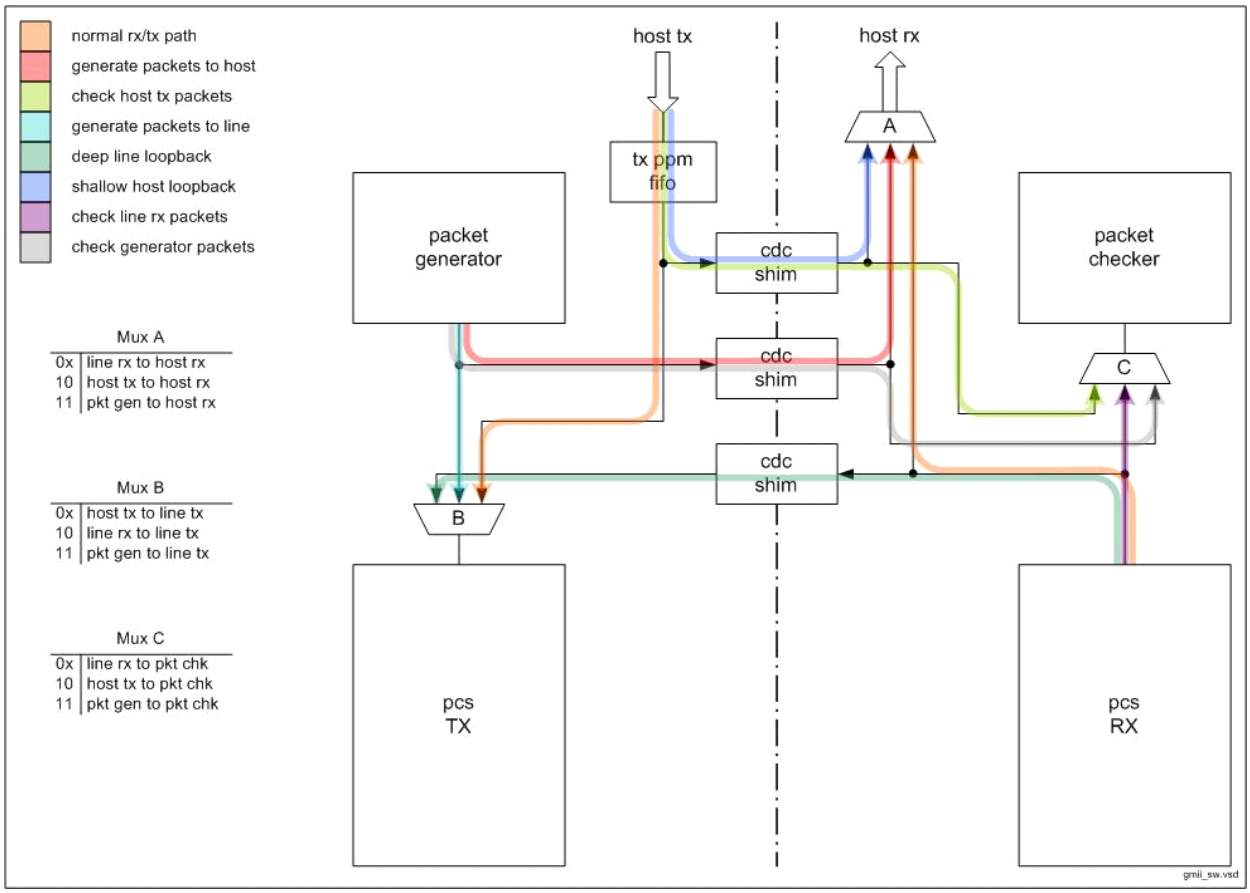
2.11.2 GMII Data Steering

The copper unit in the device includes a data steering module that allows packet generator and checker to be connected to multiple sources or destinations. The same module is also used to perform data loopback operation.

There are three sources for line data output: host GMII input, internal packet generation, and line data input also known as deep line loopback. Similarly, there are three sources for host GMII output: line data input, internal packet generation, and host GMII input also known as shallow host loopback. In addition, there is an internal packet checker as described in Section 2.11.1, which has three sources: host GMII input, internal packet generation, and line data input. Each of these selections can be independently controlled. The controls of these multiplexers must be set up for packet generator and checker before enabling the blocks. The register controls are located in 3.FD00.12:6.

A MAC loopback path must be implemented, where the output of the FIFO is looped back to the GMII Rx. Register 3.0900.14 will overwrite the multiplexer that controls this loopback path.

Figure 25: Data Steering around GMII Interface



2.11.3 Packet Generator

The device contains a very simple packet generator. Write to register 3.FD04.3 to enable the packet generator.

When enabled, fixed length packets of 64 or 1518 bytes (including CRC) will be transmitted, separated by 12 bytes of inter-packet gap (IPG).The preamble length will be 8 bytes. The payload of the packet is either a fixed 5A, A5, 5A, A5, or pseudo-random pattern. A correct IEEE CRC is appended to the end of the packet. An error packet can also be generated.

The registers are as follows:

- 3.FD04.2 Payload Type
  - 0 = Pseudo-random
  - 1 = Fixed 5A, A5, 5A, A5, and so on
- 3.FD04.1 Packet Length
  - 0 = 64 bytes
  - 1 = 1518 bytes
- 3.FD04.0 Error Packet
  - 0 = Good CRC
  - 1 = Symbol error and corrupt CRC
- 3.FD04.15:8 Packet Burst Size
  - 0x00 = Continuous
  - 0x01 to 0xFF = Burst 1 to 255 packets

2.12 Automatic Polarity Detection and Correction

For 1000BASE-T1, the device automatically corrects polarity errors on the receive pairs. On the receive side, receive polarity inversion are automatically corrected based on the sequence of idle symbols. When the descrambler is locked, the symbol lock is found and the polarity is also locked based on the incoming data. The polarity becomes unlocked only when the receiver loses lock. If 1000BASE-T1 link is established, then register 1.0901.2 records the real-time status of the polarity.

1.0901.2 Polarity (real time)

- 1 = Reversed
- 0 = Normal

For 100BASE-T1, the device, when configured as SLAVE, has the capability to automatically detect the polarity on the receive side when a polarity swap is observed. In addition to this, when a polarity flip is observed, it will also invert the polarity on its transmit side if this is enabled.

If 100BASE-T1 link is established, then register 3.8109.1 records the real-time status of the polarity.

3.8109.1 Polarity (real time)

- 1 = Reversed
- 0 = Normal

This bit is only valid when 3.8100.9 is 1.

Polarity correction feature is disabled by default and can be enabled by programming register 3.8100.9 to 1.

2.13 DME Pages Exchange Complete with No Link

Auto-Negotiation uses the DME scheme. Sometimes when the link does not come up, it is difficult to determine whether the failure is due to incomplete DME exchanges or the 1000BASE-T1/100BASE-T1 link is unable to come up.

Register 7.8001.15 is a sticky bit that gets set to 1 whenever the Auto-Negotiation exchange is completed, but master/slave does not resolve or a link cannot be established. When the bit is set, it can be cleared only by reading the register.

This bit will not be set if the DME pages exchange is not completed or if link is established.

2.14 GPIO

The GPIO and TX_ENABLE pins can be used for GPIO functionality. Registers 3.8010 to 3.8015 control the operation of the GPIO/TX_ENABLE pins. Registers 3.8013.3 and 3.8014.3 are used to program the TX_ENABLE pin for GPIO functionality. To use the TX_ENABLE pin for a GPIO function, 3.8013.3 must be 0, while 3.8014.3 must be written to 1. Register bits 3.8013.0 and 3.8013.1 control the direction of these pins. When they are programmed to 0, these pins are used as input pins. Otherwise, these are used as output pins.

When the GPIO/TX_ENABLE pins are in input mode, the register bits 3.8012.1:0 can be used to read the state of these pins. 3.8012.1 indicates the state of the TX_ENABLE pin and 3.8012.0 indicates the state of the GPIO pin. In input mode, an interrupt can also be generated depending on the value of the GPIO/TX_ENABLE pins. Registers 3.8014.10:8 and 3.8014.2:0 can be used to select when an interrupt must be generated. The interrupt status is stored in register 3.8011.1:0.

When the GPIO/TX_ENABLE pins are configured in output mode, register bits 3.8012.1:0 are used to drive the state of these pins. The value written to the 3.8012.1 register bit will be driven on the TX_ENABLE pin and the value written to the 3.8012.0 register bit will be driven on the GPIO pin. By default, the GPIO pin is programmed to be used for LED functionality.

2.15 LED

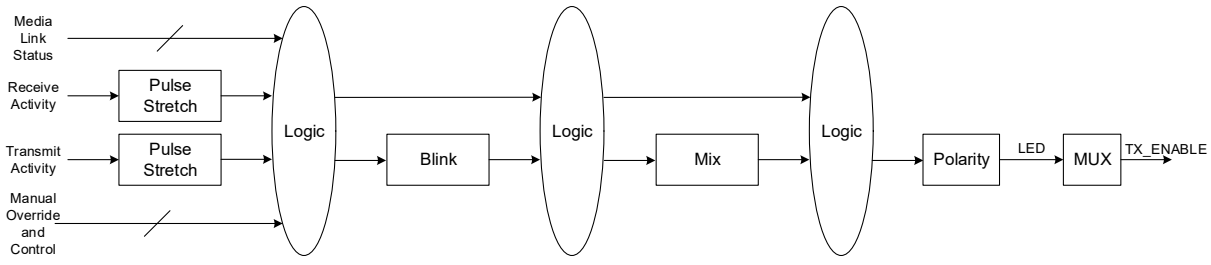
The TX_ENABLE and GPIO pins can be used to drive LED functionality. Registers 3.8013 to 3.8018 control the operation of the LEDs and by default, the GPIO pin is programmed for LED functionality. Registers 3.8014.7 and 3.8014.3 are used to configure internal bus LED [1:0] as shown in the diagram with the LED function and register bit 3.8013.3 is used to select which of the two LED signals of LED [1:0] are to be multiplexed onto the single TX_ENABLE pin. This arrangement of the LED will invalidate certain LED modes.

In general, 3.8016.7:4 controls the LED functionality for the GPIO pin and 3.8016.3:0 controls the LED functionality for the TX_ENABLE pin. These are referred to as single LED modes.

However, there are some LED modes where the GPIO and TX_ENABLE pins operate as a unit. These are entered when 3.8016.3:2 is set to 11. These are referred to as dual LED modes. In dual LED modes, register 3.8016.7:4 has no meaning when 3.8016.3:2 are set to 11.

Figure 26 shows the general chaining of function for the LEDs. The various functions are described in the following sections.

Figure 26: LED Chain

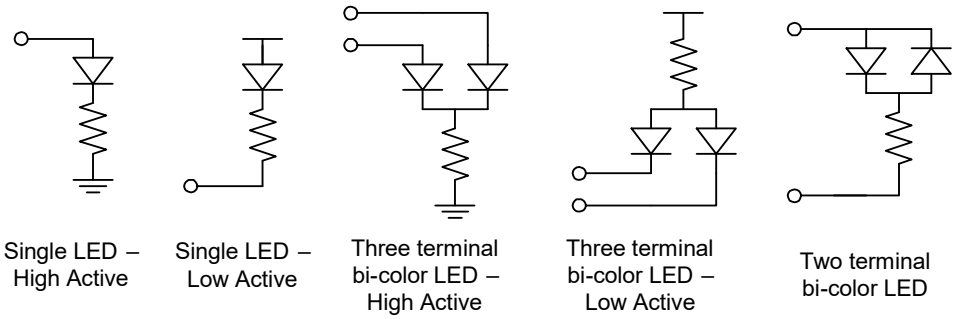


2.15.1 LED Polarity

There are a variety of ways to hook up the LED. Some examples are shown in Figure 27. For optimal design flexibility, register 3.8017.1:0 specifies the output polarity for the LEDs. The lower bit of each pair specifies the On (active) state of the LED, either high or low. The upper bit of each pair specifies whether the Off (inactive) state of the LED must be driven to the opposite level of the On state or Hi-Z.

For the register description, see Table 261, LED [1:0] Polarity Control Register, on page 211.

Figure 27: Various LED Hookup Configurations



2.15.2 Pulse Stretching and Blinking

Register 3.8018.14:12 specifies the pulse stretching duration of a particular activity. Only the transmit activity, receive activity, and (transmit or receive) activity are stretched. All other statuses are not stretched since they are static in nature and no stretching is required.

Some status will require a blinking state instead of a solid On state. Register 3.8018.10:8 specifies the blink rate. The pulse stretching is applied first and the blinking will reflect the duration of the stretched pulse.

2.15.3 Modes of Operation

The TX_ENABLE pins relay some modes of the PHY so that these modes can be displayed by the LEDs. Most of the single LED modes are self-explanatory from the register map. The non-obvious modes are covered in this section.

For the description of the related registers, see Table 260, LED Function Control Register, on page 211 and Table 262, LED Timer Control Register, on page 212.

2.15.3.1 Compound LED Modes

Compound LED modes are defined in Table 53.

Table 53: Compound LED Status

Compound Mode	Description
Activity	Transmit Activity OR Receive Activity

2.15.3.2 Speed Blink

When 3.8016.3:0 is set to 0010, the TX_ENABLE pin assumes the following behavior.

The TX_ENABLE pin outputs the sequence shown in Table 54, depending on the status of the link. The sequence consists of eight segments. The sequence repeats over and over again indefinitely.

The odd numbered segment pulse duration is specified in register 3.8018.1:0. The even numbered pulse duration is specified in register 38018.3:2.

Table 54: Speed Blinking Sequence

Segment	1000 Mbps	No Link	Duration
1	On	Off	3.8018.1:0
2	Off	Off	3.8018.3:2
3	On	Off	3.8018.1:0
4	Off	Off	3.8018.3:2
5	Off	Off	3.8018.1:0
6	Off	Off	3.8018.3:2
7	Off	Off	3.8018.1:0
8	Off	Off	3.8018.3:2

Table 55: Speed Blink

Register	Pin	Definition
3.8018.3:2	Pulse Period for Even Segments	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms
3.8018.1:0	Pulse Period for Odd Segments	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms

2.15.3.3 Manual Override

When registers 3.8016.7:6 and 3.8016.3:2 are set to 10, the LEDs are manually forced. Registers 3.8016.5:4 and 3.8016.1:0 select whether the LEDs are on, off, Hi-Z, or blink.

2.16 Synchronous Ethernet (SyncE) Clock

The GPIO pin can output a 125 MHz SyncE clock that can be used to clock other digital logic. This clock must not be used as an input to devices that require a higher quality clock.

Register 3.8004.0 is used to enable/disable the SyncE clock output on the GPIO pin. When 3.8004.0 is 1, the GPIO pin is used to output the SyncE clock. When 3.8004.0 is 0, the GPIO pin is used for GPIO/LED functionality. The default value of 3.8004.0 is 0 on power on, reset, or hardware reset.

2.16.1 Hardware Reset State

When hardware reset is asserted, the SyncE clock will not output.

2.17 Interrupt

An interrupt function is brought out to the chip's INTn pin. Register 3.8018.11 selects the polarity of the interrupt signal when it is active, where 3.8018.11 = 1 means it is active low and 3.8018.11 = 0 means it is active high. Register 3.8013.11 = 1 disables the tri-state on the INTn pin allowing an interrupt to be routed to the pin.

The registers 3.8010 and 3.8011 are interrupt enabled and function for 1000BASE-T1 and other modes of operation. For a specific interrupt, refer to the following registers:

- Register 4.8012/4.8013: Interrupt enabled and function for specific SGMII media

Registers 3.8010 and 3.8011 also contain the Interrupt Enable and the Interrupt Status registers for the GPIO pins (GPIO/LED).

There are force bits, polarity bits and tri-state control for the INTn pin. See Table 56 and Table 57.

Table 56: Interrupt Enable Bits

Register	Function
3.8018.15	Force interrupt.
3.8018.11	Set polarity.
3.8013.11	0 = The tri-state is enabled (This is the default state where the interrupt pin configured as an input). 1 = The tri-state is disabled (This setting is only for A0 or later).
3.8013.9	1 = Output is driven LOW for active interrupt and tri-stated when inactive.
3.8013.8	1 = Output is driven HIGH for active interrupt and tri-stated when inactive.

Table 57: Control Bit Interrupts

Register/Combination	Function
3.8013.9=1 and 3.8018.11=1	Output is driven LOW for active interrupt and tri-stated when inactive.
3.8013.9=0, 3.8013.8=1, and 3.8018.11=0	Output is driven HIGH for active interrupt and tri-stated when inactive.
3.8013.9=0, 3.8013.8=0, and 3.8018.11=1	Output is driven LOW for active interrupt and HIGH for inactive.
3.8013.9=0, 3.8013.8=0, and 3.8018.11=0	Output is driven HIGH for active interrupt and LOW for inactive.

2.18 Manual Impedance Calibration

The output impedance of the MAC interface I/O buffers can be programmed to match the trace impedance. Reflections can be eliminated and transmission line impedance can be matched by adjusting the NMOS and PMOS driver output strengths.

For the description of the related register, see Table 294, RGMII_IO Control Register, on page 224.

2.18.1 Manual Settings to the Calibration Registers

To use manual calibration, write to the following registers:

Write to register 3.8019.7:6 = b'PP and register 3.8019.3:2 = b'NN to adjust the PMOS and NMOS fingers accordingly, where

- PP is the 2-bit value for the PMOS strength.
- NN is the 2-bit value for the NMOS strength.

PP or NN will depend on the PCB used. A value of 11 enables all the fingers for maximum drive strength and for minimum impedance. A value of 00 turns all fingers off for minimum drive strength and for maximum impedance. Figure 28 shows an example of a signal output that must be cleaned up. Through manual calibration, the reflections can be eliminated as shown in Figure 29.

Figure 28: Signal Reflections

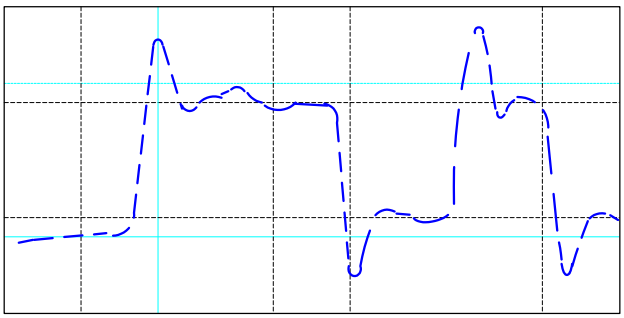
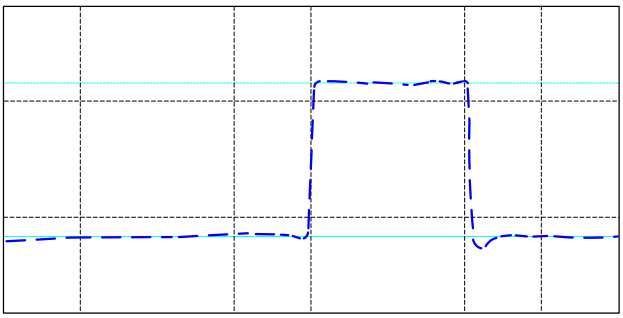


Figure 29: Clean Signal after Manual Calibration



2.19 Configuring the Device

The device can be configured in two ways:

- Hardware configuration strap options (unmanaged applications)
- MDC/MDIO register writes (managed applications)

The master/slave configuration settings can be overwritten by software. RGMII/SGMII mode settings can also be overwritten by software, but PHYAD configuration settings cannot be overwritten.

2.19.1 Hardware Configuration

The RXC, RXD [3:0], and GPIO pins are used as configuration pins. When RESETn is de-asserting, then the RXC, RXD[3:0], and GPIO pins are set as inputs and the internal pull ups are activated. If an external pull-down resistor is attached to the pin, then the input will be low; otherwise the input will be high. The RXC, RXD[3:0], and GPIO pins are sampled on the de-assertion of RESETn. After sampling is completed, the internal pull ups are disabled and the pins are set to outputs.

Table 58 shows how the sampled values are used.

Table 58: Sampled Values

Pin Name BRIGHTLANE™ 88Q2220/ 88Q2220M/ 88Q1200M	Pin Name BRIGHTLANE™ 88Q2221/ 88Q2221M/ 88Q1201M	BRIGHTLANE™ 88Q2220/88Q2220M/ 88Q1200M	BRIGHTLANE™ 88Q2221/88Q2221M/ 88Q1201M
		RGMII	SGMII
RXD[0]	CONFIG[0]	~PHYAD[0]	
RXD[1]	CONFIG[1]	~PHYAD[1]	
GPIO	GPIO	~PHYAD[2]	
RXD[2]	CONFIG[2]	0 = Master 1 = Slave	0 = Master 1 = Slave
RXD[3]	CONFIG[3]	0 = 100BT1 1 = 1000BT1	0 = 100BT1 1 = 1000BT1
RXC	CONFIG[4]	0 = Passive Mode Enable 1 = Passive Mode Disable	0 = Passive Mode Enable 1 = Passive Mode Disable
RCLK	CONFIG[5]	0 = Disable the TC10 Sleep/Wake-up feature 1 = Enable the TC10 Sleep/Wake-up feature	0 = Disable the TC10 Sleep/Wake-up feature 1 = Enable the TC10 Sleep/Wake-up feature

RGMII Delay TX and RX Clock, enabled by default.

Master/slave configuration can be overwritten by register bit 7.0202.12.

For BRIGHTLANE™ 88Q1200[M] and BRIGHTLANE™ 88Q1201[M], RXD[3]/CONFIG[3] must be strapped low, 0=100BASE-T1.

The RXC, RXD [3:0], and GPIO pins are used to configure PHYAD [0], PHYAD [1], and PHYAD [2], respectively. For a PHYAD of 0, these pins must be left floating. To configure a 1 on the PHYAD [0], PHYAD [1], and PHYAD [2] bits, the corresponding RXD/GPIO pins must have a pull-down resistor (4.7 kΩ) added to them externally. The mapping is shown in Table 59.

Table 59: {GPIO, RXD [1:0]} to PHYAD [2:0] Mapping for Configuration

GPIO Pin	RXD [1] Pin	RXD [0] Pin	PHYAD [2:0] Value
Unconnected	Unconnected	Unconnected	000
Unconnected	Unconnected	4.7 kΩ Pull-Down Resistor	001
Unconnected	4.7 kΩ Pull-Down Resistor	Unconnected	010

Table 59: {GPIO, RXD [1:0]} to PHYAD [2:0] Mapping for Configuration (Continued)

GPIO Pin	RXD [1] Pin	RXD [0] Pin	PHYAD [2:0] Value
Unconnected	4.7 kΩ Pull-Down Resistor	4.7 kΩ Pull-Down Resistor	011
4.7 kΩ Pull-Down Resistor	Unconnected	Unconnected	100
4.7 kΩ Pull-Down Resistor	Unconnected	4.7 kΩ Pull-Down Resistor	101
4.7 kΩ Pull-Down Resistor	4.7 kΩ Pull-Down Resistor	Unconnected	110
4.7 kΩ Pull-Down Resistor	4.7 kΩ Pull-Down Resistor	4.7 kΩ Pull-Down Resistor	111

2.19.2 Software Configuration — Management Interface

The management interface provides access to the internal registers via the MDC and MDIO pins and is compliant with IEEE 802.3u Clause 45 MDIO protocol. MDC is the management data clock input and it can run from DC to a maximum rate of 12.5 MHz. At high MDIO fanouts, the maximum rate may be decreased depending on the output loading. MDIO is the management data input/output and is a bidirectional signal that runs synchronously to MDC.

The MDIO pin requires a pull-up resistor in a range from 1.5 kΩ to 10 kΩ that pulls the MDIO high during the idle and turnaround phases of read and write operations.

Bits 1 and 0 of the PHY address are configured during the hardware reset sequence. PHY address bits [4:3] are set to 00 internally in the device. For detailed configuration information, see Section 2.19.

2.19.2.1 Clause 45 Register Access

Typical read and write operations on the management interface are shown in Figure 30 and Figure 31. All the required serial management registers are implemented as well as several optional registers. A description of the registers can be found in Section 3, General Registers, on page 133.

Figure 30: Typical MDC/MDIO Read Operation

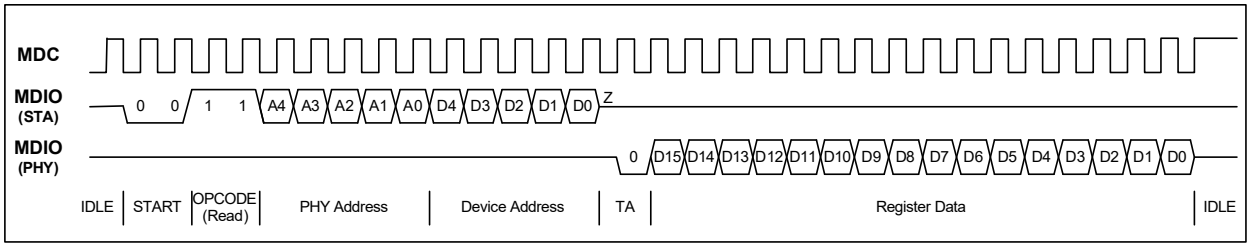
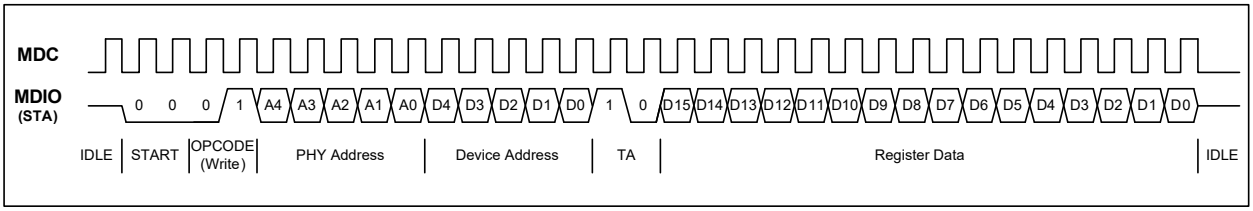


Figure 31: Typical MDC/MDIO Write Operation



The MDIO interface frame structure is compatible with the one defined in Clause 22 such that the two management interfaces can coexist on the same MDIO bus.

The extensions for Clause 45 MDIO indirect register accesses are specified in Table 60.

Table 60: Extensions for Management Frame Format for Indirect Access

Frame	PRE	ST	OP	PHYAD	DEVADR	TA	ADDRESS/DATA	Idle
Address	1...1	00	00	PPPPP	DDDDD	10	AAAAAAAAAAAAAAAA	Z
Write	1...1	00	01	PPPPP	DDDDD	10	DDDDDDDDDDDDDDDD	Z
Read	1...1	00	11	PPPPP	DDDDD	Z0	DDDDDDDDDDDDDDDD	Z
Read Increment	1...1	00	10	PPPPP	DDDDD	Z0	DDDDDDDDDDDDDDDD	Z

The MDIO implements a 16-bit address register that stores the address of the register to be accessed. For an address cycle, it contains the address of the register to be accessed on the next cycle. For read, write, post-read-increment-address cycles, the field contains the data for the register. At power up and reset, the contents of the register are undefined.

Write, read, and post-read-increment-address frames access the address register, though write and read frames do not modify the contents of the address register.

2.19.2.2 Clause 22 MDIO Register Access Method

The BRIGHTLANE™ 88Q2220/88Q2220M/88Q2221/88Q2221M supports Clause 22 MDIO manageable devices (MMD) extension registers to access Clause 45 MMD registers, using register 13 and 14 as specified in the IEEE Annex 22D.

Table 61: XMDIO MMD Control Register
Device 0, Register 13

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Function	R/W	0	0	11 = Data, post increments on writes only 10 = Data, post increment on reads and writes 01 = Data, no post increment 00 = Address
13:5	Reserved	RO	0	0	Reserved
4:0	DEVAD	R/W	0	0	Device Address

Table 62: XMDIO MMD Address Data Register
Device 0, Register 14

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Address Data	R/W	0	0	If 13.15:14 = 00, then MMD DEVAD's address register. Otherwise, MMD DEVAD's data register as indicated by the contents of its address register.

2.19.2.3 Preamble Suppression

The device is permanently programmed for preamble suppression. A minimum of one idle bit is required between operations.

2.20 Temperature Sensor

The device features an internal temperature sensor. The sensor reports the die temperature and is updated approximately once per second.

The temperature is obtained by reading the value in register 3.8043.7:0 and performing conversion functions as described in Table 63.

Table 63: Temperature Sensor

Register	Function	Setting	Mode	HW Rst	SW Rst
3.8043.7:0	Temperature Value	Temperature in °C = 3.8043.7:0 - 75, that is, for 100°C, the value is 1010_1111.	RO	xx	xx

To detect the high-temperature condition, the INTn pin must be asserted. Also, register bits 3.FE16.8 and 3.8010.11 must be enabled to allow the interrupt condition to propagate to the INTn pin.

2.21 Regulators and Power Supplies

The BRIGHTLANE™ 88Q2220/88Q2220M/88Q2221/88Q2221M devices have built-in regulators to support single rail operation from a 3.3V source. These internal regulators generate 1.2V and 0.75V[1]. The integrated regulators greatly reduce the PCB BOM cost. If regulators are not used, then an external 1.2V and 0.75V[1] supply are required. The following tables list the valid combinations of regulator usage.

The VDDO supply can operate at 1.8V/2.5V/3.3V supplies.

Note

- If VDDO is tied to either 1.8V or 2.5V, then the I/Os are not 3.3V tolerant.

Table 64: Power Supply Options — Integrated Regulator (REG_IN)

Functional Description	AVDD33	AVDDL	DVDD	Setup
Supply Source	3.3V	1.2V from Internal Regulator	0.75V[1] from Internal Regulator	Single 3.3V external supply Internal regulator enabled with external FETs.

Table 65: Power Supply Options — External Supplies

Functional Description	AVDD33	AVDDL	DVDD	Setup
Supply Source	3.3V	1.2V from External Regulator	0.75V[1] from External Regulator	3.3V, 1.2V, and 0.75V[1] external supplies Internal regulators disabled.

1. 0.75V applies for Rev B0/B1. 0.80V applies for Rev B2.

Table 66: Power Supply Options — External 0.75V[1], Integrated Regulator (REG_IN) Supplies Only 1.2V

Functional Description	AVDD33	AVDDL	DVDD	Setup
Supply Source	3.3V	1.2V from Internal Regulator	0.75V[1] from External Regulator	Internal regulator enabled but only for 1.2V. 0.75V[1] supplied externally.

Table 67: Power Supply Options — External 1.2V to AVDDL, Integrated Regulator (REG_IN) Supplies DVDD 0.75V[1] Only

Functional Description	AVDD33	AVDDL	DVDD	Setup
Supply Source	3.3V	AVDDL externally supply with 1.2V	DVDD from internal regulator	DVDD from internal regulator, sourced from external FET output. AVDDL supplied externally.

2.21.1 AVDDL

AVDDL is used as the 1.2V analog supply. AVDDL can be supplied externally with 1.2V or via the internal 1.2V LDO generated supply.

2.21.2 AVDD33

AVDD33 is used as a 3.3V analog supply and is the input supply of the internal LDO that generates the 1.2V for AVDDL.

2.21.3 DVDD

DVDD is used as the 0.75V[1] digital supply. DVDD can be supplied externally with 0.75V[1] or via the internal 0.75V[1] regulator generated supply.

2.21.4 REG_IN

REG_IN is used as the 3.3V supply to the internal buck regulator that generates the 0.75V[1] for DVDD. If the 0.75V[1] regulator is not used, then REG_IN must be left floating.

2.21.5 VDDO

VDDO supplies all digital I/O pins which use LVCMOS I/O standards. The supported voltages are 1.8V, 2.5V, or 3.3V.

Note LEDs cannot be used for VDDO 1.8V operation.

1. 0.75V applies for Rev B0/B1. 0.80V applies for Rev B2.

2.21.6 Regulator Configuration

Figure 32: Regulator-generated 1.2V for AVDDL

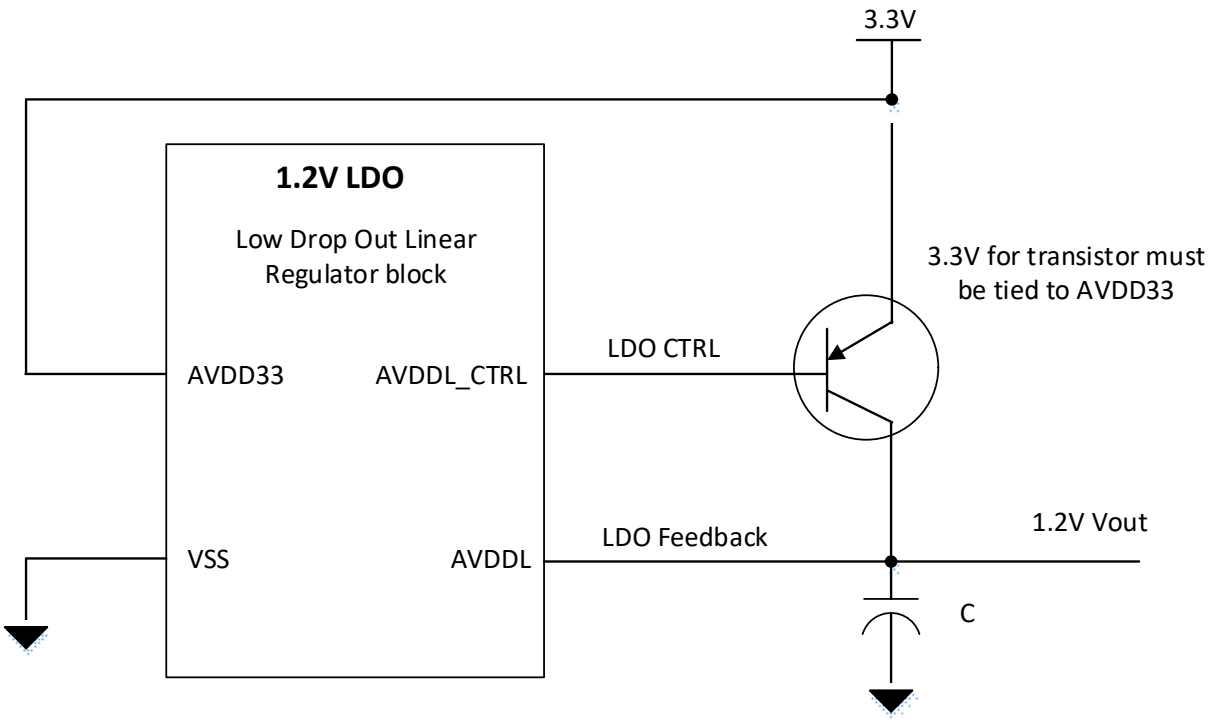
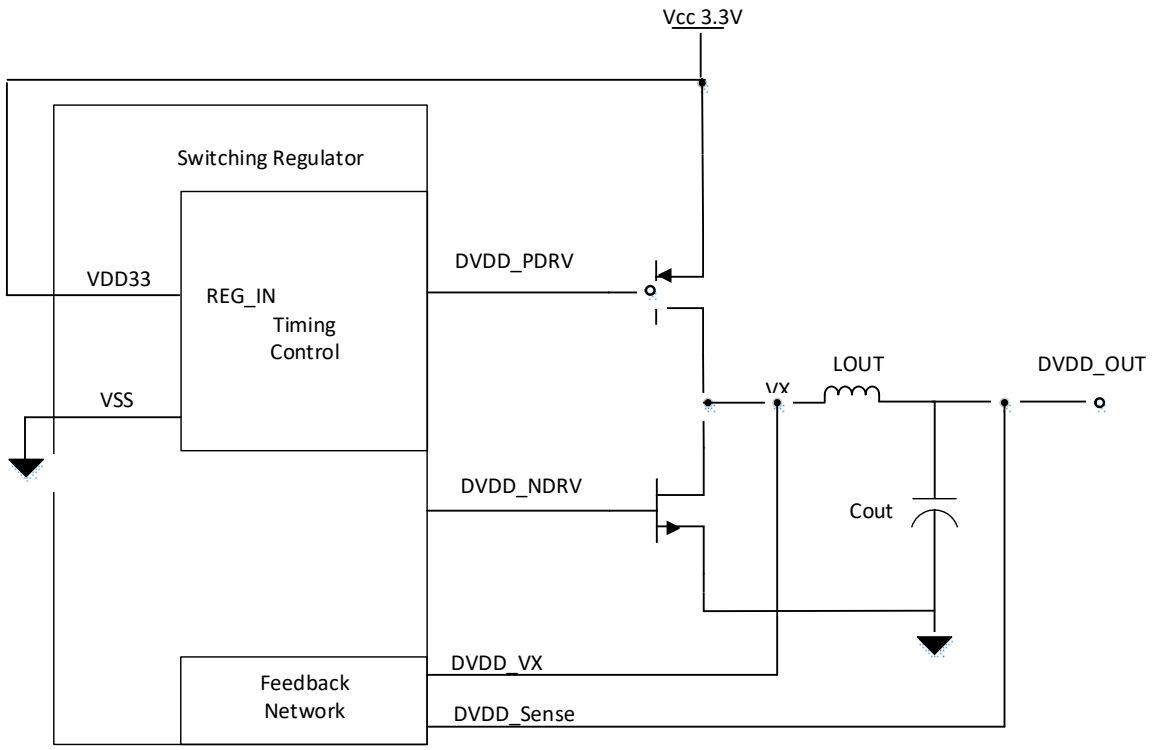


Figure 33: Regulator-generated for DVDD



2.21.7 Power Supply Sequencing

On power up, if all external supply option is used and internal regulators are not used, then each external supply rail can ramp up in any order without time limitation for non-TC10 applications. If TC10 will be used, then the power up time must meet the TC10 power up requirements. After all supplies are up and stable, and with a minimum of 1 ms RESETn assertion, the device can enter operation upon the de-assertion of RESETn.

The removal of supply rails can be in any order without time limitation. All supply rails must be removed and reached low before a new power up sequence. A supply rail reaching lower than 0.3V is considered functionally low.

If the internal supply option is used and VDDO = 3.3V, then the power up/down sequence is not necessary since only one main rail is ramping up. If VDDO is not at 3.3V, then it is the same requirement with the external supply option.

2.21.8 Under-voltage (UV) detection

The device continuously monitors the status of supply voltages. When any of the supply voltages AVDDL, AVDD33, DVDD, and VDDO drop below a specified minimum operating level, an under-voltage condition is triggered.

The device can be configured to generate an interrupt upon detection of an under-voltage condition.

When the power supply is stable, it is recommended that the user performs a hardware reset to restart the device. When enabled, by default under-voltage will trigger when the power supply falls below 6.29%. The recommended setting for under-voltage detection is 8.57%. For details, refer to registers 4.8700 through 4.8702.

Note For under-voltage trigger and recovery thresholds, there will be part-to-part variations.

2.22 Precision Time Protocol (PTP) Timestamping Support

Precision Timing Protocol (PTP) is used by IEEE specifications to determine the time of day for systems across a network. The IEEE specifications are IEEE 802.1AS, IEEE 1588 version 1, and IEEE 1588 version 2. The PTP protocol is typically used in audio video bridging (PTP) applications, or industrial and test automation applications.

The fundamental concept is to be able to time stamp the PTP frames with high precision as close to the physical wires as possible. As such, doing the time stamping in the PHY increases the accuracy compared to doing it in the MAC or higher layers since the MAC interface FIFOs can add up to ±2 bytes of uncertainty.

The PTP core in the device consists of two sub-cores, namely the Packet Time Stamping and the Time Application Interface (TAI). The time stamping core supports time stamping of frame formats as defined in IEEE 802.1AS, IEEE 1588v1, and IEEE 1588v2 frames.

2.22.1 PTP Control

To support the PTP Time Stamping function, the device has three pins that are global to the entire PHY:

- PTP Event Request input pin (the LED/GPIO pin is used for this purpose)
- PTP Trigger Generate output pin (the LED/GPIO[1] pin is used for this purpose)
- Interrupt pin

2.22.1.1 PTP Event Request

The PTP Event Request input pin can be configured to capture an external event (referred to as EventReq) and record the time at which the event occurred using the PTP Global Time Register (PTP Global Time Register – registers 1F.A84E and 1F.A84F). Users must program 4.87F0.7:4 to select whether LED or GPIO are used to enable this function. The definition of an external event is a low-to-high transition or a high-to-low transition on the LED/GPIO pin. Register 1F.A840 bit 13 (Event Phase) selects which transition (rising or falling) is used. The event time is captured in EventCapRegister (Event Capture Register – registers 1F.A84A and 1F.A84B). This field is validated by the EventCapValid bit (TAI Global Configuration Register – register 1F.A849).

2.22.1.2 PTP Trigger Generate

The PTP Trigger Generate output pin is used to output an external signal (referred to as TrigGenResp) when the internal Time of Day counter matches a value programmed into a PHY register. When there is a match, this output will go from low to high or from high to low, based on register 1F.A840 bit 12 (TrigPhase). The LED or GPIO pin is used for this function. It is selected by setting register 4.87F0.7:4 selection. The trigger output can also be a pulse or a clock, depending on what is programmed in register 1F.A840, bit 1 (TrigMode).

2.22.1.3 PTP Control Register

The PTP circuit timestamps packets as it passes through the PHY. The register control to this function can be accessed via registers 1F.A8xx. The PTP circuit can be powered down when it is not used via register 4.87F0.9. When register 4.87F0.9 is set to 1, the registers in 1F.A8xx are not accessible since the entire circuit is powered down.

By default, register 4.87F0.9 is set to 1. It must be set to 0 to enable PTP.

For the register description, see Table 319.

2.22.2 Packet Time Stamping

2.22.2.1 Time Stamping without Hardware Acceleration

The device supports two sets of hardware arrival time stamp registers to be able to capture two different PTP event messages' time stamp before the CPU reads the time stamp registers out of the device. For every incoming PTP message type, either PTPArr0Time (PTP Arrival 0 Time Registers – registers 1F.A80A and 1F.A80B) or PTPArr1Time (PTP Arrival 1 Time Registers – registers 1F.A80D and 1F.A80E) can be chosen by configuring TSArrPtr (PTP Global Configuration Register 2 – register 1F.A862). The SequenceID from the PTP Common header is captured as part of Arrival 0, Arrival 1, and/or Departure time stamp register sets, so the software can correlate the collected time stamps with the received or transmitted PTP event message. The hardware can be enabled to generate an interrupt upon capturing the time stamp information by writing a 0x1 to the interrupt enable register bits PTPArrIntEn (PTP Port Configuration Register 2 – register 1F.A802) for incoming PTP event messages or PTPDepIntEn (PTP Port Configuration Register 2 – register 1F.A802) for outgoing PTP event messages. In addition to generating an interrupt on the interrupt pin, an interrupt status (PTPArr0IntStatus, PTPArr1IntStatus, and PTPDepIntStatus) gets generated, which indicates if there were to be an error related to the time stamp register. The interrupt status gets set to 0x1 when the time stamp counter gets overwritten before the previous time stamp registers have been read out. The interrupt status gets set to a 0x2, when a time stamp could not be captured for a PTP event message because DisTSOverwrite (PTP Port Configuration Register – register 1F.A800) is set to 0x1.

Given that the device registers are accessed in units of 16 bits, to retain the entire 32-bit time stamp and the associated error messages and the SequenceID for a given PTP frame, the hardware treats the Arrival 0 block registers (registers 1F.A808 to 1F.A80B), Arrival 1 block registers (registers 1F.A80C, 1F.A80D, 1F.A80E, and 1F.A80F), and Departure block registers (registers 1F.A810 to 1F.A813) as a group and atomic operations are supported for these block of registers.

It is important to note that the device does not alter the contents of any PTP packet in either ingress or egress direction. Time stamping at the device level does not involve adding a time stamp to a packet or changing its CRC. It also does not involve the device looking at time stamps that are embedded within a packet. The PHY does not add any additional latency when the PTP function is enabled. The PHY only identifies that a packet is a PTP frame and records the enter and exit time. The PHY does this by parsing the packet for certain fields as described in later sections. If the packet is identified as such a PTP packet, the device loads the value of an internal "time of day counter" to a register showing the time for the first byte or SFD of the packet. The device then can inform the CPU or the PTP higher level firmware/software that such an event happened by activating an interrupt pin. The CPU can then read the relevant registers to find out if the event was in the Rx or TX direction and the value of the "time of day counter" when the event occurred.

Using the above time information and following the PTP protocol, the CPU or higher level entity can then determine the offset in time of day between a Grand Master Clock and the SLAVE node, as well as the frequency difference between the Grand Master Clock and the SLAVE clock in case they are not frequency-locked. These calculations are above the PHY level. The PHY provides full flexibility by allowing its time of day counter to be adjusted based on the CPU's calculations, as well as a totally new time of day value to be entered. The CPU can also use the time information provided by the PHY to create PTP packets that inform the link partners or the Grand Master when the packets had arrived or left the port in question.

The maximum jitter associated with capturing the time stamps collected by the logic is one TSClkPer (TAI Global Configuration Register 1 – register 1F.A841). Note that there are inherent delay variations introduced in PHY layer pipelines both in receive and transmit direction, which add to the overall jitter of the time stamps collected by the hardware and frequency/phase computations performed in PTP protocol software.

For achieving higher accuracies in terms of PTP, it is recommended that an external clock device is used to adjust the time stamping clock with the frequency/phase offset information computed in PTP protocol software. The frequency and/or phase adjusted clock can in turn be fed back into the device to be used by the time stamping logic.

2.22.2.2 Time Stamping with Hardware Acceleration

Hardware acceleration is available and can be turned on to offload the CPU from processing time stamp information.

Without the hardware acceleration, PTP frames are detected and the time stamp information is extracted and placed in registers so there is no alteration of any frames. A CPU or a higher level entity must access the relevant registers to obtain the time stamp information.

With the hardware acceleration, time stamp information is inserted directly into the PTP frame before it is transmitted to the CPU. Therefore, the CPU can obtain the time stamp information once the frame is received and does not need to access registers. In this case, PTP frames are being modified and additional latency is introduced due to the frame buffering and time stamp insertion.

Frames Involved

Hardware acceleration is achieved by modifying the seven frames mentioned earlier based on the mode of operation. Table 68 lists the fields of each of these frames.

Table 68: List of Frame's Fields

# Octet	Sync	Follow_Up	Delay_Req	Delay_Resp	Pdelay_Req	Pdelay_Resp	Pdelay_Resp_ Follow_Up
6	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr
6	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr
2	EtherType	EtherType	EtherType	EtherType	EtherType	EtherType	EtherType
	UDP Portion	UDP Portion	UDP Portion	UDP Portion	UDP Portion	UDP Portion	UDP Portion
1	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType
1 2	Rsvd, VersionPTP MessageLength	Rsvd, VersionPTP MessageLength	Rsvd, VersionPTP MessageLength	Rsvd, VersionPTP MessageLength	Rsvd, VersionPTP MessageLength	Rsvd, VersionPTP MessageLength	Rsvd, VersionPTP MessageLength
1	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber
1	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
2	FlagField	FlagField	FlagField	FlagField	FlagField	FlagField	FlagField
8	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField
4	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
10	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID
2	SeqID	SeqID	SeqID	SeqID	SeqID	SeqID	SeqID
1	ControlField	ControlField	ControlField	ControlField	ControlField	ControlField	ControlField
1	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval
10	OriginTS -1588 Rsvd –802.1AS	Precise OriginTS	OriginTS	ReceiveTS	OriginTS -1588 Rsvd –802.1AS	ReqReceiptTS	Response OriginTS
10		TLV – 802.1AS		ReqPortID	Rsvd	ReqPortID	ReqPortID
22	-		-	-	-	-	-

Data Receive Path

To accelerate the frames in hardware, the egress port needs information from the ingress port. The frame's ingress time stamp value is needed at the egress port to calculate the frame's residence time in the switch. When event frames ingress the switch, the hardware needs to embed the arrival time into the frame (in the 4 bytes RSVD location). In addition to the arrival time, in some cases, the correction field needs to be updated with the mean path delay and the delay asymmetry values at the ingress port.

Table 69: Receive Path Frame Modifications

Receive path
Fields highlighted in
Gray – Decode these fields in hardware (to determine if it is a supported PTP frame)
Blue – Modify these fields of the frame (as needed) in hardware
Green – Capture these fields of the frame in hardware to use for comparisons of associated frames

# Octet	Sync	Follow_Up	Delay_Req	Delay_Resp	Pdelay_Req	Pdelay_Resp	Pdelay_Resp_ Follow_Up
6	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr
6	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr
2	EtherType	EtherType	EtherType	EtherType	EtherType	EtherType	EtherType
	UDP Portion	UDP Portion	UDP Portion	UDP Portion	UDP Portion	UDP Portion	UDP Portion
1	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType	TransSpec, MessageType
1	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP
2	MessageLength	MessageLength	MessageLength	MessageLength	MessageLength	MessageLength	MessageLength
1	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber
1	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
2	FlagField	FlagField	FlagField	FlagField	FlagField	FlagField	FlagField
8	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField
4	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
10	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID
2	SeqID	SeqID	SeqID	SeqID	SeqID	SeqID	SeqID
1	ControlField	ControlField	ControlField	ControlField	ControlField	ControlField	ControlField
1	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval
10	OriginTS -1588	Precise OriginTS	OriginTS	ReceiveTS	OriginTS -1588	ReqReceiptTS	Response OriginTS
	Rsvd –802.1AS				Rsvd –802.1AS		
10		TLV – 802.1AS		ReqPortID	Rsvd	ReqPortID	ReqPortID
22	-		-	-	-	-	-

Data Transmit Path

Hardware acceleration involves modifying some of the frame's fields at the egress port. The required information is extracted from the frames and used to update them before transmitting the frames. The ingress time value should be extracted from the reserved location and the field zeroed out. Correction field will be updated on top of any modifications made at the ingress port.

Table 70: Transmit Path Frame Modifications

Transmit path
Fields highlighted in
Gray – Decode these fields in hardware (to determine if it is a supported PTP frame)
Blue – Modify these fields of the frame (as needed) in hardware
Green – Capture these fields of the frame in hardware to use for comparisons of associated frames
Red – Hardware can't modify these fields. The modification has to be done by software (after checking for associated frames)

# Octet	Sync	Follow_Up	Delay_Req	Delay_Resp	Pdelay_Req	Pdelay_Resp	Pdelay_Resp_Follow_Up
6	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr	Dest. Addr
6	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr	Source Addr
2	EtherType	EtherType	EtherType	EtherType	EtherType	EtherType	EtherType
1	UDP Portion TransSpec, MessageType	UDP Portion TransSpec, MessageType	UDP Portion TransSpec, MessageType	UDP Portion TransSpec, MessageType	UDP Portion TransSpec, MessageType	UDP Portion TransSpec, MessageType	UDP Portion TransSpec, MessageType
1	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP	Rsvd, VersionPTP
2	MessageLength	Message Length	MessageLength	MessageLength	MessageLength	MessageLength	MessageLength
1	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber	DomainNumber
1	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
2	FlagField	FlagField	FlagField	FlagField	FlagField	FlagField	FlagField
8	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField	CorrectionField
4	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd
10	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID	SourcePortID
2	SeqID	SeqID	SeqID	SeqID	SeqID	SeqID	SeqID
1	ControlField	ControlField	ControlField	ControlField	ControlField	ControlField	ControlField
1	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval	LogMsgInterval
10	OriginTS -1588 Rsvd –802.1AS	Precise OriginTS	OriginTS	ReceiveTS	OriginTS -1588 Rsvd –802.1AS	ReqReceiptTS	Response OriginTS
10		TLV – 802.1AS		ReqPortID	Rsvd	ReqPortID	ReqPortID
22	-		-	-	-	-	-

Frame Ingress Path Modification

When a frame ingresses a port, decoding its header determines if it is a PTP frame. If hardware acceleration is enabled (HA bit register 1F.A802), then IEEE 1588/802.1AS layer 2 frames of known time domains (PTP Global – register 1F.A872) and version number (PTP Global – register 1F.A807) are accelerated in hardware. The event frame's ingress time (IntPTPTime Register PTP Global – register 1F.A807) is placed in the 4 bytes of reserved space in the frame (bytes 17–20). The correction field of the frames is updated with MeanPathDelay and IngressDelayAsymmetry values whenever applicable, based on the mode of operation as described on "Equations Defining Frame Field Values" on page 106.

When a frame contains unknown domain number, unknown message type, or unsupported version number, it cannot be accelerated by hardware. In such cases, the event frame's arrival time (domain specific time or the hardware timer value) is embedded into the frame itself based on the ArrTSMode register value (PTP Port – register 1F.A802) so that the CPU has the ingress time information. If the ArrTSMode value is zero, the frame's arrival time is placed in the status registers (PTP Port – registers 1F.A808 to 1F.A80F, 1F.A80D, 1F.A80E, and 1F.A810).

A latency of about 8 byte times is introduced in the data path to achieve the hardware acceleration. Switching between bypass mode (no acceleration) and hardware acceleration mode should be done only when the port is idle to avoid corrupting the frames.

Frame Transmit Path Modification

When a frame egresses a port, decoding its header determines if it is a PTP frame. If hardware acceleration is enabled (HA bit register 1F.A802), then IEEE 1588/802.1AS layer 2 frames of know time domains (register 1F.A872) and version number (register 1F.A807, index 0x0) are accelerated in hardware. These frames could be coming from an ingress port (hardware accelerated at ingress) or from the CPU port (CPU must place the required data into the frames).

The event frame's ingress time (IntPTPTime Register – register 1F.A807) is extracted from the 4 bytes of reserved space in the frame (bytes 17–20) for use in further calculations and the reserved bytes zeroed out (unless KeepRxData bit of action vectors is set). The OriginTS field and the Correction field of the frames are updated whenever applicable, based on the mode of operation as described on "Equations Defining Frame Field Values" on page 106.

A latency of about 12 byte times is introduced in the data path to achieve the hardware acceleration. Switching between bypass mode (no hardware acceleration) and hardware acceleration mode should be done only when the port is idle to avoid corrupting the frames.

Sync – Follow_Up Frames

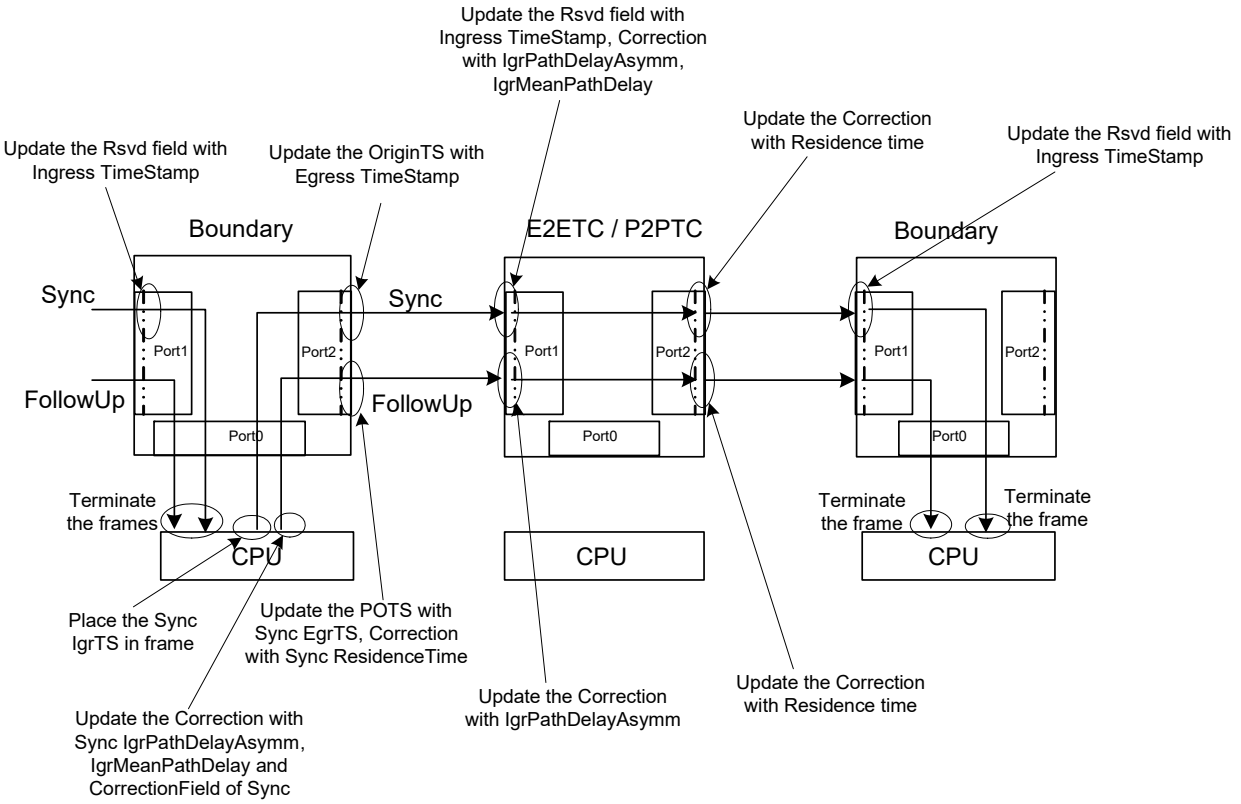
Sync and FollowUp frames travel in the same direction—from master to the slave. These frames contain master's timing information. A FollowUp frame and Sync frame are said to be associated frames if their SourcePortID and the SeqID match. A FollowUp frame should be modified only after checking its SourcePortID and SeqID against the previously received Sync frame to ensure that the associated frames are modified correctly. The fields to be updated in the FollowUp frame are ahead of the SourcePortID and the SeqID fields. The 'compare and then modify' method results in a long latency. So, the 'modify and then compare' method is used to avoid the latency, FollowUp frames are modified on the fly even before checking their SourcePortID and SeqID. After such modifications, when the SourcePortID and SeqID fields are reached in the frame, they are compared with that of the previous Sync frame. If they do not match, the FCS value of the FollowUp frame is purposefully corrupted before transmitting the frame.

At ingress, the hardware inserts the receive time into the Sync frames. The CorrectionField of the Sync and FollowUp frames is updated with MeanPathDelay and IngressDelayAsymmetry values whenever applicable, based on the mode of operation.

At the egress port, the Sync frame's ingress time is extracted from the reserved bytes (bytes 17–20 of PTP header) and the field is zeroed out before being transmitted (unless KeepRxData bit of action vectors is set). The Sync frame's OriginTS and CorrectionField are modified based on the equations matrix. The residence time of the Sync frame is saved to be used in updating the CorrectionField of the FollowUp frame when applicable. The FollowUp frame's preciseOriginTS and CorrectionField are modified on the egress path based on the equations matrix.

Figure 34 lists all possible modifications needed on Sync and FollowUp frames. However, it should be noted that the changes described in the figure do not all occur at the same time. Based on the mode, the device is in i.e. one-step, two-step, IEEE 1588 and so on, only some of the changes will be made at a time.

Figure 34: Sync-FollowUp Frame's Hardware Acceleration Path



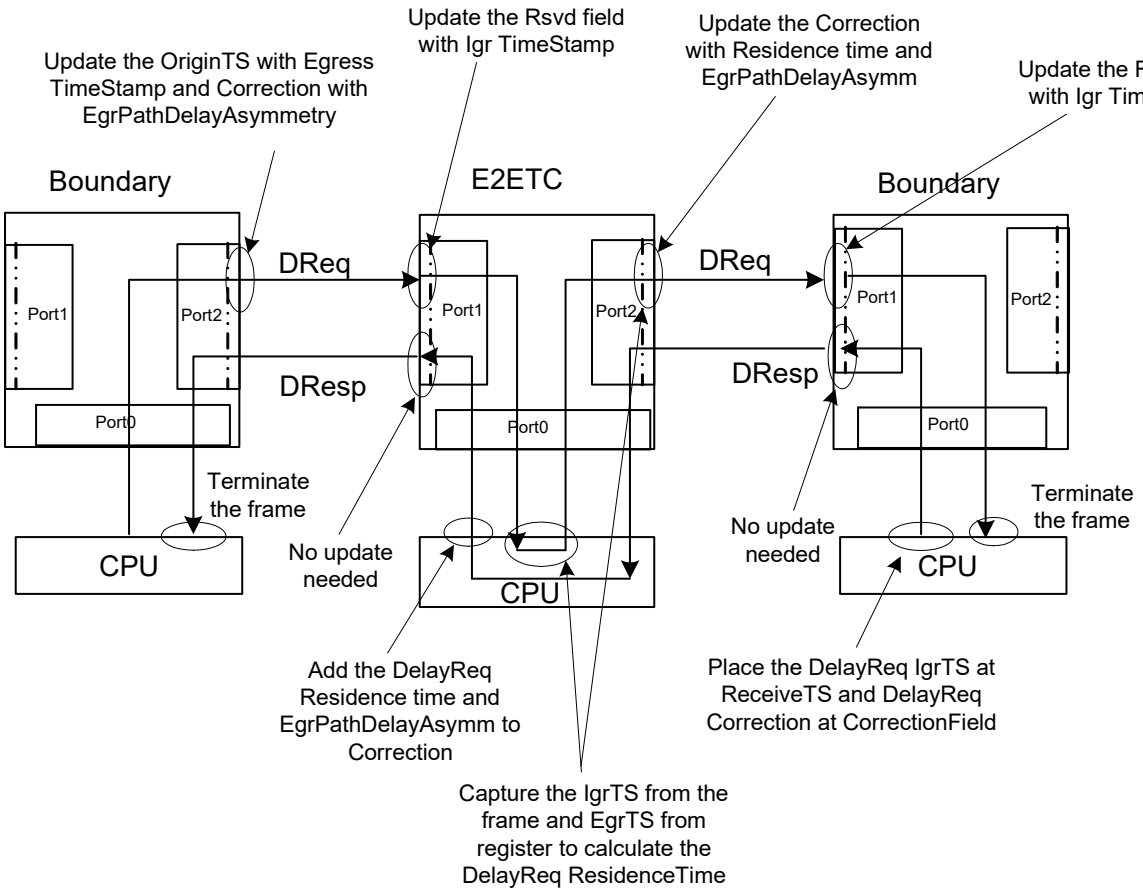
Delay_Request – Delay_Response Frames

DelayReq and DelayResp frames travel in opposite directions. DelayReq frame is sent by the slave and DelayResp frame is sent by the master port. At ingress, the hardware inserts the receive time into the DelayReq frames before sending them to the CPU. At egress port, the DelayReq frame's ingress time is extracted from the reserved bytes (bytes 17–20 of PTP header) and the field is zeroed out before being transmitted (unless KeepRxData bit of action vectors is set). The DelayReq frame's OriginTS and CorrectionField are modified based on the equations matrix. DelayReq frame's egress time is placed into the status registers so that the CPU can extract this information and use it to update the DelayResp frame.

A DelayReq frame and DelayResp frame are said to be associated frames if their SourcePortID and the SeqID match. A DelayResp frame should be modified with information from previously received DelayReq only after matching its SourcePortID and SeqID to ensure that they are associated frames. However, the hardware at egress port of DelayResp frame does not have the SourcePortId or SeqID values of the received DelayReq frame (opposite direction). So, the CPU needs to check SourcePortId and SeqId of the frames and add in the correct DelayReq frame's information (residence time, CorrectionField value and EgrPathDelayAsymm) to the DelayResp frames before transmission. The hardware does not modify/accelerate the DelayResp frames at egress.

Figure 35 lists all possible modifications needed on DelayReq and DelayResp frames. However, it should be noted that the changes described in the figure do not all occur at the same time. Based on the mode, the device is in i.e. one-step, two-step, IEEE 1588 and so on, only some of the changes will be made at a time.

Figure 35: DelayReq-DelayResp Frame's Hardware Acceleration Path



PDelayRequest, PDelayResponse, and PDelayResponseFollowUp Frames

PDelayReq frame is sent by the initiator to the responder. At ingress, the hardware inserts the receive time into the PDelayReq frames before sending them to the CPU. At egress port, the PDelayReq frame's ingress time is extracted from the reserved bytes (bytes 17–20 of PTP header) and the field is zeroed out before being transmitted (unless KeepRxData bit of action vectors is set). The PDelayReq frame's OriginTS and CorrectionField are modified based on the equations matrix. PDelayReq frame's egress time is placed into the status registers so that the CPU can extract this information and use it to update the PDelayResp/ PDelayRespFollowUp frame.

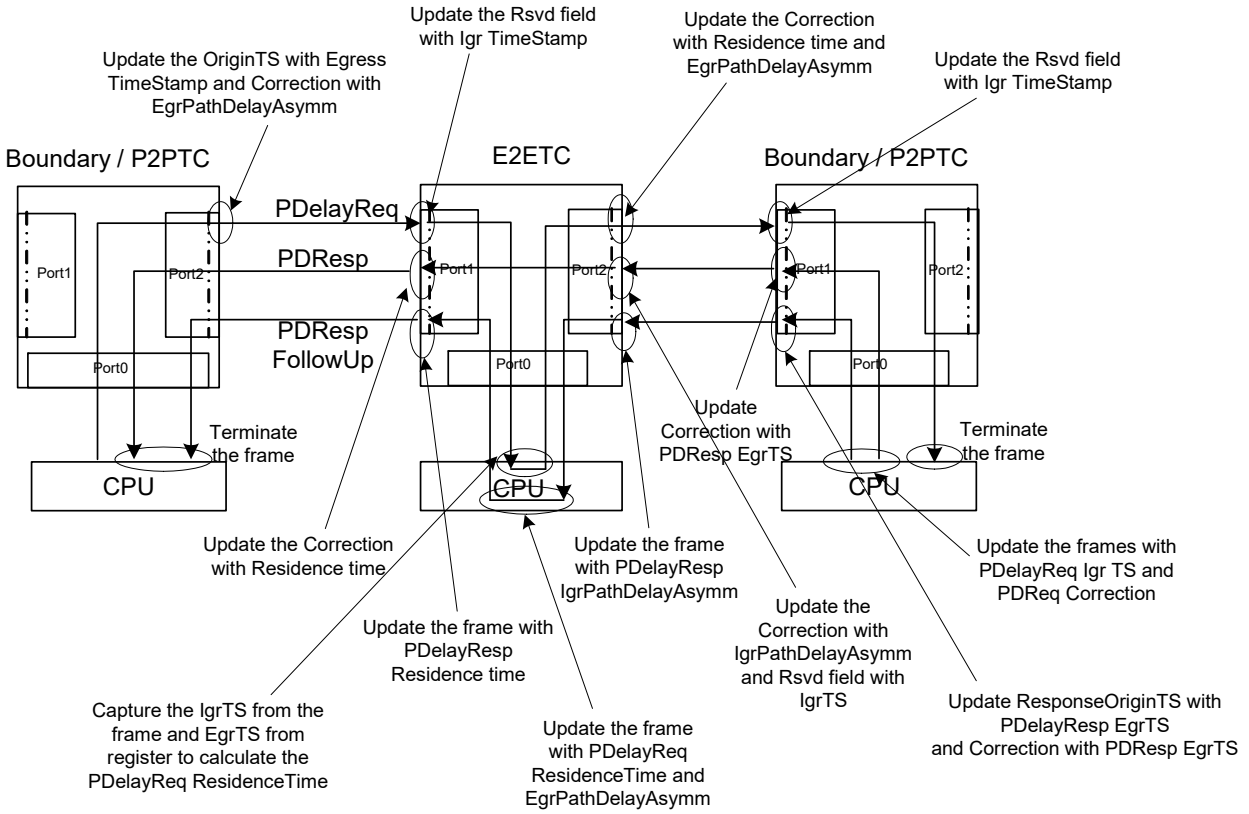
The PDelayResp frame is sent by the responder to the initiator, that is, in opposite direction than the PDelayReq frame. At ingress, the hardware inserts the receive time into the PDelayResp frames. A PDelayReq frame and PDelayResp frame are associated frames if the SourcePortID and SeqID of PDelayReq frame matches with the ReqPortID and the SeqID of PDelayResp frame. A PDelayResp frame should be modified only after checking its ReqPortID and SeqID against the SourcePortId and SeqID of previously received PDelayReq frame to ensure that the associated frames are modified correctly. However, the hardware at egress port of PDelayResp frame does not have the SourcePortId or SeqID values of the received PDelayReq frame (opposite direction). So, the CPU needs to match the frames and add in the correct PDelayReq frame's information to the

PDelayResp frames before transmission. The CorrectionField value of PDelayReq needs to be added to the CorrectionField of PDelayResp frames when applicable. The CPU should place the PDelayReq frame's IgrTS in the 4 reserved bytes (bytes 17–20 of PTP header) of PDelayResp frames when applicable. At egress, the hardware extracts this information and updates the PDelayResp frame's ReqReceiptTS and CorrectionField based on the equation's matrix.

PDelayResp and PDelayRespFollowUp frames travel in the same direction, from the responder to the initiator. A PDelayRespFollowUp frame and PDelayResp frame are associated with each other if their ReqPortID and the SeqID match. A PDelayRespFollowUp frame should be modified only after checking its ReqPortID and SeqID against the previously received PDelayResp frame to ensure that the associated frames are modified correctly. The fields to be updated in the PDRespFollowUp frame are ahead of the ReqPortID and the SeqID fields. The 'compare and then modify' method results in a long latency. So, the 'modify and then compare' method is used to avoid the latency, PDelayRespFollowUp frames are modified on the fly even before checking their ReqPortID and SeqID. After such modifications, when the ReqPortID and SeqID fields are reached in the frame, they are compared with that of the previous PDelayResp frame. If they do not match, then the FCS value of the PDelayRespFollowUp frame is purposefully corrupted before transmitting the frame. Similar to the PDelayResp frame's case, the hardware depends on the CPU to make PDelayReq related timing information changes to PDelayRespFollowUp whenever applicable.

Figure 36 lists all possible modifications needed on PDelayReq, PDelayResp, and PDelayRespFollowUp frames. However, it should be noted that the changes described in the figure do not all occur at the same time. Based on the mode the device is in i.e. one-step, two-step, IEEE1588 etc. only some of the changes will be made at a time.

Figure 36: PDelayReq, PDelayResp, PDelayRespFollowUp Frame's Hardware Acceleration Path



Equations Defining Frame Field Values

The following tables describe the equations that govern the frame field values based on various configurations supported.

Table 71: Sync Frame Equations Implemented

1. The boxes filled in red depict the special cases where the device works differently than described in the IEEE specification. The text describes the device's behavior in those cases.
2. The text highlighted in light grey is the ingress path function that is not performed in hardware. The frame is sent to CPU and it should take care of this portion.
3. The text highlighted in green is the information that CPU is required to supply the hardware in the egress path. That portion needs to be placed in the frame by the software.
4. Rest of the portion is done in hardware (combination of the ingress path and egress path)

			Ordinary/Boundary	Peer-To-Peer Transparent Clock	End-To-End Transparent Clock
Sync	**One Step**	**1588**	**OriginTS** = SyncEgrTS **CorrectionField** = Rx's CorrectionField (0) **CorrectionField(Rx)** = CorrField + IgrPathDelayAsym	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField + IgrMeanPathDelay + ResidenceTime + IgrPathDelayAsym	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField + ResidenceTime + IgrPathDelayAsym
	Two Step w/Rx **Two Step Flag = False**	**1588**	N/A	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
	Two Step w/Rx **Two Step Flag = True**	**1588**	**OriginTS** = Rx's OriginTS (0 or estimate SyncEgrTS) OR SyncEgrTS (Program action reg bit) **CorrectionField** = Rx's CorrectionField (0) **CorrectionField(Rx)** = CorrField + IgrPathDelayAsym	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
		802.1 AS	**OriginTS** - NA **CorrectionField** = Rx's CorrectionField (0) *i.e., frame not modified*	N/A	N/A

Table 72: FollowUp Frame Equations Implemented

			Ordinary/Boundary	Peer-To-Peer Transparent Clock	End-To-End Transparent Clock
FollowUp	**One Step**	**1588**	N/A	**PreciseOriginTS** = Rx's PreciseOriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*	**PreciseOriginTS** = Rx's PreciseOriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
	Two Step w/Rx Two Step Flag = False	**1588**	N/A	**PreciseOriginTS** = Rx's PreciseOriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*	**PreciseOriginTS** = Rx's PreciseOriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
	Two Step w/Rx Two Step Flag = True	**1588**	**PreciseOriginTS** = SyncEgrTS **Correction** = Rx's CorrectionField (0 – CorrectionField Sync)	**PreciseOriginTS** = Rx's PreciseOriginTS **Correction** = Rx's CorrectionField + ResidenceTime + IgrMeanPathDelay + IgrPathDelayAsym	**PreciseOriginTS** = Rx's PreciseOriginTS **Correction** = Rx's CorrectionField + ResidenceTime + IgrPathDelayAsym
		802.1 AS	**PreciseOriginTS** = (a) If GrandMaster: SyncEgrTS (b) If not the GrandMaster: Rx's PreciseOriginTS **Correction** = (a) If GrandMaster: Rx's CorrectionField (0) (b) If not the GrandMaster: Rx's CorrectionField + ResidenceTime + PropagationDelay (MeanPathDelay) + IgrPathDelayAsym	N/A	N/A

Table 73: DelayReq and DelayResp Frame Equations Implemented

			Ordinary/Boundary	Peer-To-Peer Transparent Clock	End-To-End Transparent Clock
Delay Req	**One Step**	**1588**	**OriginTS** = Rx's OriginTS (0 /estimate DelayReqEgrTS) OR DelayRespEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	Discard	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField + ResidenceTime - EgrPathDelayAsym
	Two Step w/Rx Two Step Flag = False	**1588**	**OriginTS** = Rx's OriginTS (0 /estimate DelayReqEgrTS) OR DelayRespEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	Discard	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
	Two Step w/Rx Two Step Flag = True	**1588**	**OriginTS** = Rx's OriginTS (0 /estimate DelayReqEgrTS) OR DelayRespEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	Discard	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
		802.1 AS	N/A	N/A	N/A
Delay Resp	**One Step**	**1588**	**ReceiveTS** = DelayReqIgrTS **Correction** = 0 + CorrectionField DelayReq *i.e., frame not modified*	Discard	**ReceiveTS** = Rx's ReceiveTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
	Two Step w/Rx Two Step Flag = False	**1588**	**ReceiveTS** = DelayReqIgrTS **Correction** = 0 + CorrectionField DelayReq *i.e., frame not modified*	Discard	**ReceiveTS** = Rx's ReceiveTS **Correction** = Rx's CorrectionField + ResidenceTime DelayReq – EgrPathDelayAsym of DelayReq *i.e., frame not modified*
	Two Step w/ Rx Two Step Flag = True	**1588**	**ReceiveTS** = DelayReqIgrTS **Correction** = 0 + CorrectionField DelayReq *i.e., frame not modified*	Discard	**ReceiveTS** = Rx's ReceiveTS **Correction** = Rx's CorrectionField + ResidenceTime DelayReq – EgrPathDelayAsym of DelayReq *i.e., frame not modified*
		802.1 AS	N/A	N/A	N/A

Table 74: PDelayReq Frame Equations Implemented

			Ordinary/Boundary	Peer-To-Peer Transparent Clock	End-To-End Transparent Clock
Pdelay Req	**One Step**	**1588**	**OriginTS** = Rx's OriginTS (0/ estimate PdelayReqEgrTS) OR PdelayReqEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	**OriginTS** = Rx's OriginTS (0/ estimate PdelayReqEgrTS) OR PdelayReqEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField + Residence Time PdelayReq – EgrPathDelayAsym
	Two Step w/Rx Two Step Flag = False	**1588**	**OriginTS** = Rx's OriginTS (0/ estimate PdelayReqEgrTS) OR PdelayReqEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	**OriginTS** = Rx's OriginTS (0/ estimate PdelayReqEgrTS) OR PdelayReqEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
	Two Step w/Rx Two Step Flag = True	**1588**	**OriginTS** = Rx's OriginTS (0/ estimate PdelayReqEgrTS) OR PdelayReqEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	**OriginTS** = Rx's OriginTS (0/ estimate PdelayReqEgrTS) OR PdelayReqEgrTS (Program action reg) **Correction** = Rx's CorrectionField (0) - EgrPathDelayAsym	**OriginTS** = Rx's OriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
		802.1 AS	**OriginTS** = NA **Correction** = Rx's CorrectionField (0) *i.e., frame not modified*	N/A	N/A

Table 75: PDelayResp Frame Equations Implemented

			Ordinary/Boundary	Peer-To-Peer Transparent Clock	End-To-End Transparent Clock
Pdelay Resp	**One Step**	**1588**	**ReqReceiptTS** = Rx's ReqReceiptTS (0) **Correction** = CorrectionField of PdelayReq + (PDRespEgrTS – PDReqIgrTS) **Rsvd** = PDReqIgrTS **CorrectionField(Rx)** = CorrField + IgrPathDelayAsym	**ReqReceiptTS** = Rx's ReqReceiptTS (0) **Correction** = CorrectionField of PdelayReq + (PDRespEgrTS – PDReqIgrTS) **Rsvd** = PDReqIgrTS **CorrectionField(Rx)** = CorrField + IgrPathDelayAsym	**ReqReceiptTS** = Rx's ReqReceiptTS **Correction** = Rx's CorrectionField + ResidenceTime Pdelay_Resp + IgrPathDelayAsym
	Two Step w/Rx **Two Step Flag = False**	**1588**	N/A	N/A	**ReqReceiptTS** = Rx's ReqReceiptTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
	Two Step w/Rx **Two Step Flag = True**	**1588**	**ReqReceiptTS** = (a) Rx's ReqReceiptTS (0) OR (b) ReqReceiptTS (PDelayReqIgrTS) **Correction** = (a) Rx's CorrectionField (0) OR (b) Rx's CorrectionField (0) **CorrectionField(Rx)** = CorrField + IgrPathDelayAsym	**ReqReceiptTS** = (a) Rx's ReqReceiptTS (0) OR (b) ReqReceiptTS (PDelayReqIgrTS) **Correction** = (a) Rx's CorrectionField (0) OR (b) Rx's CorrectionField (0) **CorrectionField(Rx)** = CorrField + IgrPathDelayAsym	**ReqReceiptTS** = Rx's ReqReceiptTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
		802.1 AS	**ReqReceiptTS** = Rx's ReqReceiptTS (PDelayReqIgrTS) **Correction** = Rx's CorrectionField (0) *i.e., frame not modified*	N/A	N/A

Table 76: PDelayRespFollowUp Frame Equations Implemented

			Ordinary/Boundary	Peer-To-Peer Transparent Clock	End-To-End Transparent Clock
Pdelay Resp FollowUp	**One Step**	**1588**	N/A	N/A	**ResponseOriginTS** = Rx's ResponseOriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
	Two Step w/Rx Two Step Flag = False	**1588**	N/A	N/A	**ResponseOriginTS** = Rx's ResponseOriginTS **Correction** = Rx's CorrectionField *i.e., frame not modified*
	Two Step w/Rx Two Step Flag = True	**1588**	**ResponseOriginTS** = (a) Rx's ResponseOriginTS (0) OR (b) PdelayRespEgrTS **Correction** = Correction Field PdelayReq + (a) PdelayRespEgrTS-PdelayReqIgrTS OR (b) 0 **Rsvd** = (a) PdelayReqIgrTS	**ResponseOriginTS** = (a) Rx's ResponseOriginTS (0) OR (b) PdelayRespEgrTS **Correction** = Correction Field PdelayReq + (a) PdelayRespEgrTS-PdelayReqIgrTS OR (b) 0 **Rsvd** = (a) PdelayReqIgrTS	**ResponseOriginTS** = Rx's ResponseOriginTS **Correction** = Rx's Correction field + Residence Time of PdelayReq + Residence Time of PdelayResp + IgrPathDelayAsym of PDelayResp – EgrPathDelayAsym of PDelayReq
		802.1 AS	**ResponseOriginTS** = PdelayRespEgrTS **Correction** = Rx's Correction field (0)	N/A	N/A

The PdelayResp and PdelayRespFollowUp frames follow either scheme (a) or (b), based on the register selection.

2.22.3 Time Application Interface (TAI)

The Precision Time Protocol provides both frequency and time of day with respect to the PTP Grand Master for the entire PTP network. In a given endpoint device (media talker or a media listener), once the PTP Grand Master aware clock and time are available, it needs to be transported over to the rest of the subsystem without loss of accuracy. For example, if a Digital Video Recorder (DVR) is the end device, the network clock and time need to be transported to the video SoC and/or storage SoC and to the host processor seamlessly. This ensures that when the media is played out of the DVR, the network time aware presentation time of the content is required to be carried through.

The TAI "Timing Interface Block" supports features required for the above purpose. This block utilizes two signals to offer various services. One signal is called EventRequest input signal, and the second is called TriggerGenerate output signal.

Using the above signals, there are several functions that this block supports:

- An event pulse capture function.
- Multiple event counter function.
- A trigger pulse generate function with pulse width control.
- A trigger clock generate function with digital clock compensation.
- A multi-PTP device time sync function.

2.22.3.1 Event Pulse Capture Interface

In many IEEE 1588 applications like industrial automation and so on, it is important to precisely capture the time at which a particular event has happened. The event is defined by a low-to-high or high-to-low transition on an external signal called EventRequest. The event time is captured in EventCapRegister (registers 1F.A84A and 1F.A84B). This field is validated by EventCapValid bit (TAI Global Configuration – register 1F.A849).

The captured event time register must be read out by the software and the valid bit must be cleared before the hardware captures another event. If there were to be two back-to-back events before the software read the results of the first event, an error indication is set in EventCapErr (TAI Global Configuration – register 1F.A849). If the user chooses that the hardware rather overwrite the Event capture register, then it can be configured by setting a 0x1 to EventCapOv (TAI Global Configuration – register 1F.A840).

When an event has been captured, the software can optionally (EventCapIntEn – register 1F.A840) be interrupted and an EventInt (register 1F.A850) bit is also set.

The maximum jitter associated with capturing the EventRequest signal pulse is one TSClkPer (TAI Global Configuration – register 1F.A841). The minimum pulse width of the EventRequest signal needs to be 1.5 times the TSClkPer (TAI Global Configuration – register 1F.A841). For the hardware logic to detect distinct events on the EventRequest signal, the minimum gap between two events needs to be 150 ns plus 5 times the TSClkPer amount.

2.22.3.2 Multiple Event Counter Function

Similar to the previously described Event Pulse capture interface, if multiple events must be captured for an application to detect the amount of time a particular event occurs on the EventRequest input signal, EventCtrStart (TAI Global Configuration Register – register 1F.A840) needs to be set to 0x1 and EventCapOv (TAI Global Configuration Register – register 1F.A840) needs to set to 0x1.

The Multiple Event Counter function is capable of capturing up to 255 events in EventCapCtr (TAI Global Configuration – register 1F.A850).

The maximum jitter associated with capturing the EventRequest signal pulse is one TSClkPer (TAI Global Configuration – register 1F.A841). The minimum pulse width of the EventRequest signal needs to be 1.5 times the TSClkPer (TAI Global Configuration – register 1F.A841). For the hardware logic to detect distinct events on the EventRequest signal, the minimum gap between two events needs to be 150 ns plus 5 times the TSClkPer amount.

Note

In the multiple event counter mode, the EventCapRegister (registers 1F.A84A and 1F.A84B) indicate the time stamp value for the last captured event register.

2.22.3.3 Trigger Pulse Generate Function

In many PTP applications, the time of day computed in PTP must be distributed in some form to the rest of the node. One commonly used method is to generate a pulse whenever the PTP Global Time matches a certain configured value. The pulse gets output on a TrigGenResp output signal.

The above function can be achieved by:

a) Configuring the TrigMode (TAI Global Configuration Register 1F.A840) to 0x1 and
b) Configuring the time amount when the pulse must be generated in TrigGenAmt (TAI Global Configuration Registers 1F.A842 and 1F.A843) and
c) Configuring the TrigGenReq (TAI Global Configuration Register 1F.A840) to 0x1

The PTP Global Timer gets compared to the TrigGenAmt, and upon a match a pulse signal gets generated on the TrigGenResp output signal.

Optionally after generating the TrigGenResp pulse, the CPU can be notified by setting TrigGenIntEn (TAI Global Configuration Register 1F.A840), and along with the pulse output the TrigGenInt bit (PTP Status 5 1F.A868) gets set. Upon receiving the interrupt, it is the function of the CPU to clear the interrupt bit.

The pulse width of the output signal can be controlled by PulseWidth (TAI Global Configuration Register 1F.A845). Do not set the PulseWidth to a zero value.

2.22.3.4 Trigger Clock Generate Function

Similar to the previously described trigger pulse generation function, the same set of registers can be used to generate a periodic clock. The value specified in TrigGenAmt (TAI Global Configuration Register 1F.A842 and 1F.A843) is used to generate the base period of the clock output. For this functional mode, the TrigMode (TAI Global Configuration Register 1F.A840) must be set to 0x0 and TrigGenReq (TAI Global Configuration Register 1F.A840) must be set to 0x1.

The output clock can be compensated by configuring field TrigClkComp (TAI Global Configuration Register 1F.A844) and TrigClkCompSubps (TAI Global Configuration Register 1F.A845). This field specifies the remainder amount for the clock that is being generated with the period specified by TrigGenAmt. The TrigClkComp amount gets constantly accumulated and when this accumulated amount exceeds the value specified in TSClkPer, a TSClkPer gets added to the output clock momentarily to compensate for the remainder accumulated over time.

A start time for the clock may be chosen (TAI Global Registers 1F.A850 and 4.8C0A and Register 4.8C0A). Also, a compensation direction may be chosen by indicating the amount to add or subtract in register 1F.A844, bit 15 (TrigCompDir).

Note

TrigGenAmt should be set to no less than 2 times the TSCLKPer amount.

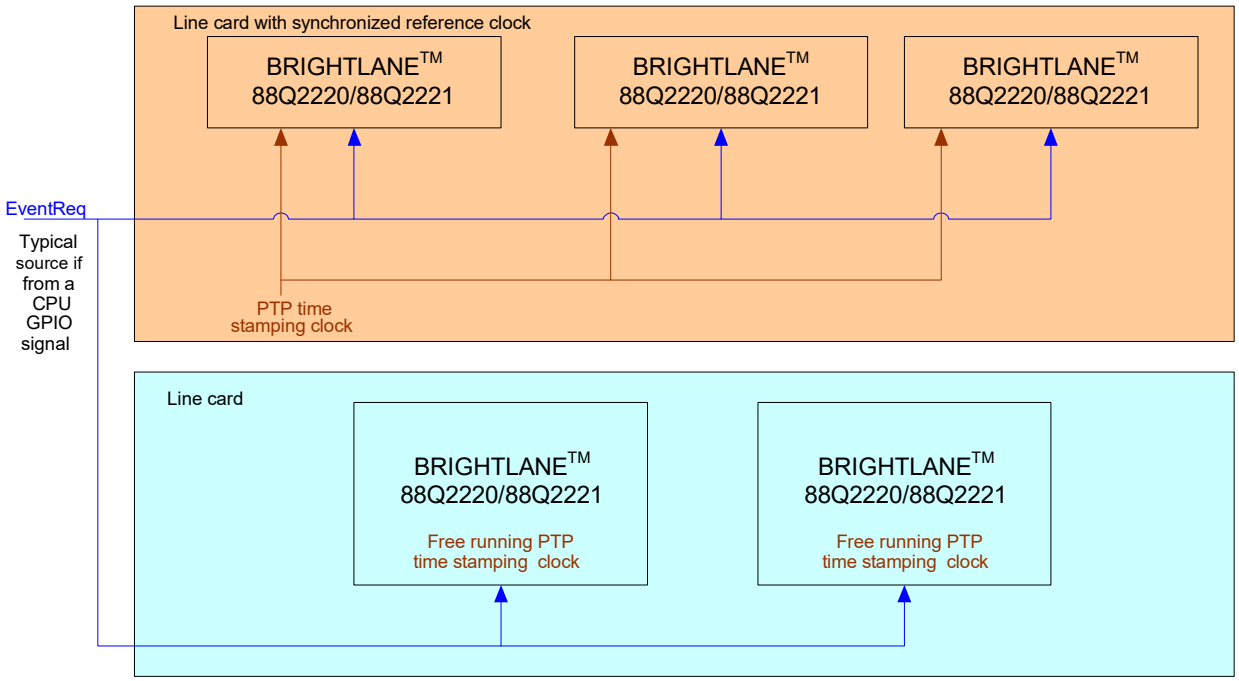
2.22.3.5 Multi-PTP Device Time Sync Function

When PTP is enabled on devices on enterprise, service provider line cards and/or chassis, it is important for various PTP capable devices on the system to have the common notion of PTP Global Time. Typically, a central processing card is present in these chassis, which runs the PTP software for the entire chassis, and all the data line cards send the PTP frames and the time stamp information to the central PTP software entity. Given that there can be so many ports on each line card and each of the line cards may be plugged into the chassis at different times, the PTP Global

Time counter value in each of the PTP devices on the line cards may not be synchronized. Thus, the hardware needs to provide a sure short way for all the PTP capable devices across various line cards, regardless of when the line cards have been powered on, to be synchronized to the same PTP Global Time so that the PTP protocol software does not have to remember the offsets with respect to the PTP Grand Master and also with respect to each of these devices.

The background for this feature is that the PTP nodes derive the time of day via PTP message exchange. The derived time of day consists of 64 bits of seconds and 32 bits of nanoseconds. The PTP slave nodes are expected to derive the frequency and phase offset information with respect to the PTP Grand Master node. The derived offset information is used to periodically adjust various device PTP global timer values. For multi-PTP (BRIGHTLANE™ devices only) capable devices, the goal is to synchronize all the nodes with a common 32-bit nanoseconds field and also adjust the nanoseconds field with the computed PTP Grand Master offset information.

Figure 37: Multiple Devices Across Multiple Line Cards Connected by an EventReq Input Signal



This feature is enabled by setting MultiPTPSyncMode (TAI Global Configuration Register 1F.A840) to 0x1. Note that when this bit is enabled, the functions EventRequest and TriggerGen are disabled.

When MultiPTPSyncMode is 0x1, a low-to-high or high-to-low transition on the EventRequest signal triggers transfer of TrigGenAmt to the PTP Global Timer register. At the timer of the low-to-high or high-to-low transition for further software time correlation, the EventCapTime register is also updated with the value of the PTP Global Time before it gets overwritten.

Note that even though the previously described schema ensures that the PTP Global Time register value is synchronized, the following are possible sources of jitter associated from a system level (which can be avoided):

a) The reference clock sources for various PTP devices that support the multi-sync EventReq interface on the same line card and/or across line cards may not be synchronized.

b) The added delays in the clock path between various PTP devices that support the multi-sync EventReq interface on the same line card and/or across line cards.
c) Inherent operating system related jitter from the point a command is issued to when it actually gets executed in hardware. This is applicable for EventReq pulse generation from a GPIO as well and has an increased level of predictability with real-time operating systems.

One guaranteed method to avoid the previously mentioned jitter factors a and b is by using a flip-flop with the EventReq as the data input and PTP time stamping clock as the clock input into the flop and the flop output gets distributed with matched delays across various PTP devices that support the multi-sync EventReq. One method to reduce the operating system associated uncertainties, is to choose an operating system in which the scheduler tasks are predictable down to 1's of nanoseconds accuracy.

2.22.4 ReadPlus Command

The PTP Global Time registers are used as 32-bit global timer value that is running off of the free-running PHY clock. A read from the PTP Global Time registers must be done with the ReadPlus command. ReadPlus can only be used after powering up the PTP Block. Otherwise, it will return 0. A read directly to the PTP Global Time registers without using the ReadPlus command will return 0. The PTP Global Time registers value can be loaded directly by writing back-to-back to the PTP Global Time register byte 3 & 2 – register 1F.A84F first, followed by PTP Global Time Register Byte 1 & 0 – register 1F.A84E. ReadPlus can read up to four consecutive registers.

The following shows the formula to program PTP ReadPlus Command Register 1F.A86E and the examples of PTP registers that need ReadPlus commands. The only exception is that PTPAddr for PTP Event Capture Time register does not follow this formula, as shown in following example.

PTPAddr[3:0] = Lower four bits of the register address to be read:

PTPReg = 0x0 (1.A800 – 1F.A81F)

PTPAddr[4] = '0' (1.A8xx)

PTPReg = 0xE (1F.A840 – 1F.A850)

PTPAddr[4] = '0' (1F.A8xx)

PTPReg = 0xF (1F.A860 – 1F.A87F)

PTPAddr[4] = '0' (1F.A8xx)

1. Write to register 1F.A86E = 0x8E0E (ReadPlus command for PTP Global Time Register 1F.A84E to 1F.A84F).
2. Read from register 1F.A81F (PTP Global Time Register bits [15:0]).
3. Read from register 1F.A81F (PTP Global Time Register bits [31:16]).

1. Write to register 1F.A86E = 0x8F10 (ReadPlus command for TOD Load Point Register 4.8F00 to 1F.A872).
2. Read from register 1F.A81F (PTP TOD Load Point Register bits [15:0]).
3. Read from register 1F.A81F (PTP TOD Load Point Register bits [31:16]).
4. Read from register 1F.A81F (PTP TOD Control Register 1F.A872).

1. Write to register 1F.A86E = 0x8F13 (ReadPlus command for TOD Nano Register 4.8F03 to 4.8F04).
2. Read from register 1F.A81F (PTP TOD Nano Register bits [15:0]).
3. Read from register 1F.A81F (PTP TOD Nano Register bits [31:16]).

1. Write to register 1F.A86E = 0x8F15 (ReadPlus command for TOD Sec Register 4.8F05 to 4.8F07).
2. Read from register 1F.A81F (PTP TOD Sec Register bits [15:0]).
3. Read from register 1F.A81F (PTP TOD Sec Register bits [31:16]).
4. Read from register 1F.A81F (PTP TOD Sec Register bits [47:32]).

1. Write to register 1F.A86E = 0x8F18 (ReadPlus command for 1722 Nano Register 4.8F08 to 4.8F0B).
2. Read from register 1F.A81F (PTP 1722 Nano Register bits [15:0]).
3. Read from register 1F.A81F (PTP 1722 Nano Register bits [31:16]).
4. Read from register 1F.A81F (PTP 1722 Nano Register bits [47:32]).
5. Read from register 1F.A81F (PTP 1722 Nano Register bits [63:48]).

1. Write to register 1F.A86E = 0x8F1C (ReadPlus command for TOD Comp Register 4.8F0C to 4.8F1D).
2. Read from register 1F.A81F (PTP TOD Comp Register bits [15:0]).
3. Read from register 1F.A81F (PTP TOD Comp Register bits [31:16]).

1. Write to register 1F.A86E = 0x8E0A (ReadPlus command for Event Capture Register 1F.A84A and 1F.A84B).
2. Read from register 1F.A81F (PTP Event Capture Register bits [15:0]).
3. Read from register 1F.A81F (PTP Event Capture Register bits [31:16]).

1. Write to register 1F.A86E = 0x8008 (ReadPlus command for Arrival 0 Register 1F.A808 to 1F.A80B).
2. Read from register 1F.A81F (PTP Arrival 0 Register 1F.A808).
3. Read from register 1F.A81F (PTP Arrival 0 Time Register bits [15:0]).
4. Read from register 1F.A81F (PTP Arrival 0 Time Register bits [31:16]).
5. Read from register 1F.A81F (PTP Arrival 0 SeqID Register 1F.A80B).

1. Write to register 1F.A86E = 0x800C (ReadPlus command for Arrival 1 Register 1F.A80C, 1F.A80D, 1F.A80E, 1F.A80F).
2. Read from register 1F.A81F (PTP Arrival 1 Register 1F.A80C).
3. Read from register 1F.A81F (PTP Arrival 1 Time Register bits [15:0]).
4. Read from register 1F.A81F (PTP Arrival 1 Time Register bits [31:16]).
5. Read from register 1F.A81F (PTP Arrival 1 SeqID Register 1F.A80F).

1. Write to register 1F.A86E = 0x8010 (ReadPlus command for Departure Register 1F.A810 to 1F.A813).
2. Read from register 1F.A81F (PTP Departure Register 1F.A810).

3. Read from register 1F.A81F (PTP Departure Time Register bits [15:0]).
4. Read from register 1F.A81F (PTP Departure Time Register bits [31:16]).
5. Read from register 1F.A81F (PTP Departure SeqID Register 1F.A80F).

Note

These registers must use the ReadPlus command; otherwise, the read-back value is incorrect:

- 1F.A870 to 1F.A87F (PTP Global Time Array Registers)
- 1F.A84E and 1F.A84F (PTP Global Time [31:0])
- 1F.A84A and 1F.A84B (Event Capture Time [31:0])
- 1F.A808 to 1F.A80B (PTP Arrival 0)
- 1F.A80C, 1F.A80D, 1F.A80E, and 1F.A80F (PTP Arrival 1)
- 1F.A810 to 1F.A813 (PTP Departure)

2.23 MMAC: MAC and MACsec

2.23.1 Overview

The MAC and MACsec (MMAC) module for this device performs all the necessary tasks of data buffering, MACsec classification, MAC Security Entities (SecY) frame transformation, and flow control management for full IEEE 802.1AE, 802.1AEbn, and 802.1AEbw-compliance operations. The key features of the MMAC module include:

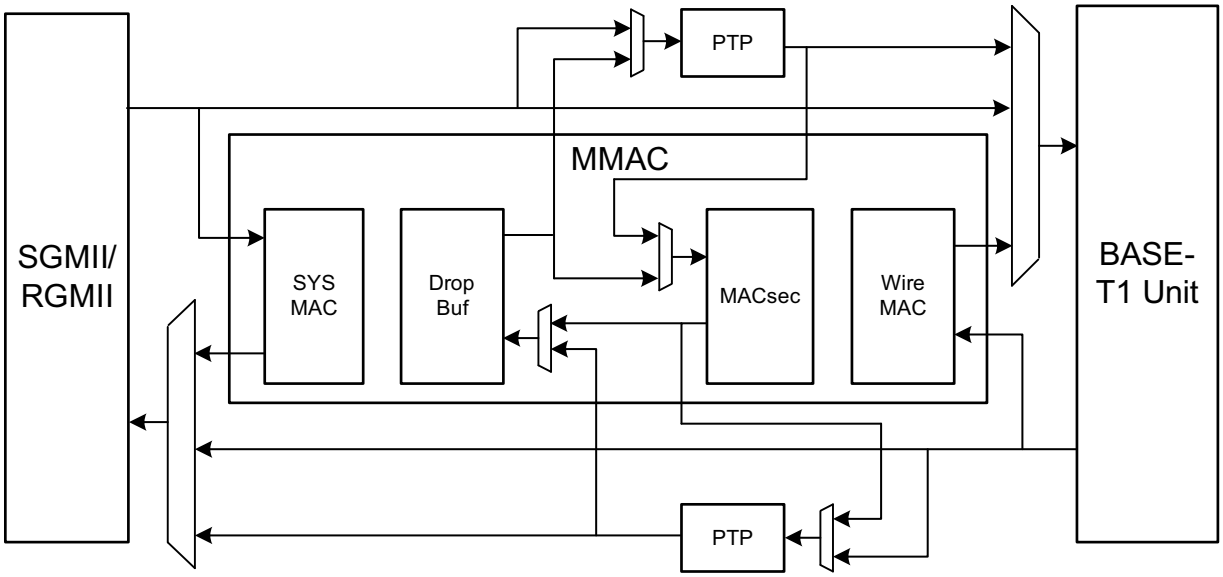
- Support for cipher suites GCM-AES-128, GCM-AES-256, GCM-AES-XPN-128, and GCM-AES-XPN-256
- Full-duplex line-rate bandwidth throughput running at 100M and 1000M for all packet sizes (up to 10 kB – BRIGHTLANE™ 88Q2221/88Q2221M/88Q1201M_RevB, and 2 kB– BRIGHTLANE™ 88Q2221/88Q2221M/88Q1201M_RevA) and transformations.
- Support for Store-forward and Cut-Through Modes
- Support for 4 concurrent Secure Channels with 8 SA (Security Association)
- Adaptive rate control to compensate for packet expansion
- Supports mixed MACsec and non-MACsec traffic
- Flexible parsing engine to parse the MAC DA, SA, Etype, and VLAN support.
- PTP timestamp operation with constant latency in both egress and ingress direction
- Statistics counter support from the MAC and MACsec module in both egress and ingress direction
- Programmable confidentiality offset (0 through 63 bytes).
- Supports Flow Control (802.3x) including Priority-based Flow Control (802.1Qbb)
- Supports and is compliant with IEEE 802.3br Interspersing Express Traffic and preemption
- Supports mixed encryption key sizes 128- and 256-bit for different secure channels
- Protocol checking logic and programmable runt filter to allow MMAC be tolerant to fragments/invalid frames
- Supports Non-disruptive Loopback (NDL) to selectively loopback packets on egress path to ingress path without dropping egress/ingress traffic
- Supports processing of short preamble bytes and regenerating as standard preamble bytes (7B preamble + 1B SFD)
- Programmable hardware key/context rotation assist per secure channel pairs – automatic switching to the next key when the pn is full.
- LPI/Fault Forwarding

The sections that follow describe the overall functionality of the MMAC block.

2.23.2 Data Flow

The MMAC block is located between the SGMII/RGMII logic on the system side which performs the host PCS function and 1000/100BASE-T1-Unit on the wire side which performs the wire PCS function. It is a block that can be optionally turned on when MACsec functionality is required; otherwise, it is completely bypassed. Figure 38 shows a simplified diagram of where the MMAC fits into the top level of the BRIGHTLANE™ 88Q2221/88Q2221M/88Q1201M. The MMAC block also support the option of fully bypassing the PTP block if only MACsec functionality is required and PTP is not required.

Figure 38: MMAC Location in BRIGHTLANE™ 88Q2221/88Q2221M/88Q1201M Data Path



When enabled, the MMAC performs the following functions in the egress (System to wire) directions:

- Transmit System MAC function
- Packet buffering functions
- PTP timestamping
- MACsec Encrypt (egress)/Decrypt (ingress) as well as Authentication
- Receive Wire MAC function

For the ingress (wire to system) direction, the order of the MACsec/PTP/Buffer functions is reversed.

The entire MMAC and PTP module is clocked by the recovered clock from the BASE-T1 unit to avoid asynchronous clock domain cross to introduce latency variation through the data path. In 1G speed, two clocking mode is supported:

- Lower Power Mode (operating MACsec and drop buffer at 1/8 of the clock rate as low latency mode) to reduce the total power consumption. Higher data latency is expected given data being processed at slower rate in MCS
- Low Latency Mode (operating MCS and drop buffer at full clock rate)

In 100M speed, only low latency mode is supported.

The MMAC block encrypts and decrypts incoming packages by passing the data through a MAC to extract the payload, encrypt/decrypt, and then passes into another MAC to form a genuine Ethernet packet again. The MMAC do not post any requirement to incoming traffic to preserve IPG for SecTag insertion for MACsec. It contains a data buffer to handle the required gap management and to avoid buffer overflow inside MMAC, pause frame will be sent to local and remote host to stop traffic when buffer is getting full. So, it is a requirement for local and remote host to support pause frame or host will need to ensure there are enough IPG between packets within the buffer's capacity.

The MMAC fully supports preemption fragments encryption and decryption, besides regular express traffic. No reassembly or fragmentation is performed in the MMAC data path. Packets/Fragments enter and exit the device in FIFO order. Encryption/Decryption context of preemption fragments are stored in between express packets to allow the encryption/decryption to resume when subsequent preemption fragments arrive.

2.23.3 System-side/Wire-side MACs

The system-side/wire-side MACs (SMC/WMC) are IEEE 802.3 Standard compliant MACs that support the IET protocol (802.3br). The MACs interfaces with the external PCSs via parallel XGMII or GMII/MII buses depending on the configured port speed. The role of the MACs and their interface logics in MMAC are as follows:

- CRC checking on receive side
- mCRC checking and generation for non-last preemptive fragments
- Preamble generation/checking/stripping
- Identification of express/preemption traffic
- IPG generation
- Preemption Verify/Respond Frame Handling
- Pause Frame Processing and Generation
- Receive Error indications such as runts, error codes, MII misalignment, CRC errors
- LPI/Fault forwarding
- Packet Padding

2.23.4 Drop Buffer

The drop buffer supports two operation modes, store-and-forward and cut-through. Each buffer (egress and ingress) can have a separate operation mode. The drop buffer can be back-pressured to pause its read out from upstream operation. To avoid overflow, the buffer has programmable on /off thresholds to trigger XON/XOFF frame generation. The operation of flow control is described in more detail in a later section.

- Cut-through: In this mode, packets/fragments are written into the buffer and can be read out immediately if there is no flow control from the upstream blocks. Error information is forwarded to the MAC, and the MAC will transmit error packets with a bad CRC to propagate the error.
- Store and Forward: In this mode, packets/fragments are written into the buffer and will not be read out until the whole packet/fragment is present in the buffer. Additionally, if express packets are marked with an error (due to bad CRC and so on), they will be dropped. The logic drops with a roll-back of the write pointer such that these packets will not be read out or consume buffer resources.
- Additionally, in the egress direction, to enable constant latency of packet from the PTP block to the wire interface, a scheduler can be turned on to ensure there is sufficient gap between packets for the packet expansion due to ICV and SecTag insertion.

2.23.5 MACsec Process

The MMAC supports all possible combinations of packet sequences with virtual port matching classifier for a complete MACsec processing solution. The following are MACsec process features:

- Full SecY processing
- IEEE 802.1AE compliant
- IEEE 802.1AEbn compliant (256-bit key)
- IEEE 802.1AEbw compliant (extended packet numbering)
- All cipher suites are supported: GCM-AES-128/256, GCM-AES-XPN-128/256

Internally, the MACsec Crypto Engine operates on 16-byte blocks, as required by the MACsec (AES-GCM) standard. As for packets or fragments coming into the MACsec block, they do not require multiples of 16-bytes in size. The MCS internally performs the proper alignment onto 16-byte crypto-blocks.

A brief description of the packet flow through the MACsec block in the ingress direction is as follows:

- The incoming packet are parsed to extract a set of fixed and flexible fields to create a lookup classification vector for the classifier. The parser supports for a variety of VLAN and/or Custom tags before the SecTAG and programmable parsing depth. The extracted fields are used to create a lookup key to associate the incoming packet with the correct SA.
- When the packet is successfully associated with a given SA, the resulting policy is used to define the IV, keys, and byte offsets required to successfully decrypt and authenticate the packet. The resulting policy is written into a policy FIFO where it is associated with the incoming packet data. These data are presented to the decryption engine.
- Data not sent to the decryption engine is merged with the decrypted user data to form the final packet. If the ICV authentication check fails, then the packet is marked with an EOP error.
- The MACsec block can also be configured to strip or preserve the incoming SecTAG and ICV fields.
- MACsec statistics are updated.

Packet flow in the egress direction involves very similar processing and handling as the ingress direction except that packets are encrypted and authenticated with a SecTAG and ICV field inserted into the packet.

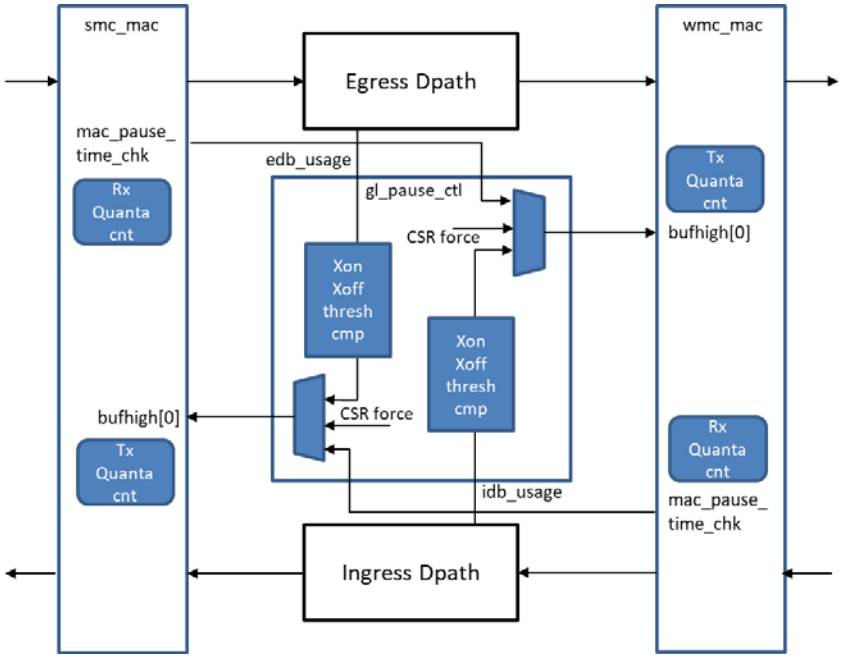
2.23.6 Flow Control

The MMAC offers three modes of operation with regards to pause: Pass-through, Low latency, and Closed loop.

Figure 39 shows the blocks involved to offer these various modes. Smc_mac/wmc_mac in the diagram represent the system/wire MAC, and certain internal signals are shown for illustrative purposes.

2.23.6.1 Pass-though Mode

Figure 39: MMAC Pause Logic

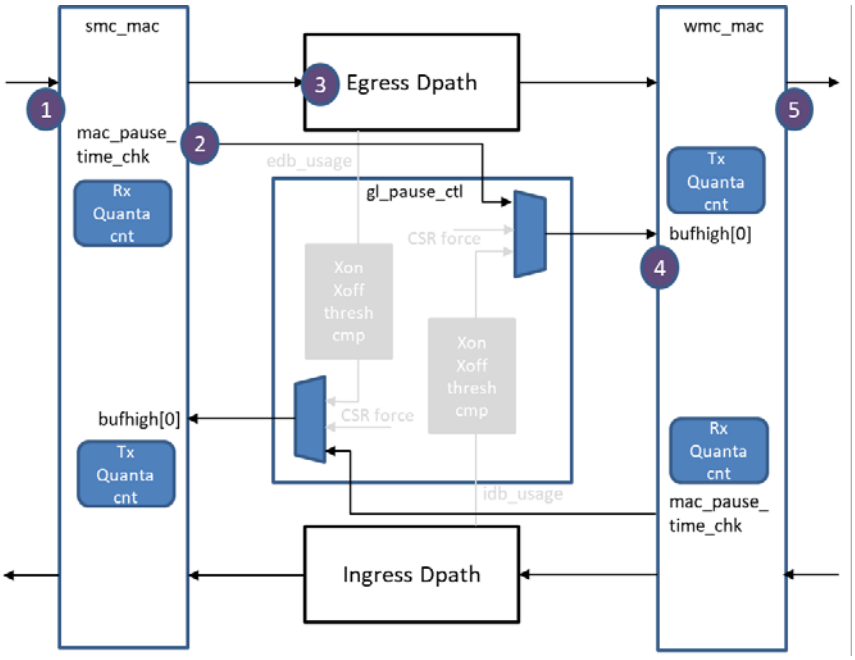


For Pass-through mode, pause frames received on the system side will flow through the egress data path and eventually get sent out of the wire side. The same behavior is present on the ingress side as well.

2.23.6.2 Low Latency Mode

Low latency mode is illustrated in Figure 40.

Figure 40: Low Latency Pause Mode



The following describes the low latency pause control flow from system to wire side. Wire to system side is identical.

Pause XOFF steps are as follows:

- A pause frame with XOFF (non-zero quanta) is received.
- The SMC Rx MAC captures the quanta and holds this mac_pause_time_chk signal level high for the quanta time.
- Egress data path drops the Pause Frame.
- The level is forwarded via the gl_pause_ctl to the bufhigh[0] pin of the WMC MAC.
- WMC MAC sends the pause frame with 0xFFFF quanta and maintains the quanta count.

Pause XON steps are as follows:

- A pause frame with XON (zero quanta) is received.
- The SMC Rx MAC clears the quanta, so the mac_pause_time_chk signal level is driven low.
- Egress data path drops the Pause Frame.
- The level is forwarded via the gl_pause_ctl to the bufhigh[0] pin of the WMC MAC.
- WMC MAC sends the pause frame with 0x0000 quanta and clears this quanta count.

Note

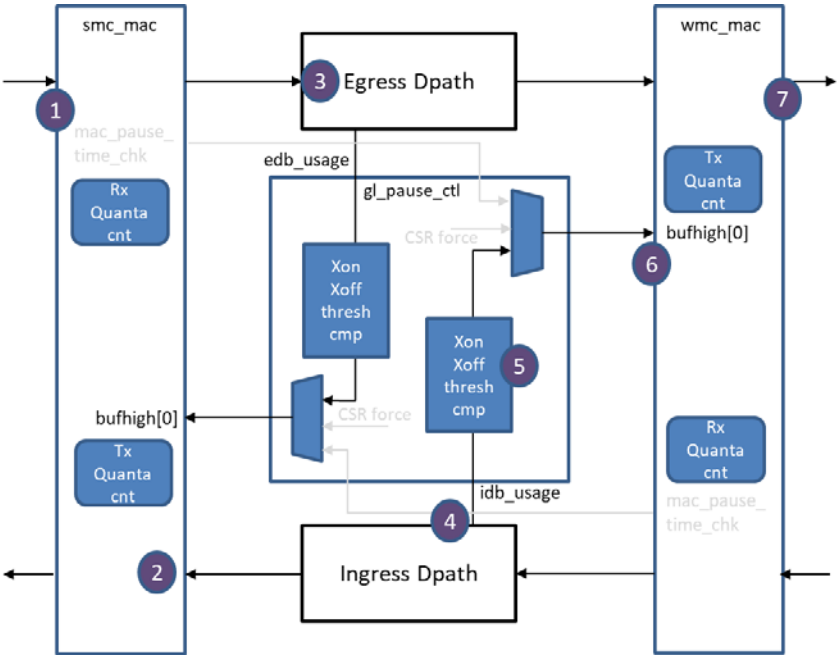
If the WMC quanta counter reaches half of 0xFFFF, then another pause frame with 0xFFFF is sent.

If the SMC Rx Quanta count drops to 0, then it is equivalent to receiving a Pause XON and steps 2 through 5 are performed.

2.23.6.3 Closed Loop Mode

The Closed Loop mode is illustrated in Figure 41.

Figure 41: Closed Loop Pause More



The following describes the pause control flow from system to wire side when in closed loop mode. The wire to system flow is identical.

Pause XOFF steps are as follows:

- A pause frame with XOFF (non-zero quanta) is received.
- The SMC Rx MAC captures the quanta and tells the Tx MAC to not accept any new frames from the Ingress data path for the quanta time.
- Egress data path drops the Pause Frame.
- Ingress drop Buffer (IDB) Fills.
- IDB Usage is compared to programmable XOFF threshold
- If the Buffer usage exceeds the Xoff threshold, then a high level is forwarded to the WMC MAC bufhigh[0] pin
- WMC MAC sends the pause frame with 0xFFFF quanta and maintains the quanta count.

Pause XON steps are as follows:

- A pause frame with XON (zero quanta) is received.
- The SMC Rx MAC clears the quanta and tells the Tx MAC to accept packets from the Ingress data path.
- Egress data path drops the Pause Frame in the smc_pfc_qos block.
- Ingress Drop Buffer Starts to empty.
- IDB usage is compared to a programmable XON threshold.
- If the Buffer usage is smaller than the Xon threshold, then a low level is forwarded to the WMC MAC bufhigh[0] pin.
- WMC MAC sends the pause frame with 0x0000 quanta and clears this quanta count.

Note

If the WMC quanta counter reaches half of 0xFFFF, then another pause frame with 0xFFFF is sent.

If the SMC Rx Quanta count goes to 0, then it is equivalent to receiving a Pause XON and steps 2 through 7 are performed.

2.23.7 MIBS

MIB statistics counters are collected at SMC Rx/Tx (as per Table 77 and Table 78 and WMC Rx/Tx (as per Table 79 and Table 80), while MIB statistics collected by the MACsec block in the Egress and Ingress direction are listed in Table 81 and Table 82.

Table 77: SMC Rx MIB Counters

Counter Name	Description
Good Octets	Good frame octets
Error Octets	Bad frame octets
Jabber	Frame size > MTU with bad CRC
Fragment	Frame size < MTU with bad CRC
Undersize	Frame size < 64B with good CRC
Oversize	Frame size > MTU with good CRC
Rx Error	Rx Error (sequence, symbol error)
CRC Error	CRC Error
Bad FC/Rx Overrun	Bad flow control/Rx overrun
GoodPackets	Good packets
FC packets	Flow control packets
Broadcast	Broadcast packets
Multicast	Multicast packets
InPAssemblyErr	Preempt packet assembly errors

Table 77: SMC Rx MIB Counters (Continued)

Counter Name	Description
InPFrames	Preempt packet counts. Non-fragmented packets are not counted, (for example, a packet with only SMDS). Packets with assembly errors or CRC errors are not counted.
InPFrags	This number of fragments that are received with SMD-C along with a matching from count. SMD-V and SMD-R are also counted here. The first fragment (with SMD-C) is not included.
InPBadFrags	The bad fragments received. A bad fragment is a fragment without a known SMD-X or a start fragment with SMD-C.

Table 78: SMC Tx MIB Counters

Counter Name	Description
Good Octets	Good frame octets
Error Octets	Bad frame octets
Jabber	Frame size > MTU with bad CRC
Fragment	Frame size < MTU with bad CRC
Undersize	Frame size < 64B with good CRC
Oversize	Frame size > MTU with good CRC
Rx Error	N/A
CRC Error/Tx underrun	CRC Error/Tx Underrun
Bad FC	Bad flow control
GoodPackets	Good packets
FC packets	Flow control packets
Broadcast	Broadcast packets
Multicast	Multicast packets
OutPFrags	This is the number of fragments that are transmitted with SMD-C along with a matching from count. SMD-V and SMD-R are also counted here. The first fragment (with SMD-C) is not included.
OutPFrames	Preempt packet counts. Non-fragmented packets are not counted (for example, packets with only SMDS). Packets with assembly errors or CRC errors are not counted.

Table 79: WMC Rx MIB Counters

Counter Name	Description
packets	Total packets
DroppedPkts	Dropped packets; packets are dropped at small packet drop, flow control drops or Drop buffer are not counted here.
Octets	All octets
Jabbers	Frame size > MTU with bad CRC
Fragment	Frame size < MTU with bad CRC
Undersize	Frame size < 64B with good CRC
Rx Error	Rx Error (sequence, symbol error)
CRC Error	CRC Error
FC pkts	Flow control packets
Broadcast	Broadcast packets
Multicast	Multicast packets
Packets with 64 octets	Packet size = 64B
Packets with 65-127 octets	Packet size between 65B and 127B
Packets with 128-255 octets	Packet size between 128B and 255B
Packets with 256-511 octets	Packet size between 256B and 511B
Packets with 512-1023 octets	Packet size between 512B and 1023B
Packets with 1024-1518 octets	Packet size between 1024B and 1518B
Packets with 1519-1522 octets	Packet size between 1519B and 1522B
Packets with 1523-1548 octets	Packet size between 1523B and 1548B
Packets with 1549-2000 octets	Packet size between 1549B and 2000B
Packets with 2001-2500 octets	Packet size between 2001B and 2500B
Packets with 2501-MTU octets	Packet size between 2501B and MTU
Packets with 1549-MTU octets	Packets size between 1549B and MTU
InPAssemblyErr	Preempt packet assembly errors
InPFrames	Preempt packet counts. Non-fragmented packets are not counted, (for example, pkt with only SMDS). Packets with assembly errors or CRC errors are not counted.
InPFrags	This is the number of fragments that are received with SMD-C along with a matching from count. SMD-V and SMD-R are also counted here. The first fragment (with SMD-C) is not included.

Table 79: WMC Rx MIB Counters (Continued)

Counter Name	Description
InPBadFrags	The bad fragments received. A bad fragment is one without a known SMD-X or a start fragment with SMD-C.

Table 80: WMC Tx MIB Counters

Counter Name	Description
packets	Total packets
DroppedPkts	Dropped packets; packets are dropped at small packet drop, flow control drops or Drop buffer are not counted here.
Octets	All octets
Jabbers	Frame size > MTU with bad CRC
Fragment	Frame size < MTU with bad CRC
Undersize	Frame size < 64B with good CRC
Rx Error	N/A
CRC Error/Tx Underrun	CRC Error/Tx underrun
FC Packets	Flow control packets
Broadcast	Broadcast packets
Multicast	Multicast packets
Packets with 64 octets	Packet size = 64B
Packets with 65-127 octets	Packet size between 65B and 127B
Packets with 128-255 octets	Packet size between 128B and 255B
Packets with 256-511 octets	Packet size between 256B and 511B
Packets with 512-1023 octets	Packet size between 512B and 1023B
Packets with 1024-1518 octets	Packet size between 1024B and 1518B
Packets with 1519-1522 octets	Packet size between 1519B and 1522B
Packets with 1523-1548 octets	Packet size between 1523B and 1548B
Packets with 1549-2000 octets	Packet size between 1549B and 2000B
Packets with 2001-2500 octets	Packet size between 2001B and 2500B
Packets with 2501-MTU octets	Packet size between 2501B and MTU
Packets with 1549-MTU octets	Packet size between 1549B and MTU

Table 80: WMC Tx MIB Counters (Continued)

Counter Name	Description
OutPFrags	This is the number of fragments that are transmitted with SMD-C along with a matching from count. SMD-V and SMD-R are also counted here. The first fragment (with SMD-C) is not included.
OutPFrames	Preempt packet counts. Non-fragmented packet are not counted (for example, packets with only SMDS). Packets with assembly errors or CRC errors are not counted.

Table 81: MACsec Egress MIB Counters

Counter Name	Index	Description
ParseError	Port	This counts the total number of parsed error packets per port.
FlowIDHit	Flow-ID	This counts the number of packets which hit an entry in the Flow- ID TCAM. Only one Hit counter increments for each packet.
FlowIDMiss	Port	This counts all Flow-ID TCAM lookups that result in a miss, per port.
IEEE Counter Name	**Index**	**Description**
Egress-controlled Port Statistics (per SecY) provided to support IETF RFC2863 interface MIB counters		
ifOutOctets	SecY	These are the total MSDU and MAC-DA/SA Octets that are received by the Controlled port from the host for this SecY for data packets (control packets are not counted in this counter), (SecY.Controlled_ Port_Enabled must be TRUE). VLAN tags before the SecTAG can be optionally included (global config). SecTAG and ICV bytes are never included.
ifOutUcastPkts	SecY	These are Unicast data packets received by the controlled port for this SecY.
ifOutMulticastPkts	SecY	These are Multicast data packets received by the controlled port for this SecY.
ifOutBroadcastPkts	SecY	These are Broadcast data packets received by the controlled port for this SecY.
ifOutDiscards	0	This is derived from sum(OutPktsNoTag, OutPktsLate, OutPktsOverrun). This is not implemented.

Table 81: MACsec Egress MIB Counters (Continued)

Counter Name	Index	Description
ifOutErrors	0	This is derived from sum(OutPktsBadTag, OutPktsNoSAError, OutPktsNoSA, OutPktsNotValid). This is not implemented.
Egress-uncontrolled Port Statistics (per SecY) provided to support IETF RFC2863 interface MIB counters		
ifOutOctets	SecY	This is all octets from all control packets received by this SecY excluding preamble and FCS octets which are dropped by the MAC (includes padding).
ifOutUcastPkts	SecY	These are Unicast control packets received by this SecY.
ifOutMulticastPkts	SecY	These are Multicast control packets received by this SecY.
ifOutBroadcastPkts	SecY	These are Broadcast control packets received by this SecY.
ifOutDiscards	0	This is not implemented since uncontrolled packets are never dropped.
ifOutErrors	0	This is not implemented since it is equivalent to OutPktsTooLong.
Secure Frame Generation SecY Statistics (secyStatsTx)		
OutPktsUntagged	SecY	This is the number of data packet (excluding control packets) transmitted without a SecTAG because SecY.Protect_Frames is FALSE.
OutPktsTooLong	SecY	This is the number of transmit packets discarded because their length is greater than the configured SecY.MTU after SecTAG/ICV insertion.
OutOctetsProtected	SecY	This is the number of plaintext octets integrity protected, but not encrypted in transmitted frames.
OutOctetsEncrypted	SecY	This is the number of plaintext octets integrity protected and encrypted in transmitted frames.
Secure Frame Generation SC Statistics (secyTxSCStats)		
OutPktsProtected	SC	This is the number of integrity-protected, but not encrypted packets for this transmit SC.
OutPktsEncrypted	SC	This is the number of integrity-protected and encrypted packets for this transmit SC.

Table 82: MACsec Ingress MIB Counters

Counter Name	Index	Description
ParseError	Port	This counts the total number of parsed error packets per port.
FlowIDHit	Flow-ID	This counts the number of packets which hit an entry in the Flow-ID TCAM. Only one Hit counter increments for each packet.
FlowIDMiss	Port	This counts the total number of parsed error packets per port.
SCCamHit	SC	This counts the total number of parsed error packets per port.
IEEE Counter Name	**Index**	**Description**
Ingress-controlled Port Statistics (per SecY) provided to support IETF RFC2863 interface MIB counters		
ifInOctets	SecY	These are the total octets of the MSDU and MAC-DA/SA that are permitted to the Controlled port of this SecY. (SecY.Controlled_ Port_Enabled must be TRUE). VLAN tags before the SecTAG can be optionally included via a global csr bit. SecTAG and ICV bytes are never included.
ifInUcastPkts	SecY	These are Unicast packets sent to the controlled port of this SecY.
ifInMulticastPkts	SecY	These are Multicast packets sent to the controlled port of this SecY.
ifInBroadcastPkts	SecY	These are Broadcast packets sent to the controlled port of this SecY.
ifInDiscards	0	This is derived from sum(InPktsNoTag, InPktsLate, InPktsOverrun). This is not implemented.
ifInErrors	0	This is derived from sum(InPktsBadTag, InPktsNoSAError, InPktsNotValid). This is not implemented.
Ingress-uncontrolled Port Statistics (per SecY) provided to support IETF RFC2863 interface MIB counters		
ifInOctets	SecY	These are all octets from all packets received by this SecY except for preamble and FCS dropped by the MAC (includes padding).

Table 82: MACsec Ingress MIB Counters (Continued)

Counter Name	Index	Description
ifInUcastPkts	SecY	These are Unicast packets received by this SecY.
ifInMulticastPkts	SecY	These are Multicast packets received by this SecY.
ifInBroadcastPkts	SecY	These are Broadcast packets received by this SecY.
ifInDiscards	0	This is not implemented since uncontrolled packets are never dropped.
ifInErrors	0	This is not implemented since there is no error checking on uncontrolled ports.
Secure Frame Validation SecY Statistics (secyStatsRx)		
InCtrlPortDisabled	SecY	This is the number of received packets dropped because the controlled port is disabled.
InPktsUntagged	SecY	This is the number of packets received without a SecTAG when SecY.Validate_Frames is not STRICT.
InPktsNoTag	SecY	This is the number of received packets without a SecTAG discarded because SecY.Validate_ Frames is ‘STRICT’.
InTaggedCtrlPkts	SecY	This is the number of KaY or tagged control packets that are received with the controlled port enabled and SecY.Validate_Frames != NULL.
InPktsBadTag	SecY	This is the number of received packets discarded because of a failing PDU/SecTag compliance check.
InPktsOverrun	0	This counter is not implemented because the AES Engine can sustain the line-rate without backpressure.
InPktsNoSA	SecY	This is the number of received packets with an unknown SCI or for an unused SA.
InPktsNoSAError	SecY	This is the number of packets discarded because the received SCI is unknown or the SA is not in use.
InOctetsValidated	SecY	This is the number of plaintext octets recovered from packets that were integrity protected, but not encrypted.
InOctetsDecrypted	SecY	This is the number of plaintext octets recovered from packets that were integrity protected and encrypted.

Table 82: MACsec Ingress MIB Counters (Continued)

Counter Name	Index	Description
Secure Frame Validation SC Statistics (secyRxSCStats)		
InPktsLate	SC	This is the number of packets discarded, for this SC, because the received PN was lower than the lowest acceptable PN (Ingress_PN_Table.Lowest_PN) when SecY.Replay_Protect is True.
InPktsNotValid	SC	This is the number of packets discarded (by asserting the ‘error’ signal towards the host), for this SC, because validation failed and SecY.Validate_Frames was ‘STRICT’ or the data was encrypted so the original frame could not be recovered.
InPktsInvalid	SC	This is the number of packets, for this SC, that failed validation but could be received because SecY.Validate_Frames was ‘CHECK’ and the data was not encrypted so the original frame could be recovered.
InPktsDelayed	SC	This is the number of received packets, for this SC, with PN lower than the lowest acceptable PN (Ingress_PN_Table.Lowest_PN) and SecY.Replay_Protect false.
InPktsUnchecked	SC	This is the number of packets received for this SC, while SecY.Validate_Frames was ‘disabled’.
InPktsOK	SC	This is the number of packets received for this SC successfully validated and within the replay window.

3 General Registers

Table 83 defines the register types used in the register map.

Table 83: Register Types

Type	Description
LH	Register field with latching high function. If the status is high, then the register is set to 1 and remains set until a read operation is performed through the management interface or a reset occurs.
LL	Register field with latching low function. If the status is low, then the register is cleared to 0 and remains 0 until a read operation is performed through the management interface or a reset occurs.
RES	Reserved. All reserved bits are read as 0 unless otherwise noted. Important to note: reserved registers default values should not be changed by the user.
Retain	The register value is retained after a software reset is executed.
RO	Read only.
ROC	Read only clear. After read, the register field is cleared.
R/W	Read and Write with initial value indicated.
RWC	Read/Write clear on read. All bits are readable and writable. After reset or after the register field is read, the register field is cleared to 0.
SC	Self-Clear. Writing a 1 to this register causes the desired function to be immediately executed, then the register field is automatically cleared to 0 when the function is complete.
Update	This is the value written to the register field does not take effect until a soft reset is executed.
WO	Write only. Reads from this type of register field return undefined data.
NR	Non-Rollover Register

PHY MDIO Register Description

The device supports Clause 45 XMDIO register access protocol. The device also supports Clause 22 MDIO access to registers in Clause 45 XMDIO register space using registers 13 and 14.

The registers in this device are divided into the following sections:

- IEEE PMA/PMD Registers
- Common Control Registers
- IEEE PCS Registers
- IEEE Auto-Negotiation Registers
- 100BASE-T1 Copper Unit Advance PCS Registers
- 1000BASE-T1 Copper Unit Advance PCS Registers
- Copper Unit Advance Auto-Negotiation Registers
- RGMII Registers
- SGMII Registers

3.1 IEEE PMA/PMD Registers

Table 84: IEEE PMA/PMD Registers — Register Map

Register Name	Register Address	Table and Page
PMA/PMD Control Register 1	Device 1, Register 0x0000	Table 85, p. 134
PMA/PMD Device Identifier Register 1	Device 1, Register 0x0002	Table 86, p. 135
PMA/PMD Device Identifier Register 2	Device 1, Register 0x0003	Table 87, p. 135
PMA/PMD Speed Ability Register	Device 1, Register 0x0004	Table 88, p. 135
PMA/PMD Devices In Package Register 1	Device 1, Register 0x0005	Table 89, p. 136
PMA/PMD Devices In Package Register 2	Device 1, Register 0x0006	Table 90, p. 136
PMA/PMD Package Identifier Register 1	Device 1, Register 0x000E	Table 91, p. 137
PMA/PMD Package Identifier Register 2	Device 1, Register 0x000F	Table 92, p. 137
BASE-T1 PMA/PMD Extended Ability Register	Device 1, Register 0x0012	Table 93, p. 137
BASE-T1 PMA/PMD Control Register	Device 1, Register 0x0834	Table 94, p. 137
100BASE-T1 PMA/PMD Test Control Register	Device 1, Register 0x0836	Table 95, p. 138
BASE-T1 Control Register	Device 1, Register 0x0900	Table 96, p. 138
1000BASE-T1 PMA Status Register	Device 1, Register 0x0901	Table 97, p. 138
1000BASE-T1 Training Register	Device 1, Register 0x0902	Table 98, p. 139
1000BASE-T1 Link Partner Training Register	Device 1, Register 0x0903	Table 99, p. 139
1000BASE-T1 Test Mode Control Register	Device 1, Register 0x0904	Table 100, p. 140
MCS_TOP_SLAVE.DBG_MUX_SEL	Device 1F, Register 0x000C	Table 101, p. 142
BBE_SLAVE0.DBG_MUX_SEL	Device 1F, Register 0x018C	Table 102, p. 142
BBE_SLAVE1.DBG_MUX_SEL	Device 1F, Register 0x020C	Table 103, p. 143
SLC_INTR_SET	Device 1F, Register 0x8004	Table 101, p. 140
MEM_ECC_ERR_CNT	Device 1F, Register 0x802E	Table 102, p. 141
MMAC_ALERT_CFG	Device 1F, Register 0x80F8	Table 103, p. 141

Table 85: PMA/PMD Control Register 1
Device 1, Register 0x0000

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reset	R/W, SC	0x1	SC	1 = PMA/PMD reset 0 = Normal operation
14	Reserved	RO	0x0	0x0	Set to 0.
13	Speed Select	RO	0x0	Retain	Bits [6,13] = 10 – Operation at 1000BASE-T1 Bits [6,13] = 01 – Operation at 100BASE-T1
12	Reserved	RO	0x0	0x0	
11	Low Power	R/W	0x0	0x0	1 = Low Power mode 0 = Normal operation
10:7	Reserved	RO	0x0	0x0	Set to 0.

Table 85: PMA/PMD Control Register 1 (Continued)
Device 1, Register 0x0000

Bits	Field	Mode	HW Rst	SW Rst	Description
6	Speed Select	RO	0x1	Retain	Bit 6, bit 13 00 = Reserved 01 = 100 Mbps 10 = 1000 Mbps 11 = Reserved
5:1	Reserved	RO	0x00	0x00	Set to 0.
0	PMA Loopback	R/W	0x0	Retain	1 = Drop link and loop data back in PMA. 0 = Normal operation

Table 86: PMA/PMD Device Identifier Register 1
Device 1, Register 0x0002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x002B	0x002B	The BRIGHTLANE™ OUI is 00:0A:C2. 0000 0000 0000 1010 1100 0010 ^ ^ bit 1.....bit 24 Register 2.[15:0] shows bits 3 to 18 of the OUI. 0000_0000_0010_1011 ^ ^ bit 3.....bit 18

Table 87: PMA/PMD Device Identifier Register 2
Device 1, Register 0x0003

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bit 19:24	RO	0x02	0x02	Organizationally Unique Identifier bits 19:24 00_0010 ^ ^ bit 19...bit 24
9:4	Model Number	RO	0x32	0x32	Set to 110010.
3:0	Revision Number	RO	See Description.	See Description.	This is the revision number. Refer to the Errata and Hardware Release Notes for detailed information.

Table 88: PMA/PMD Speed Ability Register
Device 1, Register 0x0004

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x000	0x000	Set to 000000000.
6	10M Capable	RO	0x0	0x0	1 = PMA/PMD is capable of operating at 10 Mbps.
5	100M Capable	RO	0x0	0x0	1 = PMA/PMD is capable of operating at 100 Mbps.
4	1000M Capable	RO	0x1	0x1	1 = PMA/PMD is capable of operating at 1000 Mbps.

Table 88: PMA/PMD Speed Ability Register (Continued)
Device 1, Register 0x0004

Bits	Field	Mode	HW Rst	SW Rst	Description
3:1	Reserved	RO	0x0	0x0	Set to 000.
0	10G Capable	RO	0x0	0x0	1 = PMA/PMD is capable of operating at 10 Gbps.

Table 89: PMA/PMD Devices In Package Register 1
Device 1, Register 0x0005

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	0x00	Set to 00000000.
7	Auto-Negotiation Present	RO	0x1	0x1	1 = Auto-Negotiation is present in the package. 0 = Auto-Negotiation is not present in the package.
6	Reserved	RO	0x0	0x0	Set to 0.
5	DTE XS Present	RO	0x0	0x0	1 = DTE XS is present in the package. 0 = DTE XS is not present in the package.
4	PHY XS Present	RO	0x0	0x0	1 = PHY XS is present in the package. 0 = PHY XS is not present in the package.
3	PCS Present	RO	0x1	0x1	1 = PCS is present in the package. 0 = PCS is not present in the package.
2	WIS Present	RO	0x0	0x0	1 = WIS is present in the package. 0 = WIS is not present in the package.
1	PMD/PMA Present	RO	0x1	0x1	1 = PMA/PMD is present in the package. 0 = PMA/PMD not present in the package.
0	Clause 22 Registers Present	RO	0x0	0x0	1 = Clause 22 registers are present in the package. 0 = Clause 22 registers are not present in the package.

Table 90: PMA/PMD Devices In Package Register 2
Device 1, Register 0x0006

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Vendor-specific Device 2 Present	RO	0x0	0x0	1 = The vendor-specific device 2 is present. 0 = The vendor-specific device 2 is not present.
14	Vendor-specific Device 1 Present	RO	0x0	0x0	1 = The vendor-specific device 1 is present. 0 = The vendor-specific device 1 is not present.
13:0	Reserved	RO	0x0000	0x0000	Set to 00000000000000.

Table 91: PMA/PMD Package Identifier Register 1 Device 1, Register 0x000E

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x002B	0x002B	The BRIGHTLANE™ OUI is 00:0A:C2. 0000 0000 0000 1010 1100 0010 ^ ^ bit 1.....bit 24 Register 2.[15:0] shows bits 3 to 18 of the OUI. 0000_0000_0010_1011 ^ ^ bit 3.....bit 18

Table 92: PMA/PMD Package Identifier Register 2 Device 1, Register 0x000F

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bit 9:24	RO	0x02	0x02	Organizationally Unique Identifier bits 19:24 00_0010 ^ ^ bit 19...bit 24
9:4	Model Number	RO	0x32	See Description.	This is the same as 1.0003.9:4.
3:0	Revision Number	RO	See Description.	See Description.	This is the same as 1.0003.3:0.

Table 93: BASE-T1 PMA/PMD Extended Ability Register Device 1, Register 0x0012

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	RO	0x0000	0x0000	The value is always 0.
1	1000BASE-T1 Ability	RO	0x1	0x1	1 = PMA/PMD is able to perform 1000BASE-T1. 0 = PMA/PMD is not able to perform 1000BASE-T1.
0	100BASE-T1 Ability	RO	0x1	0x1	1 = PMA/PMD is able to perform 100BASE-T1. 0 = PMA/PMD is not able to perform 100BASE-T1.

Table 94: BASE-T1 PMA/PMD Control Register Device 1, Register 0x0834

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x1	0x1	The value is always 1 and writes are ignored.
14	Master/Slave Config Value	R/W	0x1	Retain	1 = Configure PHY as master. 0 = Configure PHY as slave.
13:4	Reserved	RO	0x000	0x000	Set to 000000000000.
3:0	Type Selection	R/W	Strap	Retain	0000 = 100BASE-T1 0001 = 1000BASE-T1

Table 95: 100BASE-T1 PMA/PMD Test Control Register Device 1, Register 0x0836

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	100BASE-T1 Test Mode Control	R/W	0x0	Retain	11x = Reserved 101 = Test mode 5 100 = Test mode 4 011 = Reserved 010 = Test mode 2 001 = Test mode 1 000 = Normal operation
12:0	Reserved	RO	0x0000	0x0000	Set to 000000000000.

Table 96: BASE-T1 Control Register Device 1, Register 0x0900

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reset	R/W, SC	0x1	0x0	1 = PMA/PMD reset 0 = Normal operation
14	Global PMA Transmit Disable	R/W	0x0	Retain	0 = Enable transmitters. 1 = Disable transmitters.
13:12	Reserved	RO	0x0	0x0	
11	Low Power	R/W	0x0	0x0	1 = Low Power mode 0 = Normal operation
10:0	Reserved	RO	0x000	Retain	

Table 97: 1000BASE-T1 PMA Status Register Device 1, Register 0x0901

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RO	0x0	Retain	Ignore when read.
11	OAM Ability	RO	0x1	Retain	1 = PHY has OAM ability. 0 = PHY does not have OAM ability.
10	EEE Ability	RO	0x1	Retain	1 = PHY has EEE ability. 0 = PHY does not have EEE ability.
9	Receive Fault Ability	RO	0x0	Retain	1 = PMA/PMD has the ability to detect a fault condition on the Rx path. 0 = PMA/PMD does not have the ability to detect a fault condition on the Rx path.
8	Low Power Ability	RO	0x1	Retain	1 = PMA/PMD supports Low Power mode. 0 = PMA/PMD does not support Low Power mode.
7:3	Reserved	RO	0x00	Retain	Ignore when read.
2	Received Polarity	RO	0x0	Retain	1 = Reverse polarity is reversed. 0 = Reverse polarity is not revered.
1	Receive Fault	RO	0x0	Retain	1 = A fault condition is detected. 0 = A fault condition is not detected.

Table 97: 1000BASE-T1 PMA Status Register (Continued)
Device 1, Register 0x0901

Bits	Field	Mode	HW Rst	SW Rst	Description
0	Receive Link Status	RO, LL	0x0	Retain	1 = PMA/PMD receive link is up. 0 = PMA/PMD receive link is down.

Table 98: 1000BASE-T1 Training Register
Device 1, Register 0x0902

Bits	Field	Mode	HW Rst	SW Rst	Description
15:11	Reserved	RO	0x00	Retain	Set to 0s.
10:4	User Field	R/W	0x00	Retain	This is the 7-bit user-defined field.
3:2	Reserved	RO	0x0	Retain	Set to 0s.
1	OAM Advertisement	R/W	0x1	Retain	1 = The OAM ability is advertised to the link partner. 0 = The OAM ability is not advertised to the link partner.
0	EEE Advertisement	R/W	0x0	Retain	1 = The EEE ability is advertised to the link partner. 0 = The EEE ability is not advertised to the link partner.

Table 99: 1000BASE-T1 Link Partner Training Register
Device 1, Register 0x0903

Bits	Field	Mode	HW Rst	SW Rst	Description
15:11	Reserved	RO	0x00	Retain	
10:4	Link Partner User Field	RO	0x00	Retain	This is the 7-bit user-defined field received from the link partner.
3:2	Reserved	RO	0x0	Retain	Set to 0s.
1	OAM Advertisement	RO	0x0	Retain	1 = The link partner OAM ability has advertised to the link partner. 0 = The link partner OAM ability has not advertised to the link partner.
0	EEE Advertisement	R/W	0x0	Retain	1 = The link partner EEE ability has advertised to the link partner. 0 = The link partner EEE ability has not advertised to the link partner.

Table 100: 1000BASE-T1 Test Mode Control Register
Device 1, Register 0x0904

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Test Mode Control	R/W	0x0	Retain	111 = Test mode 7 110 = Test mode 6 101 = Test mode 5 100 = Test mode 4 011 = Reserved 010 = Test mode 2 001 = Test mode 1 000 = Normal operation
12:0	Reserved	RO	0x0	Retain	

Table 101: SLC_INTR_SET
Device 1F, Register 0x8004

Bits	Field	Mode	HW Rst	SW Rst	Description
30:0	SLC_INTR_SET	RO	0x0	0x0	Interrupts for slice, such as statistics. [0] : smc_rx_rx_intr_full [1] : smc_tx_rx_intr_full [2] : wmc_rx_rx_intr_full [3] : wmc_tx_rx_intr_full [4] : smc_rx_rx_intr_almost_full [5] : smc_tx_rx_intr_almost_full [6] : wmc_rx_rx_intr_almost_full [7] : wmc_tx_rx_intr_almost_full [8] : tx_lpi_enabled [9] : rx_lpi_enabled [10] : single-bit detection ECC qualified with rd [11] : double-bit detection ECC qualified with rd [12] : interrupt test (triggered by test_int) [13] : WMC Rx Overflow [14] : WMC Tx Overflow [15] : SMC Rx Overflow [16] : SMC Tx Overflow [17] : Egress PTP Bypass Fifo Full [18] : Ingress PTP Bypass Fifo Full [19] : Egress datapath buffer full [20] : Ingress datapath buffer full [21] : mcs_egr_stall_alert [22] : mcs_igr_stall_alert [23] : smc_rx_long_err_cnt_alert_s [24] : wmc_rx_long_err_cnt_alert_s [25] : smc_rx_short_err_cnt_alert_s [26] : wmc_rx_short_err_cnt_alert_s [27] : wmc_tx_crc_err_cnt_alert_s [28] : smc_rx_crc_err_cnt_alert_s [29] : smc_tx_crc_err_cnt_alert_s [30] : wmc_rx_crc_err_cnt_alert_s

Table 102: MEM_ECC_ERR_CNT
Device 1F, Register 0x802E

Bits	Field	Mode	HW Rst	SW Rst	Description
31:28	MEM_DB_CNT_ THRESH	R/W	0x0	0x0	Global uncorrectable ECC error count threshold = 2^mem_ dbd_cnt_thresh - 1 mem_dbd_error_alert will be triggered if mem_dbd_cnt is greater than this value no mem_dbd_error will be triggered if mem_dbd_cnt_thresh==4'hf
27:16	MEM_DBD_CNT	R/W	0x0	0x0	Counter for detection of uncorrectable ECC errors (by double bit corruption) in ALL mems enabled by test_ram_ mask.
15:12	MEM_SBD_CNT_ THRESH	R/W	0xC	0xC	Global correctable ECC error count threshold = 2^mem_ sbd_cnt_thresh - 1 mem_sbd_error_alert will be triggered if mem_sbd_cnt is greater than this value no mem_sbd_error will be triggered if mem_sbd_cnt_thresh==4'hf
11:0	MEM_SBD_CNT	R/W	0x0	0x0	Counter for correctable ECC errors (by single bit corruption) in ALL mems enabled by test_ram_mask.

Table 103: MMAC_ALERT_CFG
Device 1F, Register 0x80F8

Bits	Field	Mode	HW Rst	SW Rst	Description
31:22	Reserved				
21	MCS_ACTIVITY_ MON_EN	R/W	0x0	0x0	Set 1 to enable the MCS activity monitor for MCS stuck alert.
20:0	Reserved				

3.2 Common Control Registers

Table 104: Common Control Registers — Register Map

Register Name	Register Address	Table and Page
Reset and Control Register	Device 3, Register 0x8000	Table 105, p. 143
Config Register	Device 3, Register 0x8001	Table 106, p. 143
MDIO Broadcast Mode Register	Device 3, Register 0x800C	Table 107, p. 144
Tx Disable Status Register	Device 3, Register 0x8002	Table 108, p. 144
SyncE Control Register	Device 3, Register 0x8004	Table 109, p. 144
Interrupt Enable Register	Device 3, Register 0x8010	Table 110, p. 145
GPIO Interrupt Status Register	Device 3, Register 0x8011	Table 111, p. 146
Common LPSD Control Register 1	Device 3, Register 0x8021	Table 112, p. 146
Common Sleep/Wakeup Configuration	Device 3, Register 0x8027	Table 113, p. 148
LPSD Control Register 2	Device 3, Register 0x802C	Table 114, p. 148
Temperature Sensor Register 1	Device 3, Register 0x8041	Table 115, p. 148
Temperature Sensor Register 2	Device 3, Register 0x8042	Table 116, p. 149
FailSafe Control Register 1	Device 3, Register 0x8051	Table 117, p. 150
FailSafe Control Register 2	Device 3, Register 0x8052	Table 118, p. 150
FailSafe Status Register	Device 3, Register 0x8053	Table 119, p. 150
Remote GPIO Command Register	Device 3, Register 0x8060	Table 120, p. 150
Remote GPIO Status Register	Device 3, Register 0x8061	Table 121, p. 151
Temperature Sensor Register 3	Device 3, Register 0x8043	Table 122, p. 151
Interrupt Enable Register	Device 3, Register 0xFE16	Table 123, p. 152
Interrupt Status Register	Device 3, Register 0xFE17	Table 126, p. 153
TDR Control Register	Device 3, Register 0xFEC3	Table 131, p. 154
TDR Offset Cutoff	Device 3, Register 0xFEDE	Table 132, p. 155
TDR Offset Shortcable	Device 3, Register 0xFED9	Table 133, p. 155
TDR Status	Device 3, Register 0xFEDD	Table 134, p. 155
TDR Offset Longcable	Device 3, Register 0xFEDA	Table 135, p. 155
TDR Reset Register	Device 3, Register 0xFECA	Table 136, p. 156
WOL Interrupt Mask Register	Device 4, Register 0x8212	Table 137, p. 156
WOL Interrupt Status Register	Device 4, Register 0x8213	Table 138, p. 156
I/O Voltage Control Register	Device 4, Register 0x8214	Table 139, p. 156
WOL Control Register	Device 4, Register 0x8215	Table 140, p. 156
WOL Status Register	Device 4, Register 0x8216	Table 141, p. 157
WOL Packet Destination Register 0	Device 4, Register 0x8217	Table 142, p. 157
WOL Packet Destination Register 1	Device 4, Register 0x8218	Table 143, p. 157
WOL Packet Destination Register 2	Device 4, Register 0x8219	Table 144, p. 157
Under Voltage Interrupt Mask Register	Device 4, Register 0x8703	Table 145, p. 158
Under-voltage Detection Config 1	Device 4, Register 0x8700	Table 148, p. 160
Under-voltage Detection Config 2	Device 4, Register 0x8702	Table 149, p. 161
Under Voltage Interrupt Status Register	Device 4, Register 0x8704	Table 150, p. 162

Table 104: Common Control Registers — Register Map (Continued)

Register Name	Register Address	Table and Page
Critical Failure Interrupt Register	Device 4, Register 0x8708	Table 151, p. 162
Critical Failure Interrupt Mask Register	Device 4, Register 0x8709	Table 152, p. 163
Secondary ID Register	Device 4, Register 0x80FF	Table 153, p. 163
PTP Control Register 100BT1	Device 4, Register 0x87F0	Table 154, p. 163
PTP Control Register 1000BT1	Device 4, Register 0x87F1	Table 155, p. 164
LPSD Data Sleep Restore	Device 4, Register 0xFD20	Table 156, p. 165
LPSD Data Sleep Control	Device 4, Register 0xFD21	Table 157, p. 169

Table 105: Reset and Control Register
Device 3, Register 0x8000

Bits	Field	Mode	HW Rst	SW Rst	Description
15	RGMII Software Reset	R/W	0x0	Retain	RGMII Software Reset, not self-clearing 0 = Disable, no reset 1 = Enable, perform a software reset of the T-unit.
14	Reserved	R/W	0x0	Retain	
13	SGMII Software Reset	R/W	0x0	Retain	SGMII Software Reset, not self-clearing 0 = Disable, no reset 1 = Enable, perform a software reset of the T-unit.
12:4	Reserved	R/W	0x000	Retain	
3	Tx Disable Feature Enable	R/W	0x1	Retain	1 = Enable Tx Disable Feature. Tx packets can be stopped by TX_ENABLE pin. 0 = Disable Tx Disable Feature. TX_ENABLE has no effect on Tx packets.
2:0	Reserved	R/W	0x0	Retain	

Table 106: Config Register
Device 3, Register 8001

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RO	0x0	Retain	
11	RGMII/SGMII selection	RO	0x0	Retain	1 = RGMII 0 = SGMII
10	MACsec Capability	RO	0x0	Retain	1 = MACsec is not supported. 0 = MACsec is supported.
9	Master/Slave selection	RO	0x0	Retain	1 = MASTER 0 = SLAVE
8	GIG Selection	RO	0x0	Retain	1 = 1000BT1 0 = 100BT1
7	TC10 Enable	RO	0x0	Retain	0 = TC10 Disable 1 = TC10 Enable

Table 106: Config Register
Device 3, Register 8001

Bits	Field	Mode	HW Rst	SW Rst	Description
6	PASSIVE MODE	RO	0x0	Retain	0 = The device starts in normal mode. 1 = The device starts in Passive mode.
5	Reserved	RO	0x3	Retain	
4:0	PHY Address	RO	0x0	Retain	Device PHY address

Table 107: MDIO Broadcast Mode Register
Device 3, Register 800C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x0	Retain	
6	Enable Broadcast mode	RW	0x0	Retain	1 = Enable Broadcast mode; the device will ignore PHY address during write operation. 0 = Disable Broadcast mode.

Table 108: Tx Disable Status Register
Device 3, Register 0x8002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	RO	0x0000	Retain	
2	VDD09 BUCK Ready	RO	0x0	Retain	1 = Buck is ready. 0 = Buck is not ready.
1	AVDD1.2 LDO Ready	RO	0x1	Retain	1 = 1.2V from LDO is ready. 0 = 1.2V from LDO is not ready.
0	Status of Tx Disable	RO	0x0	Retain	0 = Tx packets are not blocked. 1 = Tx packets are blocked.

Table 109: SyncE Control Register
Device 3, Register 0x8004

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	R/W	0x0000	Retain	
1	SyncE Link Down Disable	R/W	0x0	Retain	This selects what the SyncE clock output is during link down. 1 = SyncE clock is low. 0 = SyncE clock is the local 125 MHz clock.
0	SyncE Clock Enable	R/W	0x0	Retain	1 = Enable SyncE clock to go out on the GPIO pin. 0 = Disable SyncE.

Table 110: Interrupt Enable Register
Device 3, Register 0x8010

Bits	Field	Mode	HW Rst	SW Rst	Description
15	MMAC Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
14	PTP Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
13	100BT1 TC10 Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
12	100BT1 Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
11	Includes Interrupt for Temperature Sensor	R/W	0x0	Retain	0 = Disable 1 = Enable
10:8	Reserved	R/W	0x0	Retain	
7	Link Down Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
6	Link Up Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
5	1000BT1 TC10 Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
4	WOL Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
3	Chip Failure Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
2	Reserved	R/W	0x0	Retain	
1	LED Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable
0	GPIO Interrupt Enable	R/W	0x0	Retain	0 = Disable 1 = Enable

Table 111: GPIO Interrupt Status Register Device 3, Register 0x8011

Bits	Field	Mode	HW Rst	SW Rst	Description
15	MMAC Interrupt Status	RO, LH	0x0	0x0	0 = No interrupt has occurred. 1 = An interrupt has occurred.
14	PTP Interrupt Status	RO, LH	0x0	0x0	0 = No interrupt has occurred. 1 = An interrupt has occurred.
13	100BT1 TC10 Interrupt Status	RO, LH	0x0	0x0	0 = No interrupt has occurred. 1 = An interrupt has occurred.
12	100BT1 General Interrupt Status	RO, LH	0x0	0x0	0 = No interrupt has occurred. 1 = An interrupt has occurred.
11	TEMP Interrupt Status	RO, LH	0x0	0x0	0 = No interrupt has occurred. 1 = An interrupt has occurred.
10:8	Reserved	RO, LH	0x0	0x0	
7	Link Down Interrupt Status	RO, LH	0x0	0x0	Link Down Interrupt Status 0 = No interrupt has occurred. 1 = An interrupt has occurred.
6	Link Up Interrupt Status	RO, LH	0x0	0x0	Link Up Interrupt Status 0 = No interrupt has occurred. 1 = An interrupt has occurred.
5	1000BT1 TC10 Interrupt Status	RO, LH	0x0	0x0	0 = No interrupt has occurred. 1 = An interrupt has occurred.
4	WOL Status	RO, LH	0x0	0x0	0 = No interrupt has occurred. 1 = An interrupt has occurred.
3	Chip Failure Interrupt Status	RO, LH	0x0	0x0	0 = No interrupt has occurred. 1 = An interrupt has occurred.
2	Reserved	RO, LH	0x0	0x0	
1	LED Interrupt Status	RO, LH	0x0	0x0	This bit is not valid unless register 3.8014.3 = 1 and 3.8013.1 = 0. 0 = No interrupt has occurred. 1 = An interrupt has occurred.
0	GPIO Interrupt Status	RO, LH	0x0	0x0	This bit is not valid unless register 3.8013.0 = 0. 0 = No interrupt has occurred. 1 = An interrupt has occurred.

Table 112: Common LPSD Control Register 1 Device 3, Register 0x8021

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Enable LPSD Circuit Programming	R/W, SC	0	Retain	1 = Write digital register values to the LPSD circuit.

Table 112: Common LPSD Control Register 1 (Continued)
Device 3, Register 0x8021

Bits	Field	Mode	HW Rst	SW Rst	Description
14:13	Set WAKE_IN Pulse Width	R/W	0	Retain	This allows for setting the pulse width needed at the WAKE_IN pin to power up the device after an LPSD power down. This is only valid for the following: **NOTE:** After this register bit is programmed, 3.8021.15 must be written to 1 for this register bit to take effect. 00 = Guaranteed No WAKE 10 µs; Guaranteed WAKE 40 µs 01 = Guaranteed No WAKE 320 µs; Guaranteed WAKE 1.28 ms 10 = Guaranteed No WAKE 10.24 ms; Guaranteed WAKE 40.96 ms 11 = Guaranteed No WAKE 20.48 ms; Guaranteed WAKE 81.92 ms
12	Disable LPSD Local Wake Up	R/W	0	Retain	Disable LPSD Local Wake Up after an LPSD power down. **NOTE:** After this register bit is programmed, 3.8021.15 must be written to 1 for this register bit to take effect. 1 = The device will not wake up if a pulse is received at the WAKE_IN pin. 0 = The device will wake up if a pulse is received at the WAKE_IN pin.
11	Disable LPSD Remote Wake Up	R/W	0	Retain	Disable LPSD Remote Wake Up after an LPSD power down. **NOTE:** After this register bit is programmed, 3.8021.15 must be written to 1 for this register bit to take effect. 1 = The device will not wake up if energy is received at the MDIP/N pins. 0 = The device will wake up if energy is received at the MDIP/N pins.
10:8	Reserved	R/W	0	Retain	
7:6	Set WAKE_OUT Pulse Width	R/W	0	Retain	Allows for setting the pulse width needed at the WAKE_OUT pin. This register is only used when 3.802C.14:13 is 2'b01 or 2'b1x. **NOTE:** After this register bit is programmed, 3.8021.15 must be written to 1 for this register bit to take effect. 00 = Min WAKE Pulse 40 µs; Max WAKE Pulse 160 µs 01 = Min WAKE Pulse 640 µs; Max WAKE Pulse 2.56 ms 10 = Min WAKE Pulse 20.48 ms; Max WAKE Pulse 81.92 ms 11 = Min WAKE Pulse 327.68 ms; Max WAKE Pulse 1310.72 ms
5:0	Reserved	R/W	0	Retain	

Table 113: Common Sleep/Wakeup Configuration Device 3, Register 0x8027

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0	Retain	
6	Enable overwriting TC10 from LPSD shift	R/W	0	Retain	1 = LPSD shift value of TC10 is used to enable function. 0 = Strap value selects whether to TC10 enable or whether not to TC10 enable.
5	Enable waking up in T1 port sleep	R/W	0	Retain	1 = Enable wake up in T1 sleep. 0 = Disable wake up in T1 sleep.
4	Reserved	RO	0	Retain	
3	Disable CIC command	R/W	0	Retain	1 = Upon deep sleep once recovered, disable CIC regardless of value of 3.8027[1]. 0 = 3.8027[1] controls CIC state.
1	CIC Command Enable	R/W	See Description.	Retain	At hardware reset, this register field get the default from LPSD shift register. 1 = TC10 Sleep/Wakeup Command to RGMII/SGMII is supported. **NOTE:** This bit will be shifted in to LPSD when enter power down and updated from the value shifted out from LPSD after power up.
0	TC10 Sleep/Wakeup Capability Supported	R/W	See Description.	Retain	At hardware reset, this register field gets the default from the configuration pin. 1 = TC10 Sleep/Wakeup Capability is supported.

Table 114: LPSD Control Register 2 Device 3, Register 0x802C

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	Retain	
14:13	LPSD Sel Wake Out Setting	R/W	0x00	Retain	**NOTE:** After this register bit is programmed, 3.8021.15 must be written to 1 for this register bit to take effect. 00 = No WAKE_OUT function 01 = INH pin as WAKE_OUT function 1x = WAKE_IN pin as both WAKE_IN and WAKE_OUT functions
12:0	Reserved	R/W	0x0	Retain	

Table 115: Temperature Sensor Register 1 Device 3, Register 0x8041

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Average Test Mode	R/W	0x0	Retain	1 = Average over 16 samples 0 = Normal, the number of samples to average over is determined by 3.8042.12:11.
14	Reserved	RO	0x00	Retain	

Table 115: Temperature Sensor Register 1 (Continued)
Device 3, Register 0x8041

Bits	Field	Mode	HW Rst	SW Rst	Description
13:8	Temperature Sensor Offset Value	RW	0x00	Retain	This is the offset value used in the temperature sensor calculation.
7	Temperature Sensor Interrupt Enable	R/W	0x0	Retain	1 = An interrupt is enabled. 0 = An interrupt is disabled.
6	Temperature Sensor Interrupt	RO, LH	0x0	Retain	1 = The temperature has reached the threshold. 0 = The temperature is below the threshold.
5	One Shot Temperature Sample	R/W	0x0	Retain	This bit is valid only when 3.8042.15:14 == 2'b10. 1 = Temperature sense 0 = Idle
4:1	Reserved	RO	xx	xx	
0	Raw Temperature Sensor Interrupt	RO	0x0	Retain	Set to 1'b1 when 3.8043.7:0 >= 3.8043.15:8. Set to 1'b0 when 3.8043.7:0 < 3.4044.15:8. 1 = The temperature has reached the threshold. 0 = The temperature is below the threshold.

Table 116: Temperature Sensor Register 2
Device 3, Register 0x8042

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Temperature Sense Enable	R/W	0x3	Retain	11 = Disable 10 = Use 3.8041.5. 00 = Sample every 1 second. 01 = Use sense rate on 3.8041.10:8.
13	Temperature Sense High Temperature	R/W	0x0	Retain	0 = Disable 1 = High Temperature Measurement Enable
12:11	Temperature Sensor Number of Samples to Average	R/W	0x1	Retain	00 = Average over 2^6 samples 01 = Average over 2^8 samples 10 = Average over 2^10 samples 11 = Average over 2^12 samples This register is ignored when 3.8041.15 = 1.
10:8	Temperature Sensor Sampling Rate	R/W	0x5	Retain	Sampling Rate 000 = 25 µs 001 = 47 µs 010 = 89 µs 011 = 174 µs 100 = 342 µs 101 = 1.36 ms 110 = 5.47 ms 111 = 10.93 ms
7:0	Temperature Sensor Average Reading (8-bit)	RO	xx	xx	Temperature in C = 3.8042.7:0 - 75, that is, for 100°C, the value is 10101111.

Table 117: FailSafe Control Register 1
Device 3, Register 0x8051

Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	Threshold interrupt generation	R/W	0xbe	Retain	Timer starts when the device starts Autonegotiation or SEND_S protocol, if by the time defined by this register do not archive completion of Autonegotiation or SEND_S then assert interrupt Each count corresponds to 5.24 ms, default 996 ms

Table 118: FailSafe Control Register 2
Device 3, Register 0x8052

Bits	Field	Mode	HW Rst	SW Rst	Description
3:0	Link count threshold	R/W	0x4	Retain	Count of link training attempts before Interrupt generated

Table 119: FailSafe Status Register
Device 3, Register 0x8053

Bits	Field	Mode	HW Rst	SW Rst	Description
7:4	Last linkup attempts to reach Link	RO	0	Retain	Count of link training attempts before Interrupt generated; Last time device linked up
3:0	Current linkup attempts to reach Link	RO	0	Retain	Live count of link training attempts before Interrupt generated

Table 120: Remote GPIO Command Register
Device 3, Register 0x8060

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Remote GPIO enable	R/W	0x0	Retain	Enable Remote GPIO Control Feature 0 = Disable 1 = Enable
14:8	Reserved	R/W	0x0	Retain	
7	RGPIO Execute	R/W	0x0	Retain	Set to 1 to execute GPIO Read/Write. When bit 6 is GPIO write, the device will automatically send “GPIO Write Request” to link partner with the GPIO direction and value in bit <5:0>. When bit 6 is GPIO read, the device will automatically send “GPIO Read Request” and updates bit <5:0> with the received GPIO direction and value in the subsequently received “GPIO Read response” OAM message. This bit will automatically clear when GPIO write is ACK’ed by link partner or when GPIO read response is received for an GPIO read request.

Table 120: Remote GPIO Command Register Device 3, Register 0x8060

Bits	Field	Mode	HW Rst	SW Rst	Description
6	Remote GPIO Read/Write Request	R/W	0x0	Retain	0 = Read 1 = Write
5:3	Remote GPIO Direction	R/W	0x0	Retain	0 = Input 1 = Output
2:0	Remote GPIO Value	R/W	0x0	Retain	These fields report the status of GPIO input pins or the value driven onto GPIO output pins.

Table 121: Remote GPIO Status Register Device 3, Register 0x8061

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	Retain	
14	Remote GPIO update	RO	0x0	Retain	LP_GPIO_DIR and LP_GPIO_VAL has been updated. The bit will be set high when GPIO read response is received for an GPIO read request. This bit will be reset to zero once it is read.
13	Remote GPIO Direction	RO	0x0	Retain	0 = Input 1 = Output
10:8	Remote GPIO Value	RO	0x0	Retain	These fields report the status of GPIO input pins or the value driven onto GPIO output pins.
7	Reserved	RO	0x0	Retain	
6	Local GPIO Updated	RO	0x0	Retain	LOC_GPIO_DIR and LOC_GPIO_VAL has been updated. The bit will be set high when “GPIO Write Request” message is received. This bit will be reset to zero once it is read.
5:3	Local GPIO Direction	RO	0x0	Retain	0 = Input 1 = Output
2:0	Local GPIO Value	RO	0x0	Retain	These fields report the status of GPIO input pins or the value driven onto GPIO output pins.

Table 122: Temperature Sensor Register 3 Device 3, Register 0x8043

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Temperature Interrupt Threshold	R/W	0x96	Retain	Temperature in C = 3.8043.15:8 - 75, that is, for 100^{o}C, the value is 10101111. If the temperature in register 3.8043.7:0 is equal or greater than this field, then the Temperature Sensor Interrupt register (3.FE17.8) will be set when the interrupt is enabled (3.FE16.8 = 1'b1).

Table 122: Temperature Sensor Register 3 (Continued)
Device 3, Register 0x8043

Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	Temperature Sensor Instantaneous Reading	RO	0x00	0x00	Instantaneous temperature reading based on sample rate specified in register 3.8042.10:8. Temperature in C = 3.8043.7:0 - 75, that is, for 100°C, the value is 10101111. If the value in this register is equal or greater than register 3.8043.15:8, then the Temperature Sensor Interrupt register (3.FE17.8) will be set when the interrupt is enabled (3.FE16.8 = 1'b1).

Table 123: Interrupt Enable Register
Device 3, Register 0xFE16

Bits	Field	Mode	HW Rst	SW Rst	Description
15:9	Reserved	R/W	0x00	Retain	Reserved
8	Temperature Sensor Interrupt Enable	R/W	0x0	Retain	1 = Enable the interrupt pin to toggle. 0 = The interrupt is disabled.
7:0	Reserved	R/W	0x00	Retain	

Table 124: PCS Interrupt Status Register
Device 3, Register 0xFDFC

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved				
3	PCS Link Drop Receive Interrupt Status	RO	0x0	0x0	Loss of link due to error on received data
2	PCS Link Local/Remote Data Interrupt Status	RO	0x0	0x0	Loss of link due to local/remote data not ready
1	PCS Remote Receiver Status Interrupt Status	RO	0x0	0x0	Loss of link due to remote receiver status
0	PCS Local Receiver Status Interrupt Status	RO	0x0	0x0	Loss of link due to local receiver status

Table 125: PCS Interrupt Mask Register
Device 3, Register 0xFDFD

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved		0x7FF		

Table 125: PCS Interrupt Mask Register (Continued)
Device 3, Register 0xFDFD

Bits	Field	Mode	HW Rst	SW Rst	Description
3	PCS Link Drop Receive Interrupt	R/W	0x1		Loss of link due to error on received data 0 = Turn on Interrupt 1 = Mask interrupt
2	PCS Link Local/Remote Data Interrupt	R/W	0x1		Loss of link due to local/remote data not ready 0 = Turn on Interrupt 1 = Mask interrupt
1	PCS Remote Receiver Status Interrupt	R/W	0x1		Loss of link due to remote receiver status 0 = Turn on Interrupt 1 = Mask interrupt
0	PCS Local Receiver Status Interrupt	R/W	0x1		Loss of link due to local receiver status 0 = Turn on Interrupt 1 = Mask interrupt

Table 126: Interrupt Status Register
Device 3, Register 0xFE17

Bits	Field	Mode	HW Rst	SW Rst	Description
15:9	Reserved	RO	0x00	Retain	
8	Temperature Sensor Reached Threshold	RO, LH	0x0	Retain	Write 1 to clear the status, LH. 1 = The temperature has reached the threshold. 0 = The temperature is below the threshold.
7:0	Reserved	RO, LH	0x00	Retain	

Table 127: Enable PLL Clock Check
Device 3, Register 0xFE93

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved				
1	PLL Check Enable	R/W	0x1	Retain	0 = Enable checking for clock stopped 1 = Disable check
0	PLL Offset Check Enable	R/W	0x1	Retain	0 = Enable checking for clock frequency offset 1 = Disable check

Table 128: Configure Frequency Offset Check PLL
Device 3, Register 0xFE98

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Configure PLL Frequency Offset	R/W	0x2	Retain	9'd256: Report issue if PPM offset 100 ppm or worse
6:0	Reserved				

Table 129: Enable 125 MHz Reference Clock Check
Device 3, Register 0xFE99

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved				
1	125 MHz Clock Ref Check Enable	R/W	0x1	Retain	0 = Enable checking for clock stopped 1 = Disable check
0	125 MHz Clock Ref Freq Offset Check Enable	R/W	0x1	Retain	0 = Enable checking for clock frequency offset 1 = Disable check

Table 130: Configure Frequency Offset Check of 125 MHz Ref Clock
Device 3, Register 0xFEA3

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Configure Count Prescalar Offset	R/W	0x04	Retain	9'd256: Report issue if PPM offset 100 ppm or worse RW
6:0	Reserved				

Table 131: TDR Control Register
Device 3, Register 0xFEC3

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	R/W	0x0	Retain	
11:7	Set Amplitude	R/W	0x1E	Retain	This sets the amplitude of the generated pulse.
6:2	Reserved	R/W	0x0	Retain	
1:0	Set Width of Pulse	R/W	0x3	Retain	This sets the width of the generated pulse.

Table 132: TDR Offset Cutoff
Device 3, Register 0xFEDE

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	R/W	0x0	Retain	
9:0	Window Cutoff	R/W	0xAE	Retain	Cutoff value for long and short cable. Values below programmed value in this register will used offset in 3.FED9 and above this value will use offset in 3.FEDA.

Table 133: TDR Offset Shortcable
Device 3, Register 0xFED9

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	R/W	0x0	Retain	
9:0	Offset Short	R/W	0xEB	Retain	This is the offset value used in calculation of cable length for short cables.

Table 134: TDR Status
Device 3, Register 0xFEDD

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Reserved	RO	0x0	Retain	
13:8	Distance	RO	0x00	Retain	Cable distance in meters
7:4	VCT Status	RO	0x00	Retain	0011 = Short 1110 = Open harness 0111 = Cable OK 1000 = Test in progress 0101 = Nose environment
3:2	Reserved	RO	0x0	Retain	
1:0	TDR Active	RW/SC	2'b01	Retain	01 = TDR OFF 10 = TDR ON Bit 1 is writable; Self clear when test finishes

Table 135: TDR Offset Longcable
Device 3, Register 0xFEDA

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	R/W	0x0	Retain	
9:0	Offset Long	R/W	0x6B	Retain	This is the offset value used in calculation of cable length for long cables.

Table 136: TDR Reset Register
Device 3, Register 0xFECA

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Reserved	R/W	0x0	Retain	
12	TDR Reset	R/W	0x1	Retain	TDR reset. 1 = Keep VCT function in RESET state. 0 = Remove RESET from VCT.
11:0	Reserved	R/W	0xD90	Retain	

Table 137: WOL Interrupt Mask Register
Device 4, Register 0x8212

Bits	Field	Mode	HW Rst	SW Rst	Description
15	WOL Interrupt Enable	RW	0x0	Retain	When set, it indicates WOL interrupt is enabled.
14:0	Reserved	RO	0x0	0x0	

Table 138: WOL Interrupt Status Register
Device 4, Register 0x8213

Bits	Field	Mode	HW Rst	SW Rst	Description
15	WOL Interrupt	RO, SC	0x0	0x0	When set, it indicates WOL interrupt is latched.
14:0	Reserved	RO	0x0	0x0	

Table 139: I/O Voltage Control Register
Device 4, Register 0x8214

Bits	Field	Mode	HW Rst	SW Rst	Description
15	VDDO Level Enable	RW	0x0	Retain	The VDDO supply voltage used when 1.8V is not used. The bit mapping is as follows: 0 = 3.3V 1 = 2.5V This register defaults to 0 (VDDO = 3.3V). If VDDO = 2.5V, then this bit must be programmed to 1.
14:0	Reserved	RO	0x0	0x0	

Table 140: WOL Control Register
Device 4, Register 0x8215

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	
14	Magic Packet Enable	RW	0x0	Retain	1 = Enable magic packet match.
13	Link Change Enable	RW	0x0	Retain	1 = Enable link change detection.
12	Clear Match	RW, SC	0x0	0x0	Set to clear match status.
11:0	Reserved	RO	0x0	0x0	

Table 141: WOL Status Register
Device 4, Register 0x8216

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	
14	Magic Packet Detect	RO	0x0	0x0	When set, a magic packet match is detected.
13	Link Change Detect	RO	0x0	0x0	When set, a link change is detected.
12:0	Reserved	RO	0x0	0x0	

Table 142: WOL Packet Destination Register 0
Device 4, Register 0x8217

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Data 0	RW	0x0	Retain	MAC_DA[47:32] - {bit[7:0], bit[15:8]}

Table 143: WOL Packet Destination Register 1
Device 4, Register 0x8218

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Data 1	RW	0x0	Retain	MAC_DA[31:16] - {bit[23:16], bit[31:24]}

Table 144: WOL Packet Destination Register 2
Device 4, Register 0x8219

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Data 2	RW	0x0	Retain	MAC_DA[15:0] - {bit[39:32], bit[47:40]}

Table 145: Under Voltage Interrupt Mask Register Device 4, Register 0x8703

Bits	Field	Mode	HW Rst	SW Rst	Description
15	DVDD Under Voltage Recover Interrupt Enable	RW	0x0	Retain	When set, enable under voltage cleared interrupt for DVDD.
14	AVDD33 Under Voltage Recover Interrupt Enable	RW	0x0	Retain	When set, enable under voltage cleared interrupt for AVDD33.
13	AVDD UV Under Voltage Recover Interrupt Enable	RW	0x0	Retain	When set, enable under voltage cleared interrupt for AVDD.
12	VDDO UV Under Voltage Recover Interrupt Enable	RW	0x0	Retain	When set, enable under voltage cleared interrupt for VDDO.
11:4	Reserved	RO	0x0	0x0	
3	DVDD Under Voltage Interrupt Enable	RW	0x0	Retain	When set, enable under voltage interrupt for DVDD.
2	AVDD33 Under Voltage Interrupt Enable	RW	0x0	Retain	When set, enable under voltage interrupt for AVDD33.
1	AVDD Under Voltage Interrupt Enable	RW	0x0	Retain	When set, enable under voltage interrupt for AVDD.
0	VDDO Under Voltage Interrupt Enable	RW	0x0	Retain	When set, enable under voltage interrupt for VDDO.

Table 146: PHY Safety Detection Enable Register Device 4, 0x8705

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Reserved				
13	PCS Fail Interrupt Enable	R/W	0x0	Retain	PCS Fail Enable 0 = Disable Interrupt 1 = Enable Interrupt
12:11	Reserved				
10	TC10 Configuration Interrupt Enable	R/W	0x0	Retain	TC10 Configuration incorrect after deep sleep 0 = Disable Interrupt 1 = Enable Interrupt
9	TC10 Correctable Interrupt Enable	R/W	0x0	Retain	TC10 Correctable reported after sleep 0 = Disable Interrupt 1 = Enable Interrupt
8:4	Reserved				

Table 146: PHY Safety Detection Enable Register (Continued)
Device 4, 0x8705

Bits	Field	Mode	HW Rst	SW Rst	Description
3	MMAC Traffic Stuck Interrupt Enable	R/W	0x0	Retain	Data path mmac_traffic_stuck_alert interrupt 0 = Disable Interrupt 1 = Enable Interrupt
2	MMAC Drop Buffer Interrupt Enable	R/W	0x0	Retain	Data Path mmac_dp_buf_full_alert interrupt 0 = Disable Interrupt 1 = Enable Interrupt
1	MMAC Packet Error Interrupt Enable	R/W	0x0	Retain	Data Path mmac_high_pkt_err_alert interrupt 0 = Disable Interrupt 1 = Enable Interrupt
0	MMAC ECC Cause Interrupt Enable	R/W	0x0	Retain	Data Path mmac_mem_ecc_alert interrupt 0 = Disable Interrupt 1 = Enable Interrupt
NOTE: To enable interrupts from the above table the following bits must also be set: - 4.8709[2] - Enable data path/TC10 interrupts from PHY If any of the enabled interrupts in Table XX cause interrupt, then it will be reported in the register defined in Table XX (below).					

Table 147: PHY Safety Detection Status Register
Device 4, 0x8706

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Reserved				
13	PCS Fail Interrupt Status	RO, LH	0x0	0x0	PCS Fail Enable Interrupt 0 = No Interrupt 1 = Interrupt
12:11	Reserved				
10	TC10 Configuration Interrupt Status	RO, LH	0x0	0x0	TC10 Configuration incorrect after deep sleep 0 = No Interrupt 1 = Interrupt
9	TC10 Correctable Interrupt Status	RO, LH	0x0	0x0	TC10 Correctable reported after sleep; Some bits that were correctable were updated 0 = No Interrupt 1 = Interrupt
8:4	Reserved				

Table 147: PHY Safety Detection Status Register (Continued)
Device 4, 0x8706

Bits	Field	Mode	HW Rst	SW Rst	Description
3	MMAC Traffic Stuck Interrupt Status	RO, LH	0x0	0x0	Data path mmac_traffic_stuck_alert interrupt 0 = No Interrupt 1 = Interrupt
2	MMAC Drop Buffer Interrupt Status	RO, LH	0x0	0x0	Data Path mmac_dp_buf_full_alert interrupt 0 = No Interrupt 1 = Interrupt
1	MMAC Packet Error Interrupt Status	RO, LH	0x0	0x0	Data Path mmac_high_pkt_err_alert interrupt 0 = No Interrupt 1 = Interrupt
0	MMAC ECC Cause Interrupt Status	RO, LH	0x0	0x0	Data Path mmac_mem_ecc_alert interrupt 0 = No Interrupt 1 = Interrupt
NOTE: The status for these interrupts will only be cleared by writing a “1” to corresponding bit.					

Table 148: Under-voltage Detection Config 1
Device 4, Register 0x8700

Bits	Field	Mode	HW Rst	SW Rst	Description
12	Reserved	RO	0x0	Retain	Reserved
3	Enable monitor DVDD	R/W	0x0	Retain	1 = Enable monitor of DVDD rail. 0 = Disable monitor.
2	Enable monitor VDD33	R/W	0x0	Retain	1 = Enable monitor of ADVDD rail. 0 = Disable monitor.
1	Enable monitor AVDDL	R/W	0x0	Retain	1 = Enable monitor of ADVDDL rail. 0 = Disable monitor.
0	Enable monitor VDDO	R/W	0x0	Retain	1 = Enable monitor of VDDO rail. 0 = Disable monitor.

Table 149: Under-voltage Detection Config 2
Device 4, Register 0x8702

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Trip Point DVDD	R/W	0x6	Retain	Setting Trip Point[1] (DVDD = 0.75V[2]) 3 = -9.71% 4 = -8.57% 5 = -7.43% 6 = -6.29% 7 = -5.14%
11:7	Trip Point VDD33	R/W	0x6	Retain	Setting Trip Point[1] 3 = -9.71% 4 = -8.57% 5 = -7.43% 6 = -6.29% 7 = -5.14%
7:4	Trip Point AVDD	R/W	0x6	Retain	Setting Trip Point[1] 3 = -9.71% 4 = -8.57% 5 = -7.43% 6 = -6.29% 7 = -5.14%
3:0	Trip Point VDDO	R/W	0x6	Retain	Setting Trip Point[1] 3 = -9.71% 4 = -8.57% 5 = -7.43% 6 = -6.29% 7 = -5.14%

1. Trip Point is based off nominal voltage.
2. 0.75V applies for Rev B0/B1. 0.80V applies for Rev B2.

Table 150: Under Voltage Interrupt Status Register Device 4, Register 0x8704

Bits	Field	Mode	HW Rst	SW Rst	Description
15	DVDD Under Voltage Recover	RO	0x0	0x0	A '1' indicates DVDD rail recovered from a under voltage (UV) event.
14	AVDD33 Under Voltage Recover	RO	0x0	0x0	A '1' indicates AVDD33 rail recovered from a under voltage (UV) event.
13	AVDD Under Voltage Recover	RO	0x0	0x0	A '1' indicates AVDD rail recovered from a under voltage (UV) event.
12	VDDO Under Voltage Recover	RO	0x0	0x0	A '1' indicates VDDO rail recovered from a under voltage (UV) event.
11:4	Reserved	RO	0x0	0x0	
3	DVDD Under Voltage Interrupt	RO	0x0	0x0	Latch High. Clear on hardware reset.
2	AVDD33 Under Voltage Interrupt	RO	0x0	0x0	Latch High. Clear on hardware reset.
1	AVDD Under Voltage Interrupt	RO	0x0	0x0	Latch High. Clear on hardware reset.
0	VDDO Under Voltage Interrupt	RO	0x0	0x0	Latch High. Clear on hardware reset.

Table 151: Critical Failure Interrupt Register Device 4, Register 0x8708

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	0x0	0x0	
3	Under Voltage and Ref Clock Failure Interrupt	RO, LH, WSC	0x0	Retain	1 = Under voltage and REFCLK failure. 0 = No interrupt.
2	PHY Failure Interrupt	RO, LH, WSC	0x0	Retain	1 = Interrupt caused by any PHY block events (3.8706). The enabled block events are either AND or ORed based on 4.8707(6). 0 = No interrupt. 0 = Interrupt disabled.
1	Reference Clock Fail Interrupt	RO, LH, WSC	0x0	Retain	When set, REFCLK indicates failure.
0	Under Voltage Interrupt	RO, LH, WSC	0x0	Retain	This indicates if any of the power domains AVDD/DVDD/AVDD33/VDD0 have caused an Under Voltage interrupt.

Table 152: Critical Failure Interrupt Mask Register Device 4, Register 0x8709

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	0x0	0x0	
3	Under Voltage and Ref Clock Interrupt Enable	RW	0x0	Retain	1 = Under voltage and REFCLK Failure Enable. 0 = Interrupt disabled.
2	PHY Failure Interrupt Enable	RW	0x0	Retain	1 = Interrupt caused by PHY block events (3.8706) Enable. 0 = Interrupt Disabled.
1	Reference Clock Fail Interrupt Enable	RW	0x0	Retain	Set to enable REFCLK failure.
0	Under Voltage Interrupt Enable	RW	0x0	Retain	Set to enable Under Voltage interrupt of any of the power domains.

Table 153: Secondary ID Register Device 4, Register 0x80FF

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	0x0	0x0	
3:0	AUTO_ID	RO	Device dependent	Device dependent	4'b0000: (0) Q2220M PKG RGMII+MSEC 4'b0100: (4) Q2220 PKG RGMII 4'b0001: (1) Q2221M PKG SGMII+MSEC 4'b0101: (5) Q2221 PK SGMII 4'b0011: (3) Q1211M PKG 100BT1 ONLY+SGMII+MSEC 4'b0010: (2) Q1210M PKG 100BT1 ONLY+RGMII+MSEC 4'b0111: (7) Q1211 PKG 100BT1 ONLY+SGMII 4'b0110: (6) Q1210 PKG 100BT1 ONLY+RGMII

Table 154: PTP Control Register 100BT1 Device 4, Register 0x87F0

Bits	Field	Mode	HW Rst	SW Rst	Description
15	PTPTX_SEL_RXDV	RW	0		TX side PTP's SFD selection 100BT1 1 = From TX_EN 0 = From SFD
14	PTPTX_SEL_PREAM	RW	0		TX side PTP's preamble selection 100BT1 1 = Enable detection of preempt-able packets delimiter. 0 = Disable detection of preempt-able packets delimiter.
13	PTPRX_SEL_RXDV	RW	0		RX side PTP's SFD selection 100BT1 1 = From RXDV 0 = From SFD

Table 154: PTP Control Register 100BT1 (Continued)
Device 4, Register 0x87F0

Bits	Field	Mode	HW Rst	SW Rst	Description
12	PTPRX_SEL_PREAM	RW	0		RX side PTP's preamble selection 100BT1 1 = Enable detection of preempt-able packets delimiter. 0 = Disable detection of preempt-able packets delimiter.
11:10	RESERVED	RW	0		Live value for Reserved signal
9	PTP_POWERDOWN	RW	1		1 = PTP is disabled 100BT1 and 1000BT1. 0 = PTP is enabled.
8	RESERVED	RO	0		Live value for Reserved
7:6	PTP_EVENT_IOSEL0	RW	0		100BT1 and 1000BT1 01 = Use LED pin for PTP output trigger pulse. 10 = Use LED pin for PTP One Pulse Per Second (1PPS) output. 11 = Use LED pin for PTP input trigger pulse.
5:4	PTP_EVENT_IOSEL1	RW	0		100BT1 and 1000BT1 01 = Use GPIO pin for PTP output trigger pulse. 10 = Use GPIO pin for PTP for other functions. 11 = Use GPIO pin for PTP input trigger pulse.
3:2	RESERVED	RO	0		Live value for Reserved
1	RESERVED	RO	0		Live value for Reserved
0	ENABLE_PTP_LED	RW	0		100BT1 This is used to bring PTP ptp_tx_led and ptp_rx_led to LED pin.

Table 155: PTP Control Register 1000BT1
Device 4, Register 0x87F1

Bits	Field	Mode	HW Rst	SW Rst	Description
15	PTPTX_SEL_RXDV	RW	0		TX side PTP's SFD selection 1000BT1 1 = From TX_EN 0 = From SFD
14	PTPTX_SEL_PREAM	RW	0		TX side PTP's preamble selection 1000BT1 1 = Enable detection of preempt-able packets delimiter 0 = Disable detection of preempt-able packets delimiter
13	PTPRX_SEL_RXDV	RW	0		RX side PTP's SFD selection 1000BT1 1 = From RXDV 0 = From SFD

Table 155: PTP Control Register 1000BT1 (Continued)
Device 4, Register 0x87F1

Bits	Field	Mode	HW Rst	SW Rst	Description
12	PTPRX_SEL_PREAM	RW	0		RX side PTP's preamble selection 1000BT1 1 = Enable detection of preempt-able packets delimiter 0 = Disable detection of preempt-able packets delimiter
11:1	RESERVED	RO	0		Reserved
0	ENABLE_PTP_LED	RW	0		1000BT1 Used to bring PTP ptp_tx_led and ptp_rx_led to LED pin.

Table 156: LPSD Data Sleep Restore
Device 4, Register 0xFD20

Bit	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	Retain	R/W	0x0	Reserved
14	lwo_en_t1port_wake	Retain	R/W	0x0	• 1 = loc_wake_out will be asserted when lpsd_sdet_dig_p[n-1:0] status is asserted by LPSD to wake the device up from T1 Port Sleep. • 0 = loc_wake_out will not be asserted when lpsd_sdet_dig_p[n-1:0] status is asserted by LPSD to wake the device up from T1 Port Sleep. Note: • This bit will be stored into LPSD when power is removed and restored from LPSD when power is re-applied.
13	Reserved	Retain	R/W	0x0	Reserved
12	lpsd_force_wake_dis	Retain	R/W	0x0	• 1 = Port will not transmit WUP to connected LP when the LPSD_FORCE_WAKE_STAT from LPSD is asserted. • 0 = Port will transmit WUP to connected LP when the LPSD_FORCE_WAKE_STAT from LPSD is asserted. Note: • This bit will be stored into LPSD when power is removed and restored from LPSD when power is re-applied.

Table 156: LPSD Data Sleep Restore (Continued)
Device 4, Register 0xFD20

Bit	Field	Mode	HW Rst	SW Rst	Description
11	wo_en_lpsd_force_wake	Retain	R/W	0x0	• 1 = wake_out will be asserted when LPSD_FORCE_WAKE_STAT status is asserted. • 0 = wake_out will not be asserted when LPSD_FORCE_WAKE_STAT status is asserted. Note: • This bit will be stored into LPSD when power is removed and restored from LPSD when power is re-applied.
10	Reserved	Retain	R/W	0x0	Reserved
9	wo_en_lpsd_loc_wake_in	Retain	R/W	0x0	• 1 = wake_out will be asserted when LPSD_LOCAL_WAKE status is asserted. • 0 = wake_out will not be asserted when LPSD_LOCAL_WAKE status is asserted. Note: • This bit will be stored into LPSD when power is removed and restored from LPSD when power is re-applied.
8	lwo_en_wake_req_in	Retain	R/W	0x0	• 1 = loc_wake_out will be asserted when WAKE_REQ is asserted. • 0 = loc_wake_out will not be asserted when WAKE_REQ is asserted. Note: • This bit will be stored into LPSD when power is removed and restored from LPSD when power is re-applied.
7	lwo_en_wake_fwd_in	Retain	R/W	0x0	If CIC enabled then valid: • 1 = loc_wake_out will be asserted when WAKE_FWD is asserted. • 0 = loc_wake_out will not be asserted when WAKE_FWD is asserted. Note: • This bit will be stored into LPSD when power is removed and restored from LPSD when power is re-applied.
6	lwo_en_lpsd_loc_wake_in	Retain	R/W	0x0	• 1 = loc_wake_out will be asserted when LPSD_LOCAL_WAKE status is asserted • 0 = loc_wake_out will not be asserted when LPSD_LOCAL_WAKE status is asserted. Note: • This bit will be stored into LPSD when power is removed and restored from LPSD when power is re-applied.

Table 156: LPSD Data Sleep Restore (Continued)
Device 4, Register 0xFD20

Bit	Field	Mode	HW Rst	SW Rst	Description
5	lwo_en_lpsd_rem_wake_in	Retain	R/W	0x0	• 1 = loc_wake_out will be asserted when LPSD_REMOTE_WAKE_P[n-1:0] status is asserted • 0 = loc_wake_out will not be asserted when LPSD_REMOTE_WAKE_P[n-1:0] status is asserted. Note: • This bit will be stored into LPSD when power is removed and restored from LPSD when power is re-applied.
4	wo_en_lpsd_loc_wake_raw_in	Retain	R/W	0x0	• 1 = loc_wake_out will be asserted when LPSD_LOCAL_WAKE_RAW status is asserted • 0 = loc_wake_out will not be asserted when LPSD_LOCAL_WAKE_RAW status is asserted. Note: • This bit will be stored into LPSD when power is removed and restored from LPSD when power is re-applied.
3	lwo_en_wur_in	Retain	R/W	0x0	• 1 = loc_wake_out will be asserted when WUR is received. • 0 = loc_wake_out will not be asserted when WUR is received. Note: • This bit will be stored into LPSD when power is removed and restored from LPSD when power is re-applied.
2	wo_en_lpsd_loc_wake_raw_in	Retain	R/W	0x0	• 1 = wake_out will be asserted when LPSD_LOCAL_WAKE_RAW status is asserted. • 0 = wake_out will not be asserted when LPSD_LOCAL_WAKE_RAW status is asserted. Note: • This bit will be stored into LPSD when power is removed and restored from LPSD when power is re-applied.

Table 156: LPSD Data Sleep Restore (Continued)
Device 4, Register 0xFD20

Bit	Field	Mode	HW Rst	SW Rst	Description
1	lpsd_loc_wake_dis_in	Retain	R/W	0x0	Valid WAKE_IN pulse to WUP/WUR Disable (when INH is 0). • 0 = Port will transmit WUP/WUR to connected Link Partner when a valid WAKE_IN pulse is detected (when INH is 0). • 1 = Port will not transmit WUP/WUR to connected Link Partner when a valid WAKE_IN pulse is detected (when INH is 0). Note: • When port is in Sleep, a WUP is transmitted to the connected Link Partner. • When port is powered up, WUR is transmitted to the connected Link Partner after Link Up. • This bit will be stored into LPSD when power is removed and restored from LPSD when power is re-applied.
0	lpsd_loc_wake_raw_dis_in	Retain	R/W	0x0	Valid WAKE_IN pulse to WUP/WUR Disable (when INH is 1). • 0 = Port will transmit WUP/WUR to connected Link Partner when a valid WAKE_IN pulse is detected (when INH is 1). • 1 = Port will not transmit WUP/WUR to connected Link Partner when a valid WAKE_IN pulse is detected (when INH is 1). Note: • When port is in Sleep, a WUP is transmitted to the connected Link Partner. • When port is powered up, WUR is transmitted to the connected Link Partner after Link Up. • This bit will be stored into LPSD when power is removed and restored from LPSD when power is re-applied.

Table 157: LPSD Data Sleep Control
Device 4, Register 0xFD21

Bit	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	Retain	R/W	0x0	Reserved
4	DeepSleep En	Retain	R/W	0x0	Deep Sleep Enable 0 = Disable entry into the Deep Sleep mode. 1 = Enable entry into the Deep Sleep mode when sleep handshake has completed.
3:0	Reserved	Retain	R/W	0x0	Reserved

3.3 IEEE PCS Registers

Table 158: IEEE PCS Registers — Register Map

Register Name	Register Address	Table and Page
PCS Control Register 1	Device 3, Register 0x0000	Table 159, p. 170
PCS Status Register 1	Device 3, Register 0x0001	Table 160, p. 171
PCS Device Identifier Register 1	Device 3, Register 0x0002	Table 161, p. 171
PCS Device Identifier Register 2	Device 3, Register 0x0003	Table 162, p. 171
PCS Devices In Package Register 1	Device 3, Register 0x0005	Table 163, p. 172
PCS Devices In Package Register 2	Device 3, Register 0x0006	Table 164, p. 172
1000BASE-T1 PCS Status Register 1	Device 3, Register 0x0008	Table 165, p. 172
PCS Package Identifier Register 1	Device 3, Register 0x000E	Table 166, p. 173
PCS Package Identifier Register 2	Device 3, Register 0x000F	Table 167, p. 173
1000BASE-T1 PCS Status Register 2	Device 3, Register 0x0021	Table 168, p. 173
PCS Control Register	Device 3, Register 0x0900	Table 169, p. 173
PCS 1000BASE-T1 Status Register 1	Device 3, Register 0x0901	Table 170, p. 174
PCS 1000BASE-T1 Status Register 2	Device 3, Register 0x0902	Table 171, p. 174
OAM Register 0	Device 3, Register 0x0904	Table 172, p. 175
OAM Register 1	Device 3, Register 0x0905	Table 173, p. 175
OAM Register 2	Device 3, Register 0x0906	Table 174, p. 175
OAM Register 3	Device 3, Register 0x0907	Table 175, p. 176
OAM Register 4	Device 3, Register 0x0908	Table 176, p. 176
OAM Register 5	Device 3, Register 0x0909	Table 177, p. 176
OAM Register 6	Device 3, Register 0x090A	Table 178, p. 176
OAM Register 7	Device 3, Register 0x090B	Table 179, p. 177
OAM Register 8	Device 3, Register 0x090C	Table 180, p. 177
OAM Register 9	Device 3, Register 0x090D	Table 181, p. 177

Table 159: PCS Control Register 1
Device 3, Register 0x0000

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Software Reset	R/W, SC	0x1	0x1	This bit will perform a software reset of the copper unit. 1 = Reset 0 = Normal
14	Loopback	R/W	0x0	Retain	1 = Loopback 0 = Normal
13	Speed Select	RO	0x0	0x0	BIT [6,13] = 10 - Operation at 1000BASE-T1 BIT [6,13] = 01 - Operation at 100BASE-T1
12	Reserved	RO	0x0	0x0	Set to 0.
11	Low Power	R/W	0x0	Retain	This bit will power down the copper unit. 1 = Low Power mode 0 = Normal

Table 159: PCS Control Register 1 (Continued)
Device 3, Register 0x0000

Bits	Field	Mode	HW Rst	SW Rst	Description
10:7	Reserved	RO	0x0	0x0	This bit has no effect. Write as 0.
6	Speed Select	RO	0x1	Retain	1 = Gig 0 = Hundred Note: The default value is strapped in from the device pins for devices that support both 100BT1 and 1000BT1.
5:0	Reserved	RO	0x00	0x00	Set to 0.

Table 160: PCS Status Register 1
Device 3, Register 0x0001

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	RO	0x0000	0x0000	Set to 0000.
1	Low Power Ability	RO	0x1	0x1	1 = PCS supports low power mode. 0 = PCS does not support low power mode.
0	Reserved	RO	0x0	0x0	Set to 0.

Table 161: PCS Device Identifier Register 1
Device 3, Register 0x0002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x002B	0x002B	The BRIGHTLANE™ OUI is 00:0A:C2. 0000 0000 0000 1010 1100 0010 ^ ^ bit 1.....bit 24 Register 2.[15:0] shows bits 3 to 18 of the OUI. 0000_0000_0010_1011 ^ ^ bit 3.....bit 18

Table 162: PCS Device Identifier Register 2
Device 3, Register 0x0003

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bit 19:24	RO	0x02	0x02	Organizationally Unique Identifier bits 19:24 00_0010 ^ ^ bit 19...bit 24
9:4	Model Number	RO	0x32	0x32	Set to 110010.
3:0	Revision Number	RO	See Description.	See Description.	This is the revision number. Refer to the Release Note for detailed information.

Table 163: PCS Devices In Package Register 1 Device 3, Register 0x0005

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	0x00	Set to 00000000.
7	Auto-Negotiation Present	RO	0x1	0x1	1 = Auto-Negotiation is present in the package. 0 = Auto-Negotiation is not present in the package.
6	Reserved	RO	0x0	0x0	Set to 0.
5	DTE XS Present	RO	0x0	0x0	1 = DTE XS is present in the package. 0 = DTE XS is not present in the package.
4	PHY XS Present	RO	0x0	0x0	1 = PHY XS is present in the package. 0 = PHY XS is not present in the package.
3	PCS Present	RO	0x1	0x1	1 = PCS is present in the package. 0 = PCS is not present in the package.
2	WIS Present	RO	0x0	0x0	1 = WIS is present in the package. 0 = WIS is not present in the package.
1	PMD/PMA Present	RO	0x1	0x1	1 = PMA/PMD is present in the package. 0 = PMA/PMD is not present in the package.
0	Clause 22 Registers Present	RO	0x0	0x0	1 = Clause 22 registers are present in the package. 0 = Clause 22 registers are not present in the package.

Table 164: PCS Devices In Package Register 2 Device 3, Register 0x0006

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Vendor-specific Device 2 Present	RO	0x0	0x0	1 = The vendor-specific device 2 is present. 0 = The vendor-specific device 2 is not present.
14	Vendor-specific Device 1 Present	RO	0x0	0x0	1 = The vendor-specific device 1 is present. 0 = The vendor-specific device 1 is not present.
13:0	Reserved	RO	0x0000	0x0000	Set to 00000000000000.

Table 165: 1000BASE-T1 PCS Status Register 1 Device 3, Register 0x0008

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Device Present	RO	0x2	0x2	10 = The device is responding to this address.
13:12	Reserved	RO	0x0	0x0	Set to 00.
11	Transmit Fault	RO, LH	0x0	0x0	1 = There is a fault on the Tx path. 0 = There is no fault on the Tx path.
10	Receive Fault	RO, LH	0x0	0x0	1 = There is a fault on the Rx path. 0 = There is no fault on the Rx path.
9:0	Reserved	RO	0x000	0x000	Set to 0000000000.

Table 166: PCS Package Identifier Register 1
Device 3, Register 0x000E

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x002B	0x002B	The BRIGHTLANE™ OUI is 00:0A:C2. 0000 0000 0000 1010 1100 0010 ^ ^ bit 1.....bit 24 Register 2.[15:0] shows bits 3 to 18 of the OUI. 0000_0000_0010_1011 ^ ^ bit 3.....bit 18

Table 167: PCS Package Identifier Register 2
Device 3, Register 0x000F

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bit 9:24	RO	0x02	0x02	Organizationally Unique Identifier bits 19:24 00_0010 ^ ^ bit 19...bit 24
9:4	Model Number	RO	0x32	See Description.	This is the same as 3.0003.9:4.
3:0	Revision Number	RO	See Description.	See Description.	This is the same as 3.0003.3:0.

Table 168: 1000BASE-T1 PCS Status Register 2
Device 3, Register 0x0021

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	Setting 0.
14	Latched High Bit Error Rate	RO, LH	0x0	0x0	1 = PCS has reported a high BER. 0 = PCS has not reported a high BER.
13:8	Reserved	RO	0x00	0x00	Setting 0.
7:0	Errored Blocks Counter	RO	0x00	0x00	Errored Blocks Counter The counter clears on read. The counter will peg at all 1s.

Table 169: PCS Control Register
Device 3, Register 0x0900

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Software Reset	R/W, SC	0x1	0x1	This bit will perform a software reset of the copper unit. 1 = Reset 0 = Normal
14	Loopback	R/W	0x0	Retain	1 = Loopback 0 = Normal
13:0	Reserved	RO	0x0	0x0	

Table 170: PCS 1000BASE-T1 Status Register 1
Device 3, Register 0x0901

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RO	0x0	0x0	
11	Tx LPI Received	RO, LH	0x0	0x0	1 = Tx LPI was received.
10	Rx LPI Received	RO, LH	0x0	0x0	1 = Rx LPI was received.
9	Tx LPI Indication	RO	0x0	0x0	1 = Tx LPI is being received. 0 = No Tx LPI is being received.
8	Rx LPI Indication	RO	0x0	0x0	1 = Rx LPI is being received. 0 = No Rx LPI is being received.
7	Fault	RO	0x0	0x0	1 = There is a fault condition (pcs_tx_fault or pcs_rx_fault). 0 = There is no fault condition.
6:3	Reserved	RO	0x0	0x0	Ignore when read.
2	Link Status	RO, LL	0x0	0x0	1 = The PCS link is up. 0 = The PCS link is down.
1:0	Reserved	RO	0x0	0x0	Ignore when read.

Table 171: PCS 1000BASE-T1 Status Register 2
Device 3, Register 0x0902

Bits	Field	Mode	HW Rst	SW Rst	Description
15:11	Reserved	RO	0x00	0x00	Set to 0000.
10	Receive Link Status	RO	0x0	0x0	1 = The PCS receive link is up. 0 = The PCS receive link is down.
9	PCS High BER	RO	0x0	0x0	1 = The PCS is reporting a high BER. 0 = The PCS is not reporting a high BER.
8	Block Lock	RO	0x0	0x0	1 = The PCS is locked to received blocks. 0 = The PCS is not locked to received blocks.
7	Latched High BER	RO, LH	0x0	0x0	1 = The PCS has reported a high BER. 0 = The PCS has not reported a high BER.
6	Latched Block Lock	RO, LL	0x0	0x0	1 = The PCS has block lock. 0 = The PCS does not have block lock.
5:0	BER Counter	RO, NR	0x00	0x00	This is the BER counter.

Table 172: OAM Register 0
Device 3, Register 0x0904

Bits	Field	Mode	HW Rst	SW Rst	Description
15	OAM Message Valid	RO	0x0	Retain	This bit is used to indicate message data in registers 3.904.11:8, 3.905, 3.906, 3.907, and 3.908 are valid and ready to be loaded. This bit must self clear when registers are loaded by the state machine. 1 = Message data in the registers is valid. 0 = Message data in the registers is not valid.
14	Toggle Value	RO	0x0	Retain	This is the toggle value to be transmitted with the message. This bit is set by the state machine and cannot be overridden by the user.
13	OAM Message Received	RO, LH	0x0	Retain	This bit must self clear on read. 1 = 1000BASE-T1 OAM message is received by the link partner. 0 = 1000BASE-T1 OAM message is not received the by link partner.
12	Receive Message Toggle Value	RO	0x0	Retain	This is the toggle value of the message that was received by the link partner as indicated in 3.904.13.
11:8	Message Number	R/W	0x0	Retain	This is the user-defined message number to send.
7:4	Reserved	RO	0x0	Retain	
3	Ping Received	RO	0x0	Retain	This is the Received Ping Tx value from the latest good 1000BASE-T1 OAM frame received.
2	Ping Transmit	R/W	0x0	Retain	This is the ping value to send to the link partner.
1:0	Local SNR	RO	0x0	Retain	00 = NA 01 = LPI refresh is insufficient to maintain PHY SNR. Request the link partner to exit LPI and send idles (used only when EEE is enabled). 10 = PHY SNR is marginal. 11 = PHY SNR is good.

Table 173: OAM Register 1
Device 3, Register 0x0905

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	OAM Message 1	R/W	0x00	Retain	Message octet 1. LSB transmitted first.
7:0	OAM Message 0	R/W	0x00	Retain	Message octet 0. LSB transmitted first.

Table 174: OAM Register 2
Device 3, Register 0x0906

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	OAM Message 3	R/W	0x00	Retain	Message octet 3. LSB transmitted first.
7:0	OAM Message 2	R/W	0x00	Retain	Message octet 2. LSB transmitted first.

Table 175: OAM Register 3
Device 3, Register 0x0907

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	OAM Message 5	R/W	0x00	Retain	Message octet 5. LSB transmitted first.
7:0	OAM Message 4	R/W	0x00	Retain	Message octet 4. LSB transmitted first.

Table 176: OAM Register 4
Device 3, Register 0x0908

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	OAM Message 7	R/W	0x00	Retain	Message octet 7. LSB transmitted first.
7:0	OAM Message 6	R/W	0x00	Retain	Message octet 6. LSB transmitted first.

Table 177: OAM Register 5
Device 3, Register 0x0909

Bits	Field	Mode	HW Rst	SW Rst	Description
15	LP OAM Message Valid	RO, SC	0x0	Retain	This bit is used to indicate that message data in registers 3.909.11:8, 3.90A, 3.90B, 3.90C, and 3.90D are stored and ready to be read. This bit must self clear when register 3.2317 is read. 1 = Message data in the registers is valid. 0 = Message data in the registers is not valid.
14	Toggle Value	RO	0x0	Retain	This is the toggle value received with the message.
13:12	Reserved	RO	0x0	Retain	
11:8	LP Message Number	RO	0x0	Retain	This is the message number from the link partner.
7:2	Reserved	RO	0x00	Retain	
1:0	Link Partner SNR	RO	0x0	Retain	00 = NA 01 = LPI refresh is insufficient to maintain link partner SNR. The link partner requests the local device to exit LPI and send idles (used only when EEE is enabled). 10 = Link partner SNR is marginal. 11 = Link partner SNR is good.

Table 178: OAM Register 6
Device 3, Register 0x090A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Link OAM Message 1	RO	0x00	0x00	Message octet 1. LSB transmitted first.
7:0	Link OAM Message 0	RO	0x00	0x00	Message octet 0. LSB transmitted first.

Table 179: OAM Register 7
Device 3, Register 0x090B

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Link OAM Message 3	RO	0x00	0x00	Message octet 3. LSB transmitted first.
7:0	Link OAM Message 2	RO	0x00	0x00	Message octet 2. LSB transmitted first.

Table 180: OAM Register 8
Device 3, Register 0x090C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Link OAM Message 5	RO	0x00	0x00	Message octet 5. LSB transmitted first.
7:0	Link OAM Message 4	RO	0x00	0x00	Message octet 4. LSB transmitted first.

Table 181: OAM Register 9
Device 3, Register 0x090D

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Link OAM Message 7	RO	0x00	0x00	Message octet 7. LSB transmitted first.
7:0	Link OAM Message 6	RO	0x00	0x00	Message octet 6. LSB transmitted first.

3.4 IEEE Auto-Negotiation Registers

Table 182: IEEE Auto-Negotiation Registers — Register Map

Register Name	Register Address	Table and Page
Auto-Negotiation Device Identifier Register 1	Device 7, Register 0x0002	Table 183, p. 178
Auto-Negotiation Device Identifier Register 2	Device 7, Register 0x0003	Table 184, p. 179
Auto-Negotiation Devices In Package Register 1	Device 7, Register 0x0005	Table 185, p. 179
Auto-Negotiation Devices In Package Register 2	Device 7, Register 0x0006	Table 186, p. 179
Auto-Negotiation Package Identifier Register 1	Device 7, Register 0x000E	Table 187, p. 180
Auto-Negotiation Package Identifier Register 2	Device 7, Register 0x000F	Table 188, p. 180
BASE-T1 Auto-Negotiation Control Register	Device 7, Register 0x0200	Table 189, p. 180
BASE-T1 Auto-Negotiation Status Register	Device 7, Register 0x0201	Table 190, p. 181
Auto-Negotiation Advertisement Register 1	Device 7, Register 0x0202	Table 191, p. 181
Auto-Negotiation Advertisement Register 2	Device 7, Register 0x0203	Table 192, p. 182
Auto-Negotiation Advertisement Register 3	Device 7, Register 0x0204	Table 193, p. 182
Link Partner Base Page Ability Register 1	Device 7, Register 0x0205	Table 194, p. 183
Link Partner Base Page Ability Register 2	Device 7, Register 0x0206	Table 195, p. 183
Link Partner Base Page Ability Register 3	Device 7, Register 0x0207	Table 196, p. 183
Next Page Transmit/Extended Next Page Transmit Register	Device 7, Register 0x0208	Table 197, p. 183
Extended Next Page Transmit Unformatted Code Field U0 to U15 Register	Device 7, Register 0x0209	Table 198, p. 184
Extended Next Page Transmit Unformatted Code Field U16 to U31 Register	Device 7, Register 0x020A	Table 199, p. 184
Link Partner Next Page/Link Partner Extended Next Page Ability Register	Device 7, Register 0x020B	Table 200, p. 184
Link Partner Extended Next Page Ability Unformatted Code Field U0 to U15 Register	Device 7, Register 0x020C	Table 201, p. 185
Link Partner Extended Next Page Ability Unformatted Code Field U16 to U31 Register	Device 7, Register 0x020D	Table 202, p. 185

Table 183: Auto-Negotiation Device Identifier Register 1
Device 7, Register 0x0002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x002B	0x002B	The BRIGHTLANE™ OUI is 00:0A:C2. 0000 0000 0000 1010 1100 0010 ^ ^ bit 1.....bit 24 Register 2.[15:0] shows bits 3 to 18 of the OUI. 0000_0000_0010_1011 ^ ^ bit 3.....bit 18

Table 184: Auto-Negotiation Device Identifier Register 2 Device 7, Register 0x0003

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bit 19:24	RO	0x02	0x02	Organizationally Unique Identifier bits 19:24 00_0010 ^ ^ bit 19...bit 24
9:4	Model Number	RO	0x32	0x32	Set to 110010.
3:0	Revision Number	RO	See Description.	See Description.	This is the revision number. Refer to the Release Notes for detailed information.

Table 185: Auto-Negotiation Devices In Package Register 1 Device 7, Register 0x0005

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	0x00	Set to 0000000000.
7	Auto-Negotiation Present	RO	0x1	0x1	1 = Auto-Negotiation is present in the package. 0 = Auto-Negotiation is not present in the package.
6	Reserved	RO	0x0	0x0	Set to 0.
5	DTE XS Present	RO	0x0	0x0	1 = DTE XS is present in the package. 0 = DTE XS is not present in package.
4	PHY XS Present	RO	0x0	0x0	1 = PHY XS is present in the package. 0 = PHY XS is not present in the package.
3	PCS Present	RO	0x1	0x1	1 = PCS is present in the package. 0 = PCS is not present in the package.
2	WIS Present	RO	0x0	0x0	1 = WIS is present in the package. 0 = WIS is not present in the package.
1	PMD/PMA Present	RO	0x1	0x1	1 = PMA/PMD is present in the package. 0 = PMA/PMD is not present in the package.
0	Clause 22 Registers Present	RO	0x0	0x0	1 = Clause 22 registers are present in the package. 0 = Clause 22 registers are not present in the package.

Table 186: Auto-Negotiation Devices In Package Register 2 Device 7, Register 0x0006

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Vendor-specific Device 2 Present	RO	0X0	0X0	1 = The vendor-specific device 2 is present. 0 = A vendor-specific device 2 is not present.
14	Vendor-specific Device 1 Present	RO	0X0	0X0	1 = The vendor-specific device 1 is present. 0 = The vendor-specific device 1 is not present.
13:0	Reserved	RO	0x0000	0x0000	Set to 00000000000000.

Table 187: Auto-Negotiation Package Identifier Register 1
Device 7, Register 0x000E

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x002B	0x002B	The BRIGHTLANE™ OUI is 00:0A:C2. 0000 0000 0000 1010 1100 0010 ^ ^ bit 1.....bit 24 Register 2.[15:0] shows bits 3 to 18 of the OUI. 0000_0000_0010_1011 ^ ^ bit 3.....bit 18

Table 188: Auto-Negotiation Package Identifier Register 2
Device 7, Register 0x000F

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Organizationally Unique Identifier Bit 9:24	RO	0x02	0x02	Organizationally Unique Identifier bits 19:24 00_0010 ^ ^ bit 19...bit 24
9:4	Model Number	RO	0x32	0x32	This is the same as 7.0003.9:4.
3:0	Revision Number	RO	See Description.	See Description.	This is the same as 7.0003.3:0.

Table 189: BASE-T1 Auto-Negotiation Control Register
Device 7, Register 0x0200

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reset	R/W, SC	0x1	0x1	This bit will perform a software reset of the T-unit. 1 = Reset 0 = Normal
14:13	Reserved	RO	0x0	Retain	
12	Auto-Negotiation Enable	R/W	0x0	Retain	A change in this bit will cause Auto-Negotiation to restart. 1 = Enable the Auto-Negotiation process. 0 = Disable the Auto-Negotiation process.
11:10	Reserved	RO	0x0	Retain	
9	Restart Auto-Negotiation	R/W, SC	0x0	0x0	Setting this bit will cause Auto-Negotiation to restart. 1 = Restart the Auto-Negotiation process. 0 = Normal operation
8:0	Reserved	RO	0x000	0x000	

Table 190: BASE-T1 Auto-Negotiation Status Register Device 7, Register 0x0201

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x000	0x000	
6	Page Received	RO, LH	0x0	0x0	This bit is set when a new link code word has been received and is stored in registers 7.0019, 7.001A, and 7.001B if extended next pages are used, and in register 7.0019 if regular next pages are used. 1 = A new page has been received. 0 = A new page has not been received.
5	Auto-Negotiation Complete	RO	0x0	0x0	1 = The Auto-Negotiation process is complete. 0 = The Auto-Negotiation process is not complete.
4	Remote Fault	RO, LH	0x0	0x0	1 = A remote fault condition has been detected. 0 = A remote fault condition has not been detected.
3	Auto-Negotiation Ability	RO	0x1	0x1	1 = The PHY is able to perform Auto-Negotiation. 0 = The PHY is not able to perform Auto-Negotiation.
2	Link Status	RO, LL	0x0	0x0	This bit indicates whether link status was down since the last read. For the current link status, read this register back-to-back. 1 = The link is up. 0 = The link is down.
1:0	Reserved	RO	0x0	0x0	

Table 191: Auto-Negotiation Advertisement Register 1 Device 7, Register 0x0202

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	Retain	If 1000BASE-T1 is advertised or extended next page is advertised and enabled, then the required next pages are automatically transmitted. Register 7.0010.15 must be set to 0 if no additional next pages are needed. 1 = Advertise 0 = Not advertised
14	Acknowledge	RO	0x0	0x0	The value is always 0, writes are ignored.
13	Remote Fault	R/W	0x0	Retain	1 = Set the remote fault bit. 0 = Do not set the remote fault bit.
12	Enable Device in Force Mode During Auto-Negotiation	R/W	0x0	Retain	1 = Force master. 0 = Slave
11:10	Pause	R/W	0x0	Retain	This is used to advertise Pause capability; capability is not related to the PHY.
9:5	Echoed Nonce Field	R/W	0x00	Retain	
4:0	Selector Field	R/W	0x01	Retain	This is the selector field mode. 00001 = 802.3

Note

A write to register 7.202.15:0 does not take effect until any of the following occurs:

- There is a software reset (register 1.0000.15, 3.0000.15, 7.0200.15, or any other software reset).
- A low power (register 1.0000.11, 3.0000.11, or any other low power) transitions from low power down to normal operation.
- A Restart Auto-Negotiation is asserted (register 7.0200.9).
- Auto-Negotiation Enable toggles (register 7.0200.12).

Table 192: Auto-Negotiation Advertisement Register 2 Device 7, Register 0x0203

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Technology Ability Field	R/W	0x0	Retain	Set to 0s.
7	Advertise 1000BT1	R/W	0x1	Retain	1 = The device advertises 1000BT1. 0 = The device does not advertise 1000BT1.
6	Reserved	R/W	0x0	Retain	
5	Advertise 100BT1	R/W	0x1	Retain	1 = The device advertises 100BT1. 0 = The device does not advertise 100BT1.
4	Prefer Master	R/W	Strap	Retain	0 = Prefer Slave. 1 = Prefer Master.
3:0	Transmitted Nonce Field	R/W	0x0	Retain	Set to 0s.

Note

This register is the same as 7.0202.

Table 193: Auto-Negotiation Advertisement Register 3 Device 7, Register 0x0204

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Technology Ability Field	R/W	0x0000	Retain	Set to 0s.

Note

This register is the same as 7.0202.

Table 194: Link Partner Base Page Ability Register 1 Device 7, Register 0x0205

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Received Code Word bit 15 1 = The link partner is capable of next page. 0 = The link partner is not capable of next page.
14	Acknowledge	RO	0x0	0x0	Received Code Word bit 14 1 = The link partner received a link code word.
13	Remote Fault	RO	0x0	0x0	Received Code Word bit 13 1 = The link partner has detected a remote fault. 0 = The link partner has not detected a remote fault.
12	Force Master/Slave	RO	0x0	0x0	Received Code Word bit 12 1 = The link partner will force the master.
11:10	Pause	RO	0x0	0x0	Received Code Word bit 11 1 = The link partner requests an asymmetric pause. 0 = The link partner does not request an asymmetric pause.
9:5	Echoed Nonce Field	RO	0x00	0x00	This is the link partner Echoed Nonce field.
4:0	Selector Field	RO	0x00	0x00	This is the link partner Selector field.

Table 195: Link Partner Base Page Ability Register 2 Device 7, Register 0x0206

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Technology Ability Field	RO	0x000	Retain	This is the link partner Technology field.
4:0	Transmitted Nonce Field	RO	0x00	Retain	This is the link partner Echoed Nonce field.

Table 196: Link Partner Base Page Ability Register 3 Device 7, Register 0x0207

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Technology Ability Field	RO	0x0000	Retain	This is the link partner Technology Ability field.

Table 197: Next Page Transmit/Extended Next Page Transmit Register Device 7, Register 0x0208

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	0x0	Transmit Code Word bit 15
14	Reserved	RO	0x0	0x0	Transmit Code Word bit 14
13	Message Page Mode	R/W	0x1	0x1	Transmit Code Word bit 13
12	Acknowledge 2	R/W	0x0	0x0	Transmit Code Word bit 12
11	Toggle	RO	0x0	0x0	Transmit Code Word bit 11

Table 197: Next Page Transmit/Extended Next Page Transmit Register (Continued) Device 7, Register 0x0208

Bits	Field	Mode	HW Rst	SW Rst	Description
10:0	Message/ Unformatted Field	R/W	0x001	0x001	Transmit Code Word bits [10:0]

Note

A write to register 7.0208 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded.
This register is used for regular next page exchange and extended next page exchange.
A link fail will clear register 7.0208.

Table 198: Extended Next Page Transmit Unformatted Code Field U0 to U15 Register Device 7, Register 0x0209

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Unformatted Field	R/W	0x0000	0x0000	U15 to U0

Note

A write to register 7.0208 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded, so register 7.0209 must be written before register 7.0208 is written.
This register is used for extended next page exchange and is not used for regular next page exchange.
A link fail will clear register 7.0209.

Table 199: Extended Next Page Transmit Unformatted Code Field U16 to U31 Register Device 7, Register 0x020A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Unformatted Field	R/W	0x0000	0x0000	U31 to U16

Note

A write to register 7.0208 implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded, so register 7.020A must be written before register 7.0208 is written.
This register is used for extended next page exchange and is not used for regular next page exchange.
A link fail will clear register 7.020A.

Table 200: Link Partner Next Page/Link Partner Extended Next Page Ability Register Device 7, Register 0x020B

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	Receive Code Word bit 15
14	Acknowledge	RO	0x0	0x0	Receive Code Word bit 14
13	Message Page	RO	0x0	0x0	Receive Code Word bit 13
12	Acknowledge 2	RO	0x0	0x0	Receive Code Word bit 12

Table 200: Link Partner Next Page/Link Partner Extended Next Page Ability Register (Continued) Device 7, Register 0x020B

Bits	Field	Mode	HW Rst	SW Rst	Description
11	Toggle	RO	0x0	0x0	Receive Code Word bit 11
10:0	Message/Unformatted Field	RO	0x000	0x000	Receive Code Word bits [10:0]

Note
This register is used for regular next page exchange and extended next page exchange.
A link fail will clear register 7.020B.

Table 201: Link Partner Extended Next Page Ability Unformatted Code Field U0 to U15 Register Device 7, Register 0x020C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Unformatted Field	RO	0x0000	0x0000	U15 to U0

Note
This register is used for extended next page exchange and is not used for regular next page exchange.
A link fail will clear register 7.020C.

Table 202: Link Partner Extended Next Page Ability Unformatted Code Field U16 to U31 Register Device 7, Register 0x020D

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Unformatted Field	RO	0x0000	0x0000	U31 to U16

Note
This register is used for extended next page exchange and is not used for regular next page exchange.
A link fail will clear register 7.020D.

3.5 100BASE-T1 Copper Unit Advance PCS Registers

Table 203: 100BASE-T1 Copper Unit Advance PCS Registers — Register Map

Register Name	Register Address	Table and Page
100BASE-T1 Copper Control Register	Device 3, Register 0x8100	Table 204, p. 187
100BASE-T1 Status Register	Device 3, Register 0x8108	Table 205, p. 188
100BASE-T1 Status Register	Device 3, Register 0x8109	Table 206, p. 188
PHY Status	Device 3, Register 0x810A	Table 207, p. 189
PHY REM/LOC Counters	Device 3, Register 0x810B	Table 208, p. 189
100BASE-T1 Specific Interrupt Enable Register	Device 3, Register 0x8112	Table 209, p. 189
Copper Interrupt Status Register	Device 3, Register 0x8113	Table 210, p. 190
Interrupt Status Register	Device 3, Register 0x8117	Table 211, p. 190
Link Drop Counter Register	Device 3, Register 0x8120	Table 212, p. 191
MAC Specific Control Register	Device 3, Register 0x8210	Table 213, p. 191
MAC Specific Interrupt Enable Register	Device 3, Register 0x8212	Table 214, p. 191
MAC Specific Status Register	Device 3, Register 0x8213	Table 215, p. 191
Tx FIFO Overflow/Underflow Counter Register	Device 3, Register 0x8214	Table 216, p. 192
Counter Control Register	Device 3, Register 0x8220	Table 217, p. 192
Bad Link Counter Register	Device 3, Register 0x8221	Table 218, p. 192
Bad SSD Counter Register	Device 3, Register 0x8222	Table 219, p. 193
Bad ESD Counter Register	Device 3, Register 0x8223	Table 220, p. 193
Rx Error Counter Register	Device 3, Register 0x8224	Table 221, p. 193
Receiver Status Register	Device 3, Register 0x8230	Table 222, p. 194
Link Training Time	Device 3, Register 0x8231	Table 223, p. 194
Local Receiver Time	Device 3, Register 0x8232	Table 224, p. 195
Remote Receiver Time	Device 3, Register 0x8233	Table 225, p. 195
Link Failures and Losses	Device 3, Register 0x8234	Table 226, p. 195
Communication Ready Status	Device 3, Register 0x8235	Table 227, p. 196
Mean Square Error	Device 3, Register 0x8236	Table 228, p. 196
Worst Case Mean Square Error	Device 3, Register 0x8237	Table 229, p. 196
Peak Mean Square Error	Device 3, Register 0x8238	Table 230, p. 196
DCQ MSE Enable	Device 3, Register 0x8239	Table 231, p. 197
Interrupt Enable Register	Device 3, Register 0x8300	Table 232, p. 197
Interrupt Status Register	Device 3, Register 0x8301	Table 233, p. 197
GPIO/TX_ENABLE Control Register	Device 3, Register 0x8302	Table 234, p. 198
GPIO/TX_ENABLE Control Register	Device 3, Register 0x8303	Table 235, p. 198
GPIO/TX_ENABLE Control Register	Device 3, Register 0x8304	Table 236, p. 198
GPIO/LED Control Register	Device 3, Register 0x8305	Table 237, p. 199
LED Function Control Register	Device 3, Register 0x8310	Table 238, p. 199
LED Polarity Control Register	Device 3, Register 0x8311	Table 239, p. 200
LED Timer/INTn Control Register	Device 3, Register 0x8312	Table 240, p. 201
Copper Port Packet Generation Register	Device 3, Register 0x8610	Table 241, p. 202

Table 203: 100BASE-T1 Copper Unit Advance PCS Registers — Register Map (Continued)

Register Name	Register Address	Table and Page
Copper Port Packet Size Register	Device 3, Register 0x8611	Table 242, p. 202
Checker Control Register	Device 3, Register 0x8612	Table 243, p. 202
Packet Generator Control Register	Device 3, Register 0x8613	Table 244, p. 203
Copper Port Packet Counter Register	Device 3, Register 0x8614	Table 245, p. 203
Copper Port CRC Counter Register	Device 3, Register 0x8615	Table 246, p. 203
100BASE-T1 LPSD Status Register	Device 3, Register 0x8700	Table 247, p. 203
100BASE-T1 Sleep/Wake Request	Device 3, Register 0x8702	Table 248, p. 204
100BASE-T1 Sleep Status	Device 3, Register 0x8703	Table 249, p. 205
100BASE-T1 Wakeup Status	Device 3, Register 0x8704	Table 250, p. 205
100BASE-T1 Sleep/Wakeup Interrupt Status	Device 3, Register 0x8705	Table 251, p. 205
100BASE-T1 Sleep/Wakeup Interrupt Enable	Device 3, Register 0x8706	Table 252, p. 206
100BT1 Sleep/Wakeup Interrupt Status 2	Device 3, Register 0x870A	Table 253, p. 206
100BT1 Sleep/Wakeup Interrupt Enable 2	Device 3, Register 0x870B	Table 254, p. 207

Table 204: 100BASE-T1 Copper Control Register
Device 3, Register 0x8100

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	R/W	0x0	Retain	
14	Copper Line Loopback	R/W	0x0	0x0	1 = Enable the loopback of MDI to MDI. 0 = Normal operation
13:10	Reserved	R/W	0x0	Retain	
9	PCS Automatic Polarity Detection and Correction	R/W	0x0	Retain	When this bit is a 1 and the PCS is slave, the PCS Rx will detect the polarity, and correct the Rx polarity if a polarity swap is observed. In addition, it will also reverse the polarity on the Tx. The detected Rx polarity status is shown in 3.8109.1.
8:2	Reserved	R/W	0x00	Retain	
1	Tx Polarity Reversal Enable	R/W	0x0	Retain	1 = Tx PCS polarity is reversed. 0 = Tx PCS polarity is not reversed.
0	Disable Jabber	R/W	0x0	Retain	1 = Disable the jabber function. 0 = Enable the jabber function.

Table 205: 100BASE-T1 Status Register Device 3, Register 0x8108

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	
14	Master/Slave Configuration Resolution	RO	0x0	0x0	1 = The local PHY configuration is resolved to the master. 0 = The local PHY configuration is resolved to the slave.
13	Local Receiver Status	RO	0x0	0x0	1 = The local receiver is OK. 0 = The local receiver is not OK.
12	Remote Receiver Status	RO	0x0	0x0	1 = The remote receiver is OK. 0 = The remote receiver is not OK.
11:10	Reserved	RO	Always 0x0	Always 0x0	
9	Copper Link Status	RO, LL	0x0	0x0	This register bit indicates when link was down since the last read. For the current link status, either read this register back-to-back or read register 3.8109.2 (Copper Link Real Time). 1 = The link is up. 0 = The link is down.
8	Jabber Detect	RO, LH	0x0	0x0	1 = A jabber condition is detected. 0 = A jabber condition is not detected.
7:0	Idle Error Count	RO, ROC	0x00	Retain	Idle Error Counter These bits report the idle error count since the last time this register was read. The counter pegs at 11111111 and will not roll over.

Table 206: 100BASE-T1 Status Register Device 3, Register 0x8109

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	R/W	0x0	Retain	
3	Auto-Negotiation Resolved	RO	0x0	0x0	1 = The Auto-Negotiation is resolved. 0 = The Auto-Negotiation is not resolved.
2	Copper Link (Real Time)	RO	0x0	0x0	1 = The link is up. 0 = The link is down.
1	Polarity (Real Time)	RO	0x0	0x0	1 = Reversed 0 = Normal This bit is only valid when 3.8100.9 is 1.
0	Jabber (Real Time)	RO	0x0	0x0	1 = Jabber 0 = No jabber

Table 207: PHY Status
Device 3, Register 0x810A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Idle Error	RO, ROC	0x0	Retain	Idle Error Counter This register reports the idle error count since the last time the register was read. The counter pegs at 0xFF and does not roll over.
7	DSP SNR Margin OK	RO	0x0	Retain	1 = OK
6	Descrambler/Polarity/ Alignment Status	RO	0x0	Retain	1= OK
5	Scrambler Status (to PHY CTRL)	RO	0x0	Retain	1 = OK (only valid for Master)
4	Polarity (Real Time)	RO	0x0	Retain	1 = The polarity swapped.
3	PHY_CTRL in SEND_N State	RO	0x0	Retain	1 = PHY_CTRL in SEND_N state
2	Link Status (Real Time)	RO	0x0	Retain	1 = The link OK.
1	Remote Receiver Status	RO	0x0	Retain	1 = OK
0	Local Receiver Status	RO	0x0	Retain	1 = OK

Table 208: PHY REM/LOC Counters
Device 3, Register 0x810B

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Remote Receiver Not OK Counter	RO, ROC	0x0	Retain	This register reports the number of times the REM_RCVR_ STATUS was NOT_OK since the last time the register was read. The counter pegs at 0xFF and does not roll over.
7:0	Local Receiver Not OK Counter	RO, ROC	0x0	Retain	This register reports the number of times the LOC_RCVR_ STATUS was NOT_OK since the last time the register was read. The counter pegs at 0xFF and does not roll over.

Table 209: 100BASE-T1 Specific Interrupt Enable Register
Device 3, Register 0x8112

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	R/W	0x0	Retain	
11	Auto-Negotiation Completed Interrupt Enable	R/W	0x0	Retain	1 = An interrupt is enabled. 0 = An interrupt is disabled.
10	Link Status Changed Interrupt Enable	R/W	0x0	Retain	1 = An interrupt is enabled. 0 = An interrupt is disabled.
9	Symbol Error Interrupt Enable	R/W	0x0	Retain	1 = An interrupt is enabled. 0 = An interrupt is disabled.

Table 209: 100BASE-T1 Specific Interrupt Enable Register (Continued)
Device 3, Register 0x8112

Bits	Field	Mode	HW Rst	SW Rst	Description
8	False Carrier Interrupt Enable	R/W	0x0	Retain	1 = An interrupt is enabled. 0 = An interrupt is disabled.
7:2	Reserved	R/W	0x0	Retain	
1	Polarity Changed Interrupt Enable	R/W	0x0	Retain	1 = An interrupt is enabled. 0 = An interrupt is disabled.
0	Jabber Interrupt Enable	R/W	0x0	Retain	1 = An interrupt is enabled. 0 = An interrupt is disabled.

Table 210: Copper Interrupt Status Register
Device 3, Register 0x8113

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	RO	0x0	0x0	
11	Copper Auto-Negotiation Completed Interrupt Enable	RO, LH	0x0	Retain	1 = An interrupt is enabled. 0 = An interrupt is disabled.
10	Copper Link Status Changed	RO, LH	0x0	0x0	1 = The link status has changed. 0 = The link status has not changed.
9	Copper Symbol Error	RO, LH	0x0	0x0	1 = There is a symbol error. 0 = There is no symbol error.
8	Copper False Carrier	RO, LH	0x0	0x0	1 = There is a false carrier. 0 = There is no false carrier.
7:2	Reserved	RO	0x0	0x0	
1	Polarity Changed	RO, LH	0x0	0x0	1 = The polarity has changed. 0 = The polarity has not changed.
0	Jabber	RO, LH	0x0	0x0	1 = Jabber 0 = No jabber

Table 211: Interrupt Status Register
Device 3, Register 0x8117

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	RO	0x0000	0x0000	Reserved
0	Port Interrupt	RO	0x0	0x0	This bit indicates the 100BASE-T1 port interrupt status. 1 = An interrupt is active on the 100BASE-T1 port. 0 = No interrupt is active on the 100BASE-T1 port.

Table 212: Link Drop Counter Register Device 3, Register 0x8120

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x0	Retain	
7:0	Link Drop Counter	RO, ROC	0x00	Retain	This counter increments every time the link transitions from up to down. The counter saturates at 0xFF (maximum value) and is cleared when read.

Table 213: MAC Specific Control Register Device 3, Register 0x8210

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Copper Tx FIFO Depth	R/W	0x1	Retain	00 = This supports 2 KB at ±100 ppm. 01 = This supports 10 KB at ±100 ppm. 10 = This supports 18 KB at ±100 ppm. 11 = This supports 27 KB at ±100 ppm.
13:0	Reserved	R/W	0x00	Retain	

Table 214: MAC Specific Interrupt Enable Register Device 3, Register 0x8212

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	
7	FIFO Over/Underflow Interrupt Enable	R/W	0x0	Retain	1 = The interrupt is enabled. 0 = The interrupt is disabled.
6:4	Reserved	R/W	0x0	Retain	
3	FIFO Idle Inserted Interrupt Enable	R/W	0x0	Retain	1 = The interrupt is enabled. 0 = The interrupt is disabled.
2	FIFO Idle Deleted Interrupt Enable	R/W	0x0	Retain	1 = The interrupt is enabled. 0 = The interrupt is disabled.
1:0	Reserved	R/W	0x0	Retain	

Table 215: MAC Specific Status Register Device 3, Register 0x8213

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	Always 0x00	Always 0x00	
7	FIFO Over/Underflow	RO, LH	0x0	0x0	1 = There is an overflow/underflow error 0 = There is no FIFO error.
6:4	Reserved	RO	Always 0x0	Always 0x0	
3	FIFO Idle Inserted	RO, LH	0x0	0x0	1 = Idle is inserted. 0 = No idle is inserted.

Table 215: MAC Specific Status Register (Continued)
Device 3, Register 0x8213

Bits	Field	Mode	HW Rst	SW Rst	Description
2	FIFO Idle Deleted	RO, LH	0x0	0x0	1 = Idle is deleted. 0 = Idle is not deleted.
1:0	Reserved	RO	Always 0x0	Always 0x0	

Table 216: Tx FIFO Overflow/Underflow Counter Register
Device 3, Register 0x8214

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Tx FIFO Over/Underflow Counter	RO, ROC	0x0000	Retain	This is a 16-bit counter for Tx FIFO overflow/underflow error. The counter saturates at 0xFFFF (maximum value) and will clear on read.

Table 217: Counter Control Register
Device 3, Register 0x8220

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	R/W	0x0	Retain	
1	Bad Link/SDD/ESD Counter Control	R/W	0x0	Retain	This controls the counters in registers 3.8221 to 3.8223. 1 = The counters count the number of cycles. 0 = The counters count the number of events.
0	Rx Error Counter Control	R/W	0x0	Retain	This controls the counters in register 3.8224. 1 = The counters count the number of cycles. 0 = The counters count the number of events.

Table 218: Bad Link Counter Register
Device 3, Register 0x8221

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Bad Link Counter	RO, ROC	0x00	Retain	If register 3.8220.1 = 1, then it counts each cycle of RX_ER assertion in the LINK FAILED state. If register 3.8220.1 = 0, then it counts each event of RX_ER assertion in the LINK FAILED state. The counter saturates at 16'hFFFF (maximum value) and will clear on read.

Table 219: Bad SSD Counter Register Device 3, Register 0x8222

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Bad SSD Counter	RO, ROC	0x00	Retain	Start of stream delimiter (SSD) When 3.8220 = 1, the counter is counting the number of RX_CLK cycle that RX_ER is asserted high while inside one of the listed state. When 3.8220 = 0, the counter is counting the number of distinct time RX_ER is asserted high while inside one of the listed state. (it only increase if Rx_ER is drop to 0, then back to 1). The counter saturates at 16'hFFFF (maximum value) and will clear on read.

Table 220: Bad ESD Counter Register Device 3, Register 0x8223

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Bad ESD Counter	RO, ROC	0x00	Retain	End of stream delimiter (ESD) If register 3.8220.1 = 1, then it counts each cycle of RX_ER assertion in the BAD ESD2, BAD END, and Rx ERROR states. If register 3.8220.1 = 0, then it counts each event of RX_ER assertion in the BAD ESD2, BAD END, and Rx ERROR states. The counter saturates at 16'hFFFF (maximum value) and will clear on read.

Table 221: Rx Error Counter Register Device 3, Register 0x8224

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Rx Error Counter	RO, ROC	0x00	Retain	If register 3.8220.0 = 1, then it counts each cycle of RX_ER assertion in the 25 MHz domain. If register 3.8220.0 = 0, then it counts each event of RX_ER assertion in the 25 MHz domain. The counter saturates at 16'hFFFF (maximum value) and will clear on read.

Table 222: Receiver Status Register Device 3, Register 0x8230

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	SQI Level	RO, ROC	0x0	0x0	This is the Signal Quality Index (SQI). The SQI level is listed from 0 to 7 in accordance with the ascending signal quality. The SQI level is reported as 0 during the link up process and if there is no link up.
12	Reserved	RO, ROC	0x0	0x0	
11:9	Lowest SQI Level	RO	0x00	0x0	This register records the lowest SQI value recorded since the last read of this register.
8:6	Reserved	RO, ROC	0x00	0x00	
5	Link Status	RO, ROC	0x0	0x0	1 = The link status is OK.
4	Remote Receiver Status	RO, ROC	0x0	0x0	1 = The remote receiver status is OK.
3	Local Receiver Status	RO, ROC	0x0	0x0	1 = The local receiver status is OK.
2	Polarity Done Status	RO, ROC	0x0	0x0	1 = The polarity is done.
1	Alignment Done Status	RO, ROC	0x0	0x0	1 = The alignment is done.
0	Descrambler Lock Status	RO, ROC	0x0	0x0	1 = The descrambler is locked.

Table 223: Link Training Time Device 3, Register 0x8231

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	Retain	
7:0	Link Training Time	RO	0x00	Retain	Information about the Link Training time of the last link training (loc_rcvr_status AND rem_rcvr_status) 0x00 = 0 ms 0x01 = 1 ms .. 0x64 = 100 ms .. 0xFA = 250 ms 0xFB = More than 250 ms .. = N/A 0xFF = Measurement not possible

Table 224: Local Receiver Time
Device 3, Register 0x8232

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	Retain	
7:0	Local Receiver Time	RO	0x00	Retain	Time until loc_receiver = OK 0x00 = 0 ms 0x01 = 1 ms .. 0x64 = 100 ms .. 0xFA = 250 ms 0xFB = more than 250 ms .. = N/A 0xFF = Measurement not possible

Table 225: Remote Receiver Time
Device 3, Register 0x8233

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x00	Retain	
7:0	Remote Receiver Time	RO	0x00	Retain	Time until remote_receiver = OK 0x00 = 0 ms 0x01 = 1 ms .. 0x64 = 100 ms .. 0xFA = 250 ms 0xFB = more than 250 ms .. = N/A 0xFF = Measurement not possible

Table 226: Link Failures and Losses
Device 3, Register 0x8234

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Link Losses	RO	0x00	Retain	This is the number of link losses occurred since last power cycle (0…63).
9:0	Link Failures	RO	0x00	Retain	This is the number of link failures causing NOT a link loss (SSD failure, ESD failure, and so on) since last power cycle (0…1023) 0x000 = 0 failure 0x001 = 1 failure … 0x3FE = 1022 failures 0x3FF = 1023 or more failures occurred

Table 227: Communication Ready Status
Device 3, Register 0x8235

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	RO	0x00	Retain	
0	Communication Ready Status	RO	0x0	Retain	Information on communication_ready 0 = Communication_ready is NOT_OK/FALSE. 1 = Communication_ready is OK_TRUE.

Table 228: Mean Square Error
Device 3, Register 0x8236

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	RO	0x00	Retain	
9	Mean Square Error Value Valid	RO	0x1	Retain	1 = Invalid 0 = Valid
8:0	Mean Square Error Value	RO	0x00	Retain	0x000 = MSE = 0 0x001 = MSE = 1 … 0x1FE = MSE = 510 0x1FF = MSE = 511

Table 229: Worst Case Mean Square Error
Device 3, Register 0x8237

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	RO	0x00	Retain	
9	Worst Case Mean Square Error Value Valid	RO	0x1	Retain	1 = Invalid 0 = Valid
8:0	Worst Case Mean Square Error Value	RO	0x00	Retain	0x000 = MSE = 0 0x001 = MSE = 1 … 0x1FE = MSE = 510 0x1FF = MSE = 511

Table 230: Peak Mean Square Error
Device 3, Register 0x8238

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Worst Case Peak Mean Square Error Value Since Last Read	RO	0xff	Retain	0x00 = peakMSE = 0 0x01 = peakMSE = 1 … 0x3E = peakMSE = 62 0x3F = peakMSE = 63 0x4E - 0xFE = Value invalid 0xFF = Measurement is not possible.

Table 230: Peak Mean Square Error
Device 3, Register 0x8238

Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	Current Peak Mean Square Error Value	RO	0x00	Retain	0x00 = peakMSE = 0 0x01 = peakMSE = 1 … 0x3E = peakMSE = 62 0x3F = peakMSE = 63 0x4E - 0xFE = Value invalid 0xFF = Measurement is not possible.

Table 231: DCQ MSE Enable
Device 3, Register 0x8239

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	R/W	0x00	Retain	
0	DCQ MSE Enable	R/W	0	Retain	1 = Enable DCQ MSE.

Table 232: Interrupt Enable Register
Device 3, Register 0x8300

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	R/W	0x000	Retain	
1	TX_ENABLE Interrupt Enable	R/W	0x0	Retain	1 = Enable
0	GPIO Interrupt Enable	R/W	0x0	Retain	1 = Enable

Table 233: Interrupt Status Register
Device 3, Register 0x8301

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	RO, LH	0x000	0x000	
1	TX_ENABLE Interrupt Status	RO, LH	0x0	0x0	0 = No interrupt has occurred. 1 = An interrupt has occurred.
0	GPIO Interrupt Status	RO, LH	0x0	0x0	0 = No interrupt has occurred. 1 = An interrupt has occurred.

Table 234: GPIO/TX_ENABLE Control Register Device 3, Register 0x8302

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	R/W	0x0000	Retain	
1	TX_ENABLE Data	R/W	0x0	Retain	This bit has no effect unless register 3.8304.3 = 1. When 3.8303.1 = 0, a read to this register will reflect the state of the TX_ENABLE pin and a write will write the output register, but have no effect on the TX_ENABLE pin. When 3.8303.1 = 1, a read to this register will reflect the state of the output register and a write will write the output register and drive the state of the TX_ENABLE pin.
0	GPIO Data	R/W	0x0	Retain	This bit has no effect unless register 3.8304.11 = 1. When 3.8303.0 = 0, a read to this register will reflect the state of the GPIO pin and a write will write the output register, but have no effect on the GPIO pin. When 3.8303.0 = 1, a read to this register will reflect the state of the output register and a write will write the output register and drive the state of the GPIO pin.

Table 235: GPIO/TX_ENABLE Control Register Device 3, Register 0x8303

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	R/W	0x0000	Retain	
1	TX_ENABLE Pin Output Enable	R/W	0x1	Retain	This bit has no effect unless register 3.8304.3 = 1. 0 = Input 1 = Output
0	GPIO Pin Output Enable	R/W	0x1	Retain	This bit has no effect unless register 3.8304.11 = 1. 0 = Input 1 = Output

Table 236: GPIO/TX_ENABLE Control Register Device 3, Register 0x8304

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	R/W	0x0	Retain	
11	GPIO Pin Function	R/W	0x0	Retain	GPIO Pin Function 0 = GPIO is used for an LED function. 1 = GPIO is used for a GPIO function.
10:8	GPIO Interrupt Select	R/W	0x0	Retain	The interrupt is effective only when 3.8303.0 = 0. 000 = No interrupt 001 = Reserved 010 = Interrupt on low level 011 = Interrupt on high level 100 = Interrupt on high to low 101 = Interrupt on low to high 110 = Reserved 111 = Interrupt on low to high or high to low

Table 236: GPIO/TX_ENABLE Control Register (Continued)
Device 3, Register 0x8304

Bits	Field	Mode	HW Rst	SW Rst	Description
7:4	Reserved	R/W	0x0	Retain	
3	TX_ENABLE Pin Function	R/W	0x0	Retain	This is the TX_ENABLE Pin Function. 0 = TX_ENABLE pin is used for an LED function. 1 = TX_ENABLE pin is used for a GPIO function.
2:0	TX_ENABLE Interrupt Select	R/W	0x0	Retain	The interrupt is effective only when 3.8303.1 = 0. 000 = No interrupt 001 = Reserved 010 = Interrupt on low level 011 = Interrupt on high level 100 = Interrupt on high to low 101 = Interrupt on low to high 110 = Reserved 111 = Interrupt on low to high or high to low

Table 237: GPIO/LED Control Register
Device 3, Register 0x8305

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	R/W	0x0	Retain	
1	TX_ENABLE Open Drain Control	R/W	0x0	Retain	1 = Open drain I/O
0	GPIO Open Drain Control	R/W	0x0	Retain	1 = Open drain I/O

Table 238: LED Function Control Register
Device 3, Register 0x8310

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x0	0x0	
7:4	GPIO Pin Control for LED Functionality	R/W	0x1	Retain	The GPIO pin must be configured in LED function mode, otherwise 3.8310.7:4 has no effect. 0000 = On - Receive, Off - No Receive 0001 = On - Link, Blink - Activity, Off - No Link 0010 = On - Link, Blink - Receive, Off - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = Reserved 0110 = On - 100 Mbps Link, Off - Else 0111 = On - 100 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 11xx = Reserved

Table 238: LED Function Control Register (Continued)
Device 3, Register 0x8310

Bits	Field	Mode	HW Rst	SW Rst	Description
3:0	TX_ENABLE Pin Control for LED Functionality	R/W	0x1	Retain	The TX_ENABLE pin must be configured in LED function mode, otherwise register 3.8310.3:0 has no effect. 0000 = On - Link, Off - No Link 0001 = On - Link, Blink - Activity, Off - No Link 0010 = 2 blinks - 100 Mbps 0 blink - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - Copper Link, Off - Else 0111 = Reserved 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink 1100 = MODE 1 (Dual LED mode) 1101 = MODE 2 (Dual LED mode) 1110 = MODE 3 (Dual LED mode) 1111 = MODE 4 (Dual LED mode)

Table 239: LED Polarity Control Register
Device 3, Register 0x8311

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	GPIO Pin Mix Percentage for LED Functionality	R/W	0x8	Retain	This register is only used when GPIO is configured in LED function mode. When using two-terminal bi-color LEDs, the mixing percentage must not be set greater than 50%. 0000 = 0% 0001 = 12.5% ... 0111 = 87.5% 1000 = 100% 1001 to 1111 = Reserved
11:8	TX_ENABLE Pin Mix Percentage for LED Functionality	R/W	0x8	Retain	This register is only used when TX_ENABLE is configured in LED function mode. When using two-terminal bi-color LEDs, the mixing percentage must not be set greater than 50%. 0000 = 0% 0001 = 12.5% ... 0111 = 87.5% 1000 = 100% 1001 to 1111 = Reserved
7:4	Reserved	R/W	0x0	Retain	

Table 239: LED Polarity Control Register (Continued)
Device 3, Register 0x8311

Bits	Field	Mode	HW Rst	SW Rst	Description
3:2	GPIO Pin Polarity for LED Functionality	R/W	0x0	Retain	This register is only used when GPIO is configured in LED function mode. 00 = On - drive GPIO low, Off - drive GPIO High 01 = On - drive GPIO high, Off - drive GPIO Low 10 = On - drive GPIO low, Off - tri-state GPIO 11 = On - drive GPIO high, Off - tri-state GPIO
1:0	TX_ENABLE Pin Polarity For LED Functionality	R/W	0x0	Retain	This register is only used when TX_ENABLE is configured in LED function mode. 00 = On - drive LED low, Off - drive LED High 01 = On - drive LED high, Off - drive LED Low 10 = On - drive LED low, Off - tri-state LED 11 = On - drive LED high, Off - tri-state LED

Table 240: LED Timer/INTn Control Register
Device 3, Register 0x8312

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Force INTn	R/W	0x0	Retain	1 = The INTn pin was forced to be asserted. 0 = Normal operation
14:12	Pulse Stretch Duration	R/W	0x4	Retain	000 = No pulse stretching 001 = 21 to 42 ms 010 = 42 to 84 ms 011 = 84 to 170 ms 100 = 170 to 340 ms 101 = 340 to 670 ms 110 = 670 ms to 1.3s 111 = 1.3 to 2.7s
11	Interrupt Polarity	R/W	0x1	Retain	0 = Interrupt active high 1 = Interrupt active low
10:8	Blink Rate	R/W	0x1	Retain	000 = 42 ms 001 = 84 ms 010 = 170 ms 011 = 340 ms 100 = 670 ms 101 to 111 = Reserved
7:4	Reserved	R/W	0x0	Retain	
3:2	Speed Off Pulse Period	R/W	0x1	Retain	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms
1:0	Speed On Pulse Period	R/W	0x1	Retain	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms

Table 241: Copper Port Packet Generation Register Device 3, Register 0x8610

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	
7	Packet Generator Transmit Trigger	R/W	0x0	Retain	This bit is only valid when all of the following are true: • bit 6 =1 • bit 3 =1 • 3.8611.15:0 is not equal to all 0s A read of this bit gives the following: 1 = Packet generator transmit is done. 0 = Packet generator is transmitting data. When this bit is 1, a write of 0 will trigger the packet generator to transmit again. When this bit is 0, a write of 0 or 1 will have no effect.
6	Packet Generator Enable Self Clear Control	R/W	0x0	Retain	0 = Bit 3 will self-clear after all packets are sent. 1 = Bit 3 will stay high after all packets are sent.
5	Reserved	R/W	0x0	Retain	
4	Enable CRC Checker	R/W	0x0	Retain	1 = Enable 0 = Disable
3	Enable Packet Generator	R/W	0x0	Retain	1 = Enable 0 = Disable
2	Payload of Packet to Transmit	R/W	0x0	Retain	0 = Pseudo-random 1 = For 10/100/1000 Mbps = A5, 5A, A5, 5A
1	Length of Packet to Transmit	R/W	0x0	Retain	1 = 1518 bytes 0 = 64 bytes
0	Transmit an Errored Packet	R/W	0x0	Retain	1 = Tx packets with CRC errors and symbol error 0 = No error

Table 242: Copper Port Packet Size Register Device 3, Register 0x8611

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Packet Burst	R/W	0x0000	Retain	0x0000 = Continuous 0x01 to 0xFFFF = Burst 1 to 65535 packets

Table 243: Checker Control Register Device 3, Register 0x8612

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	RO	0x000	Retain	Reserved
4	CRC Counter Reset	R/W, SC	0x0	0x0	1 = Reset This bit will self-clear after write to 1.
3:0	Reserved	R/W	0x0	Retain	Reserved

Table 244: Packet Generator Control Register Device 3, Register 0x8613

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Packet Generator Constant Payload Enable	R/W	0x0	Retain	1 = The payload of the packet controlled by 3.8613.14 when packet generator is enabled. 0 = The payload of the packet controlled by 3.8610.2 when packet generator is enabled.
14	Packet Generator Constant Payload Value	R/W	0x0	Retain	1 = All 1s in the payload when 3.8613.15 = 1 0 = All 0s in the payload when 3.8613.15 = 1
13:8	Reserved	R/W	0x00	Retain	
7:0	Packet Generator Inter-Packet Gap	R/W	0x0B	Retain	This value plus 1 is IPG in bytes.

Table 245: Copper Port Packet Counter Register Device 3, Register 0x8614

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Packet Count	RO	0x0000	Retain	0x0000 = No packets were received. 0xFFFF = 65535 packets were received (maximum count). Bit 3.8610.4 must be set to 1 for this field to be valid.

Table 246: Copper Port CRC Counter Register Device 3, Register 0x8615

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	CRC Error Count	RO	0x0000	Retain	0x0000 = No CRC errors were detected in the packets received. 0xFFFF = 65535 CRC errors were detected in the packets received (maximum count). Bit 3.8610.4 must be set to 1 for this field to be valid.

Table 247: 100BASE-T1 LPSD Status Register Device 3, Register 0x8700

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	R/W	0	Retain	
4	Local Wake Status after T1 Port Sleep	RO, LH	0x0	Retain	This status is valid only after T1 Port Sleep Mode. 1 = The device came out of T1 Port Sleep Mode because a pulse was received at the WAKE_IN pin.
3	Remote Wake Status after T1 Port Sleep	RO, LH	0x0	Retain	This status is valid only after T1 Port Sleep Mode. 1 = The device powered up due to energy received on the MDIN/P pins. 0 = No energy has been detected on the MDIN/P pins.

Table 247: 100BASE-T1 LPSD Status Register (Continued)
Device 3, Register 0x8700

Bits	Field	Mode	HW Rst	SW Rst	Description
2	LPSD Local Wake Status	RO, LH	0x0	Retain	This status is valid only after an LPSD power up. 1 = The device powered up because a pulse was received at the WAKE_IN pin 0 = The device did not power up due to a pulse received at the WAKE_IN pin.
1	LPSD Remote Wake Status	RO, LH	0x0	Retain	This status is valid only after an LPSD power up. 1 = The device powered up because of energy received at the MDIP/N pins 0 = The device did not power up due to energy received at the MDIP/N pins.
0	LPSD Power Down Enable	R/W	0	Retain	1 = Enable an LPSD power down. 0 = Do not enable an LPSD power down.

Table 248: 100BASE-T1 Sleep/Wake Request
Device 3, Register 0x8702

Bits	Field	Mode	HW Rst	SW Rst	Description
15:6	Reserved	R/W	0	Retain	
5	Enable Passive Mode	R/W	0	Strap refer to Hardware configuration, (RXC Pin)	1 = Enable. This will put the port in T1 Port Sleep Mode by powering down the port without completing a Sleep handshake.
4	Local Wake Request (to trigger WUR)	R/W	0	Retain	1 = Trigger WUR to the link partner.
3	Enable Passive mode exit	R/W	0	Retain	1 = 100BT1 allows the device to exit passive mode on wake event. 0 = 100BT1 passive mode disabled only upon write to register 3.8702[5].
2	Reserved	R/W	0	Retain	
1	Sleep Abort	R/W	0	Retain	1 = Abort the Sleep Request Received from the link partner.
0	Local Sleep Request	R/W	0	Retain	1 = Sleep Request The device will initiate sleep handshake with the link partner. This register does not do anything if 3.8707.0 is 0.

Table 249: 100BASE-T1 Sleep Status Device 3, Register 0x8703

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	R/W	0	Retain	
2:0	Sleep Status	RO	0	Retain	3'b000 = Normal 3'b001 = Sleep 3'b010 = Sleep has failed. 3'b100 = Sleep Request has been aborted.

Table 250: 100BASE-T1 Wakeup Status Device 3, Register 0x8704

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	R/W	0	Retain	
0	Wakeup Status	RO	0	Retain	1 = Wakeup was received.

Table 251: 100BASE-T1 Sleep/Wakeup Interrupt Status Device 3, Register 0x8705

Bits	Field	Mode	HW Rst	SW Rst	Description
15:9	Reserved	R/W	0	Retain	
8	Pulse Received on WAKE_IN pin Digital or Analog Pulse	RO, LH	0	Retain	1 = Pulse Received on WAKE_IN pin (Digital or Analog pulse)
7	Pulse Received on WAKE_IN pin Analog Pulse	RO, LH	0	Retain	1 = Pulse Received on WAKE_IN pin (only in Deep Sleep Mode)
6	WUR Received	RO, LH	0	Retain	1 = WUR Received
5	WUP Received when device in Deep Sleep Mode	RO, LH	0	Retain	1 = WUP Received when device in Deep Sleep Mode
4	WUP Received when device in T1 Port Sleep Mode	RO, LH	0	Retain	1 = WUP Received when device in T1 Port Sleep Mode
3	Sleep Request Aborted	RO, LH	0	Retain	1 = Sleep Request has been aborted.
2	Sleep Fail Status	RO, LH	0	Retain	1 = Sleep failed since last read.
1	Sleep Status	RO, LH	0	Retain	1 = Sleep completed since last read.
0	Wakeup Status	RO, LH	0	Retain	1 = Wakeup received since last read.

Table 252: 100BASE-T1 Sleep/Wakeup Interrupt Enable Device 3, Register 0x8706

Bits	Field	Mode	HW Rst	SW Rst	Description
15:9	Reserved	R/W	0	Retain	
8	Pulse Received on WAKE_IN pin Digital or Analog Pulse Interrupt Enable	R/W	0	Retain	1 = Enable
7	Pulse Received on WAKE_IN pin Analog Pulse Interrupt Enable	R/W	0	Retain	1 = Enable
6	WUR Received Interrupt Enable	R/W	0	Retain	1 = Enable
5	WUP Received when device in Deep Sleep Mode Interrupt Enable	R/W	0	Retain	1 = Enable
4	WUP Received when device in T1 Port Sleep Mode Interrupt Enable	R/W	0	Retain	1 = Enable
3	Sleep Request Aborted Interrupt Enable	R/W	0	Retain	1 = Enable
2	Sleep Fail Status Interrupt Enable	R/W	0	Retain	1 = Enable
1	Sleep Status Interrupt Enable	R/W	0	Retain	1 = Enable
0	Wakeup Status Interrupt Enable	R/W	0	Retain	1 = Enable

Table 253: 100BT1 Sleep/Wakeup Interrupt Status 2 Device 3, Register 0x870A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	RO, LH	0	Retain	
4	LPS Received from Link Partner	RO, LH	0	Retain	1 = LPS Received from Link Partner
3:0	Reserved	RO, LH	0	Retain	

Table 254: 100BT1 Sleep/Wakeup Interrupt Enable 2
Device 3, Register 0x870B

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	RO, LH	0	Retain	
4	LPS Received from Link Partner Interrupt Enable	RO, LH	0	Retain	1 = Enable
3:0	Reserved	RO, LH	0	Retain	

3.6 1000BASE-T1 Copper Unit Advance PCS Registers

Table 255: 1000BASE-T1 Copper Unit Advance PCS Registers — Register Map

Register Name	Register Address	Table and Page
GPIO Data Register	Device 3, Register 0x8012	Table 256, p. 209
GPIO Function and Interrupt Tri-state Control Register	Device 3, Register 0x8013	Table 257, p. 209
GPIO Interrupt Register	Device 3, Register 0x8014	Table 258, p. 210
Open Drain Control Register	Device 3, Register 0x8015	Table 259, p. 211
LED Function Control Register	Device 3, Register 0x8016	Table 260, p. 211
LED [1:0] Polarity Control Register	Device 3, Register 0x8017	Table 261, p. 211
LED Timer Control Register	Device 3, Register 0x8018	Table 262, p. 212
1000BT LPSD Status Register	Device 3, Register 0x8020	Table 263, p. 213
1000BT1 Sleep/Wake Request	Device 3, Register 0x8022	Table 264, p. 213
1000BT1 Sleep Status	Device 3, Register 0x8023	Table 265, p. 214
1000BT1 Wakeup Status	Device 3, Register 0x8024	Table 266, p. 214
1000BT1 Sleep/Wakeup Interrupt Status	Device 3, Register 0x8025	Table 267, p. 214
1000BT1 Sleep/Wakeup Interrupt Enable	Device 3, Register 0x8026	Table 268, p. 215
1000BT1 Sleep/Wakeup Interrupt Status 2	Device 3, Register 0x802A	Table 269, p. 216
1000BT1 Sleep/Wakeup Interrupt Enable 2	Device 3, Register 0x802B	Table 270, p. 216
Signal Quality Index	Device 3, Register 0xFCD8	Table 271, p. 216
Mean Square Error	Device 3, Register 0xFCDA	Table 272, p. 216
Worst Case Mean Square Error	Device 3, Register 0xFCDB	Table 273, p. 217
PCS Control Register	Device 3, Register 0xFD00	Table 274, p. 217
Packet Generator Control Register	Device 3, Register 0xFD04	Table 275, p. 218
Packet Generator Parameters Register	Device 3, Register 0xFD05	Table 276, p. 218
Packet Checker Control Register	Device 3, Register 0xFD07	Table 277, p. 219
Packet Checker Count Register	Device 3, Register 0xFD08	Table 278, p. 219
Tx FIFO Control Register	Device 3, Register 0xFD20	Table 279, p. 219
LinkUp Status Count	Device 3, Register 0xFDBD	Table 280, p. 219
LinkDown Status Count	Device 3, Register 0xFDBE	Table 281, p. 219
Enable Code Word Count	Device 3, Register 0xFDEF	Table 282, p. 220
Retain Code Word Count	Device 3, Register 0xFDF0	Table 283, p. 220
Clear Code Word Count	Device 3, Register 0xFDF1	Table 284, p. 220
Correctable Code Word Count	Device 3, Register 0xFDF2	Table 285, p. 220
1000BASE-T1 Link Training Time	Device 3, Register 0xFF4A	Table 286, p. 220
1000BASE-T1 Local Receiver Time	Device 3, Register 0xFF4B	Table 287, p. 221
1000BASE-T1 Remote Receiver Time	Device 3, Register 0xFF4C	Table 288, p. 221

Table 256: GPIO Data Register
Device 3, Register 0x8012

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	R/W	0x0	Retain	
1	LED Data	R/W	0x0	Retain	This bit has no effect unless register 3.8014.3 = 1. When 3.8013.1 = 0, a read to this register will reflect the state of the LED pin and a write will write the output register, but have no effect on the LED pin. When 3.8013.1 = 1, a read to this register will reflect the state of the output register and a write will write the output register and drive the state of the LED pin.
0	GPIO Data	R/W	0x0	Retain	When 3.8013.0 = 0, a read to this register will reflect the state of the GPIO pin, and a write will write the output register, but have no effect on the GPIO pin. When 3.8013.0 = 1, a read to this register will reflect the state of the output register and a write will write the output register and drive the state of the GPIO pin.

Table 257: GPIO Function and Interrupt Tri-state Control Register
Device 3, Register 0x8013

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	Reserved	R/W	0x000	Retain	Set to 0s.
11	Tri-state on Interrupt Pin	R/W	0x0	Retain	0 = Tri-state is enabled; the interrupt pin is configured as an input. 1 = Tri-state is disabled.
10	Observe LED on GPIO	R/W	0x1	Retain	1 = The LED pin is driven on GPIO. 0 = The LED is not driven on GPIO.
9	Open Drain Control	R/W	0x0	Retain	INT open drain control 1 = This is an open drain I/O where the output is driven LOW for an active interrupt and tri-stated for an inactive one and there would be an external pull-up to drive the line HIGH.
8	Open Source Control	R/W	0x0	Retain	INT open source control 1 = This is an open source I/O where the output is driven HIGH for an active interrupt and tri-stated for an inactive one and there would be an external pull-down to drive the line LOW.
7	LED/GPIO Data from 1000BASE_T1 Valid	R/W	0x0	Retain	0 = If bit 6 is set, then overwrite mode so that LED/GPIO value must be from 100BASE-T1 LED registers. 1 = If bit 6 is set, then overwrite mode so that LED/GPIO value must be from 1000BASE-T1 LED/GPIO register.
6	LED/GPIO Overwrite Control	R/W	0x0	Retain	This is the LED/GPIO value from 100 or 1000BASE-T1 based on bit 7.
5	LED Drive Ability	R/W	0x0	Retain	Fast LED mode 0 = LED pads drive LEDs. 1 = LED pads can drive fast signals.

Table 257: GPIO Function and Interrupt Tri-state Control Register (Continued)
Device 3, Register 0x8013

Bits	Field	Mode	HW Rst	SW Rst	Description
4	GPIO Functionality	R/W	0x0	Retain	The function of GPIO pin is mapped to following: 0 = GPIO 1 = LED
3:2	Reserved	R/W	0x0	Retain	
1	LED Output Enable	R/W	0x1	Retain	This bit has no effect unless register 3.8014.3 = 1. 0 = Input 1 = Output
0	GPIO Output Enable	R/W	0x1	Retain	0 = Input 1 = Output

Table 258: GPIO Interrupt Register
Device 3, Register 0x8014

Bits	Field	Mode	HW Rst	SW Rst	Description
15:11	Reserved	R/W	0x00	Retain	
10:8	GPIO Select	R/W	0x0	Retain	Interrupt is effective only when 3.8013.0 = 0. 000 = No interrupt 001 = Reserved 010 = Interrupt on low level 011 = Interrupt on high level 100 = Interrupt on high to low 101 = Interrupt on low to high 110 = Reserved 111 = Interrupt on low to high or high to low
7:4	Reserved	R/W	0x00	Retain	
3	LED Function	R/W	0x0	Retain	0 = LED [0] is used for an LED function. 1 = LED [0] is used for a GPIO function.
2:0	LED Select	R/W	0x0	Retain	Interrupt is effective only when 3.8013.4 = 0. 000 = No interrupt 001 = Reserved 010 = Interrupt on low level 011 = Interrupt on high level 100 = Interrupt on high to low 101 = Interrupt on low to high 110 = Reserved 111 = Interrupt on low to high or high to low

Table 259: Open Drain Control Register Device 3, Register 0x8015

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	RW	0x00	Retain	
9:8	Slew Rate LED Pad	RW	0x2	Retain	Slew Rate for LED I/O Pad Fastest slew rate to Slowest: 11,10,01,00
7:6	Slew Rate for Left side I/O Pads	RW	0x3	Retain	Slew Rate for Left side I/O Pad INT/MDIO/GPIO Fastest slew rate to Slowest: 11,10,01,00
5:2	Reserved	RW	0x00	Retain	
1	LED Open Drain Control	RW	0x0	Retain	1 = Open drain I/O
0	GPIO Open Drain Control	RW	0x0	Retain	1 = Open drain I/O

Table 260: LED Function Control Register Device 3, Register 0x8016

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	
7:4	Reserved	R/W	0x00	Retain	Reserved
3:0	LED Control	R/W	0x1	Retain	0000 = On - Link, Off - No Link 0001 = On - Link, Blink - Activity, Off - No Link 0010 = 3 blinks - 1000 Mbps 0 blink - No Link 0011 = On - Activity, Off - No Activity 0100 = Blink - Activity, Off - No Activity 0101 = On - Transmit, Off - No Transmit 0110 = On - Copper Link, Off - Else 0111 = On - 1000 Mbps Link, Off - Else 1000 = Force Off 1001 = Force On 1010 = Force Hi-Z 1011 = Force Blink

Table 261: LED [1:0] Polarity Control Register Device 3, Register 0x8017

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	R/W	0x0	Retain	
1:0	LED Polarity	R/W	0x0	Retain	00 = On - Drive LED low, Off - Drive LED [0] high 01 = On - Drive LED high, Off - Drive LED [0] low 10 = On - Drive LED low, Off - Tri-state LED [0] 11 = On - Drive LED high, Off - Tri-state LED [0]

Table 262: LED Timer Control Register
Device 3, Register 0x8018

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Force INT	R/W	0x0	0x0	1 = The int_out_s pin is forced to be asserted. 0 = Normal operation
14:12	Pulse Stretch Duration	R/W	0x4	Retain	000 = No pulse stretching 001 = 21 to 42 ms 010 = 42 to 84 ms 011 = 84 to 170 ms 100 = 170 to 340 ms 101 = 340 to 670 ms 110 = 670 ms to 1.3s 111 = 1.3 to 2.7s
11	Interrupt Polarity	R/W	0x1	Retain	0 = Interrupt active high 1 = Interrupt active low
10:8	Blink Rate	R/W	0x1	Retain	000 = 42 ms 001 = 84 ms 010 = 170 ms 011 = 340 ms 100 = 670 ms 101 to 111 = Reserved
7:6	Reserved	R/W	0x0	Retain	
5	Timer Speed Up	R/W	0x0	Retain	Internal test mode: Timer Speed Up 1 = Speed up timer. 0 = Normal operation
4	Bypass LED Blinker	R/W	0x0	Retain	Internal test mode: Bypass LED Blinker 1 = Bypass LED blinker. 0 = Normal operation
3:2	Speed Off Pulse Period	R/W	0x1	Retain	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms
1:0	Speed On Pulse Period	R/W	0x1	Retain	00 = 84 ms 01 = 170 ms 10 = 340 ms 11 = 670 ms

Table 263: 1000BT LPSD Status Register
Device 3, Register 0x8020

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	R/W	0	Retain	
4	Local Wake Status after T1 Port Sleep	RO	0	Retain	This status is valid only after T1 Port Sleep Mode. 1 = The device came out of T1 Port Sleep Mode because a pulse was received at the WAKE_IN pin.
3	Wake Status after T1 Port Sleep	RO	0	Retain	This status is valid only after T1 Port Sleep Mode. 1 = The port is powered up due to energy received on the MDIN/P pins. 0 = No energy has been detected on the MDIN/P pins.
2	LPSD Local Wake Status	RO	0	Retain	This status is valid only after an LPSD power up. 1 = The device powered up because a pulse was received at the WAKE_IN pin. 0 = The device did not power up due to a pulse received at the WAKE_IN pin.
1	LPSD Remote Wake Status	RO	0	Retain	This status is valid only after an LPSD power up. 1 = The device powered up because of energy received at the MDIP/N pins. 0 = The device did not power up due to energy received at the MDIP/N pins.
0	LPSD Power Down Enable	R/W	0	Retain	1 = Enable an LPSD power down. 0 = Do not enable an LPSD power down.

Table 264: 1000BT1 Sleep/Wake Request
Device 3, Register 0x8022

Bits	Field	Mode	HW Rst	SW Rst	Description
15:6	Reserved	RO	0	Retain	
5	Enable Passive Mode	R/W	0	Strap refer to Hardware configuration, (RXC Pin)	1 = Enable. This will put the Port in T1 Port Sleep Mode by powering down the port without completing a Sleep handshake.
4	Local Wake Request (to trigger WUR)	R/W	0	Retain	1= Wake up and send WUP if the device is powered down; otherwise, send WUR when the device gets to Linkup state. 0 = Disabled
3	Enable Passive mode exit	R/W	0	Retain	1 = 1000BT1 allows the device to exit passive mode on wake event 0 = 1000BT1 passive mode disabled only upon write to register 3.8022[5]
2	Reserved	RO	0	Retain	
1	Sleep Abort	R/W	0	Retain	1 = Abort the Sleep Request Received from the link partner.

Table 264: 1000BT1 Sleep/Wake Request (Continued)
Device 3, Register 0x8022

Bits	Field	Mode	HW Rst	SW Rst	Description
0	Local Sleep Request	R/W	0	Retain	1 = Sleep Request. The device will initiate sleep handshake with the link partner. This register does not do anything if 3.8027.0 is 0.

Table 265: 1000BT1 Sleep Status
Device 3, Register 0x8023

Bits	Field	Mode	HW Rst	SW Rst	Description
15:3	Reserved	RO	0	Retain	
2:0	Sleep Status	RO	0	Retain	3'b000 = Normal 3'b001 = Sleep. 3'b010 = Sleep Failed. 3'b100 = Sleep Request has been aborted.

Table 266: 1000BT1 Wakeup Status
Device 3, Register 0x8024

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	RO	0	Retain	
0	Wakeup Status	RO	0	Retain	1 = Wakeup received

Table 267: 1000BT1 Sleep/Wakeup Interrupt Status
Device 3, Register 0x8025

Bits	Field	Mode	HW Rst	SW Rst	Description
15:9	Reserved	RO	0	Retain	
8	Pulse Received on WAKE_IN pin Digital or Analog Pulse	RO, LH	0	Retain	1 = Pulse Received on WAKE_IN pin (Digital or Analog pulse).
7	Pulse Received on WAKE_IN pin Analog Pulse	RO, LH	0	Retain	1 = Pulse Received on WAKE_IN pin (only in Deep Sleep Mode).
6	WUR Received	RO, LH	0	Retain	1 = WUR Received.
5	WUP Received when device in Deep Sleep Mode	RO, LH	0	Retain	1 = WUP Received when the device is in Deep Sleep Mode.
4	WUP Received when device in T1 Port Sleep Model	RO, LH	0	Retain	1 = WUP Received when the device is in T1 Port Sleep Mode.

Table 267: 1000BT1 Sleep/Wakeup Interrupt Status (Continued)
Device 3, Register 0x8025

Bits	Field	Mode	HW Rst	SW Rst	Description
3	Sleep Request Aborted	RO, LH	0	Retain	1 = Sleep Request has been aborted.
2	Sleep Fail Status	RO, LH	0	Retain	1 = Sleep Failed since last read
1	Sleep Status	RO, LH	0	Retain	1 = Sleep completed since last read
0	Wakeup Status	RO, LH	0	Retain	1 = Wakeup received since last read

Table 268: 1000BT1 Sleep/Wakeup Interrupt Enable
Device 3, Register 0x8026

Bits	Field	Mode	HW Rst	SW Rst	Description
15:9	Reserved	R/W	0	Retain	
8	Pulse Received on WAKE_IN pin Digital or Analog Pulse Interrupt Enable	R/W	0	Retain	1 = Enable Interrupt 0 = Disable Interrupt
7	Pulse Received on WAKE_IN pin Analog Pulse Interrupt Enable	R/W	0	Retain	1 = Enable Interrupt 0 = Disable Interrupt
6	WUR Received Interrupt Enable	R/W	0	Retain	1 = Enable Interrupt 0 = Disable Interrupt
5	WUP Received when device in Deep Sleep Mode Interrupt Enable	R/W	0	Retain	1 = Enable Interrupt 0 = Disable Interrupt
4	WUP Received when device in T1 Port Sleep Mode Interrupt Enable	R/W	0	Retain	1 = Enable Interrupt 0 = Disable Interrupt
3	Sleep Request Aborted Interrupt Enable	R/W	0	Retain	1 = Enable Interrupt 0 = Disable Interrupt
2	Sleep Fail Status Interrupt Enable	R/W	0	Retain	1 = Enable Interrupt 0 = Disable Interrupt
1	Sleep Status Interrupt Enable	R/W	0	Retain	1 = Enable Interrupt 0 = Disable Interrupt
0	Wakeup Status Interrupt Enable	R/W	0	Retain	1 = Enable Interrupt 0 = Disable Interrupt

Table 269: 1000BT1 Sleep/Wakeup Interrupt Status 2
Device 3, Register 0x802A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	RO, LH	0	Retain	
4	LPS Received from Link Partner	RO, LH	0	Retain	1 = LPS Received from Link Partner
3:0	Reserved	RO, LH	0	Retain	

Table 270: 1000BT1 Sleep/Wakeup Interrupt Enable 2
Device 3, Register 0x802B

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	RO, LH	0	Retain	
4	LPS Received from Link Partner Interrupt Enable	RO, LH	0	Retain	1 = Enable
3:0	Reserved	RO, LH	0	Retain	

Table 271: Signal Quality Index
Device 3, Register 0xFCD8

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	RO	0x0	Retain	
6:4	SQI worst Case	RO	0x0	Retain	Worst SQI since last read.
3	Reserved	RO	0x0	Retain	
2:0	SQI current	RO	0x00	Retain	This is the Signal Quality index The SQI level is listed from 0 to 7 in accordance with the ascending signal quality. The SQI level is reported as 0 during the link up process and if there is no link up.

Table 272: Mean Square Error
Device 3, Register 0xFCDA

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	RO	0x0	Retain	
9	Mean Square Error Value Valid	RO	0x1	Retain	1 = Invalid 0 = Valid

Table 272: Mean Square Error
Device 3, Register 0xFCDA

Bits	Field	Mode	HW Rst	SW Rst	Description
8:0	Mean Square Error	RO	0x00	Retain	0x000 = ME = 0 0x001 = MSE = 1 … 0x1FE = MSE = 510 0x1FF = MSE = 511

Table 273: Worst Case Mean Square Error
Device 3, Register 0xFCDB

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	RO	0x0	Retain	
9	Worst Case Mean Square Error Valid	RO	0x1	Retain	1 = Invalid 0 = Valid
8:0	Worst Case Mean Square Error	RO	0x00	Retain	Worse case Mean square Error Value 0x000 = ME = 0 0x001 = MSE = 1 … 0x1FE = MSE = 510 0x1FF = MSE = 511

Table 274: PCS Control Register
Device 3, Register 0xFD00

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Reserved	R/W	0x7	Retain	Reserved
12:7	PCS Host Config	R/W	0x00	0x00	GMII data steering as shown in Figure 25, Data Steering around GMII Interface. Bits 12, 11 (MUX C in Figure 25) 0x = Line Rx to packet checker 10 = Host Tx to packet checker 11 = Packet generator to packet checker Bits 10, 9 (MUX B in Figure 25) 0x = Host Tx to line Tx 10 = Line Rx to line Tx 11 = Packet generator to line Tx Bits 8, 7 (MUX A in Figure 25) 0x = Line Rx to host Rx 10 = Host Tx to host Rx 11 = Packet generator to host Rx
6:0	Reserved	R/W	0x00	0x00	Reserved

Table 275: Packet Generator Control Register Device 3, Register 0xFD04

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Packet Burst	R/W	0x00	Retain	0x00 = Continuous 0x01 to 0xFF = Burst 1 to 255 packets
7	Packet Generator Transmit Trigger	R/W	0x0	0x0	This bit is only valid when all of the following are true: • Bit 6 = 1. • Bit 3 = 1. • Bits [15:8] are not equal to all 0s. A read of this bit gives the following: • 1 = Packet generator transmit is done. • 0 = Packet generator is transmitting data. When this bit is 1, a write of 0 will trigger the packet generator to transmit again. When this bit is 0, a write of 0 or 1 will have no effect.
6	Packet Generator Enable Self Clear Control	R/W	0x0	0x0	0 = Bit 3 will self-clear after all packets are sent. 1 = Bit 3 will stay high after all packets are sent.
5:4	Reserved	RO	0x0	0x0	
3	Enable Packet Generator	R/W, SC	0x0	0x0	1 = Enable 0 = Disable
2	Payload of Packet to Transmit	R/W	0x0	0x0	0 = Pseudo-random 1 = 5A, A5, 5A, A5, and so on
1	Length of Packet to Transmit	R/W	0x0	0x0	1 = 1518 bytes 0 = 64 bytes
0	Transmit an Errored Packet	R/W	0x0	0x0	1 = Tx packets with CRC errors and symbol error 0 = No error

Table 276: Packet Generator Parameters Register Device 3, Register 0xFD05

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Constant Packet Payload Enable	R/W	0x0	0x0	This enables a constant payload for packets generated by the packet generator. 1 = Enable constant packet payload. 0 = Use other payload options.
14	Constant Packet Payload Type	R/W	0x0	0x0	This bit selects the type of constant payload to use. It is valid only when 3.FD05.15 = 1. 1 = Use all 1s packet payload. 0 = Use all 0s packet payload.
13:8	Reserved	RO	0x00	0x00	
7:0	IPG Length	R/W	12	0x00	The number in bits [7:0] +1 is the number of bytes for IPG.

Table 277: Packet Checker Control Register Device 3, Register 0xFD07

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	0x000	0x000	
3	CRC Reset	R/W	0x0	0x0	Reset CRC/packet counter.
2	PC Enable	R/W	0x0	0x0	Enable CRC/packet counter block.
1	Reserved	R/W	0x0	0x0	
0	CRC Sample	R/W	0x0	0x0	Start packet counter and CRC counter sampling.

Table 278: Packet Checker Count Register Device 3, Register 0xFD08

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Error Package Counter Readout	RO	0x00	0x00	Error Package Counter Readout
7:0	Receive Package Counter Readout	RO	0x00	0x00	Receive Package Counter Readout

Table 279: Tx FIFO Control Register Device 3, Register 0xFD20

Bits	Field	Mode	HW Rst	SW Rst	Description
15:2	Reserved	RO	0x0000	0x0000	
1:0	Tx FIFO Depth	R/W	0x1	Retain	00 = This supports 10 KB at ±100 ppm. 01 = This supports 15 KB at ±100 ppm. 10 = This supports 20 KB at ±100 ppm. 11 = This supports 25 KB at ±100 ppm.

Table 280: LinkUp Status Count Device 3, Register 0xFDBD

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Link up Count	SC/RO	0x00	Retain	Counts the number of time device linked up. This register will clear to 0 upon read.

Table 281: LinkDown Status Count Device 3, Register 0xFDBE

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Link Down Count	SC/RO	0x00	Retain	Counts the number of time device linked down. This register will clear to 0 upon read.

Table 282: Enable Code Word Count
Device 3, Register 0xFDEF

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	R/W	0x0	Retain	
0	Enable Correctable CWD	R/W	0x0	Retain	1 = Enable count of register 3.FDF2. 0 = Disable count.

Table 283: Retain Code Word Count
Device 3, Register 0xFDF0

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	R/W	0x0	Retain	
0	Retain Correctable CWD	R/W	0x0	Retain	1 = Retain count of register 3.FDF2 correctable code word.

Table 284: Clear Code Word Count
Device 3, Register 0xFDF1

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	Reserved	SC	0x0	Retain	
0	Clear Correctable CWD	SC	0x0	0x0	1 = Clear count of register 3.FDF2 correctable code word.

Table 285: Correctable Code Word Count
Device 3, Register 0xFDF2

Bits	Field	Mode	HW Rst	SW Rst	Description
15:10	Reserved	RO	0x00	Retain	
9:0	Correctable CWD Count	RO	0x0	0x0	Reports number of correctable code word. Read to clear register unless retain bit is set.

Table 286: 1000BASE-T1 Link Training Time
Device 3, Register 0xFF4A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x0	0x0	
7:0	Link Training Timer	RO	0x0	0x0	Each count corresponds to 1 ms. Information about the link training of the last link training; max value (FA) 250 ms. FB = More than 250 ms FF = Measurement not possible

Table 287: 1000BASE-T1 Local Receiver Time Device 3, Register 0xFF4B

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x0	0x0	
7:0	Local Receiver Timing	RO	0x0	0x0	Each count corresponds to 1 ms. Time until local receiver =OK; max value (FA) 250 ms. FB = More than 250 ms FF = Measurement not possible

Table 288: 1000BASE-T1 Remote Receiver Time Device 3, Register 0xFF4C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	RO	0x0	0x0	
7:0	Remote Receiver Timing	RO	0x0	0x0	Each count corresponds to 1 ms. Time until remote receiver =OK; max value (FA) 250 ms. FB = More than 250 ms FF = Measurement not possible

3.7 Copper Unit Advance Auto-Negotiation Registers

Table 289: Copper Unit Advance Auto-Negotiation Registers — Register Map

Register Name	Register Address	Table and Page
Auto-Negotiation Status Register	Device 7, Register 0x8001	Table 290, p. 222
Auto-Negotiation Status 2 Register	Device 7, Register 0x8016	Table 291, p. 222
Auto-Negotiation Status Register 2	Device 7, Register 0x801A	Table 292, p. 223

Table 290: Auto-Negotiation Status Register Device 7, Register 0x8001

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Master/Slave Configuration Fault	RO, LH	0x0	0x0	This register bit will clear on read. 1 = Master/slave configuration fault has been detected. 0 = No master/slave configuration fault has been detected.
14	Master/Slave Configuration Resolution	RO	0x0	0x0	1 = The local PHY configuration is resolved to the master. 0 = The local PHY configuration is resolved to the slave.
13	Remote Receiver Status	RO	0x0	0x0	1 = The remote receiver is OK. 0 = The remote receiver is not OK.
12	Local Receiver Status	RO	0x0	0x0	1 = The local receiver is OK. 0 = The local receiver is not OK.
11:9	Reserved	RO	0x0	0x0	
8	Link Partner Auto-Negotiation Enable	RO	0x0	0x0	This enables the link partner's Auto-Negotiation.
7:0	Reserved	RO	0x00	0x00	

Table 291: Auto-Negotiation Status 2 Register Device 7, Register 0x8016

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	
14	Device Link	RO	0x0	0x0	1 = The device link is valid. 0 = The device is not linked.
13:6	Reserved	RO	0x01	0x00	
5	Acknowledge Finished	RO	0x0	0x0	1 = Acknowledge is finished.
4	Page Received	RO	0x0	0x0	1 = The page is received.
3	Clear HCD	RO	0x1	0x1	1 = The HCD is cleared.
2	HCD Resolved	RO	0x0	0x0	1 = Auto-Negotiation HCD has been resolved.
1	Reserved	RO	0x0	0x0	
0	Auto-Negotiation Link	RO	0x0	0x0	1 = FLP exchange is complete, wait for link up.

Table 292: Auto-Negotiation Status Register 2
Device 7, Register 0x801A

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	0x0	0x0	
14:13	AN Speed Selected	RO	0x2	0x0	01 = 100BT1 selected 10 = 1000BT1 Selected
12	Auto-Negotiation Page Received	RO	0x0	0x0	1 = The Auto-Negotiation page has been received.
11	Auto-Negotiation HCD Resolved	RO	0x0	0x0	1 = The Speed and Auto-Negotiation settings are resolved.
10	PCS Link	RO	0x0	0x0	1 = The PCS link is complete (training complete).
9	Auto-Negotiation Pause Tx	RO	0x0	0x0	1 = Pause Tx.
8	Auto-Negotiation Pause Rx	RO	0x0	0x0	1 = Pause Rx.
7	Reserved	RO	0x0	0x0	1 = The link partner is able to perform Auto-Negotiation. 0 = The link partner is not able to perform Auto-Negotiation.
6:0	Reserved	RO	0x0	0x0	

3.8 RGMII Registers

Table 293: RGMII Registers — Register Map

Register Name	Register Address	Table and Page
RGMII_IO Control Register	Device 3, Register 0x8019	Table 294, p. 224
Com Port Control Register	Device 4, Register 0xA001	Table 295, p. 224

Table 294: RGMII_IO Control Register Device 3, Register 0x8019

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x0	Retain	
7:6	PMOS Slew Rate Adjustment	R/W	0x2	Retain	ZP_DSR is used to program the PMOS output slew rate for RGMII output pads. 2'b11 gives the strongest setting.
5:4	PMOS Impedance Adjustment	R/W	0x2	Retain	ZP_DCS is used to program the PMOS output slew rate for RGMII output pads. 2'b11 gives the strongest setting.
3:2	NMOS Slew Rate Adjustment	R/W	0x2	Retain	ZN_DSR is used to program the NMOS output slew rate for RGMII output pads. 2'b11 gives the strongest setting.
1:0	NMOS Impedance Adjustment	R/W	0x2	Retain	ZN_DCS is used to program the NMOS output slew rate for RGMII output pads. 2'b11 gives the strongest setting.

Table 295: Com Port Control Register Device 4, Register 0xA001

Bits	Field	Mode	HW Rst	SW Rst	Description
15	RGMII Transmit Timing Control	R/W	0x0**	Update	Changes to this bit are disruptive to the normal operation; any changes to these registers must be followed by software reset (3.8000.15) to take effect. 1 = Transmit clock is internally delayed. 0 = Transmit clock is not internally delayed. **Default value 0x0 if configured to RGMII mode1 TCLK no delay; 0x1 if configured to RGMII mode2 TCLK Delay.
14	RGMII Receive Timing Control	R/W	0x1	Update	Changes to this bit are disruptive to the normal operation; so any changes to these registers must be followed by software reset (3.8000.15) to take effect. 1 = Receive clock transition when the data is stable. 0 = Receive clock transition when the data transitions.
13	RXCLK During Power Down	R/W	0x0	0x0	1 = RXCLK toggles during power down. 0 = RXCLK stops during power down.
12	Isolate	R/W	0x0	0x0	1 = Tri-state the output pins of RXC, RXCLK, and RXD. 0 = Normal operation
11:0	Reserved	R/W	0x000	0x000	

3.9 SGMII Registers

Table 296: SGMII Registers — Register Map

Register Name	Register Address	Table and Page
SGMII Control Register	Device 4, Register 0x8000	Table 297, p. 226
SGMII Status Register	Device 4, Register 0x8001	Table 298, p. 227
PHY Identifier Register 1	Device 4, Register 0x8002	Table 299, p. 228
SGMII Auto-Negotiation Advertisement Register	Device 4, Register 0x8004	Table 300, p. 229
SGMII Link Partner Ability/SGMII Register	Device 4, Register 0x8005	Table 301, p. 231
SGMII Auto-Negotiation Expansion Register	Device 4, Register 0x8006	Table 302, p. 232
SGMII Next Page Transmit Register	Device 4, Register 0x8007	Table 303, p. 232
SGMII Link Partner Register	Device 4, Register 0x8008	Table 304, p. 233
SGMII SERDES Specific Control 1 Register	Device 4, Register 0x8010	Table 305, p. 233
SGMII Extended Status Register	Device 4, Register 0x800F	Table 306, p. 234
SGMII Specific Status Register	Device 4, Register 0x8011	Table 307, p. 234
SGMII Interrupt Enable Register	Device 4, Register 0x8012	Table 308, p. 236
SGMII Interrupt Status Register	Device 4, Register 0x8013	Table 309, p. 237
SGMII Receive Error Counter Register	Device 4, Register 0x8015	Table 310, p. 237
PRBS Control Register	Device 4, Register 0x8017	Table 311, p. 238
PRBS Error Counter LSB Register	Device 4, Register 0x8018	Table 312, p. 238
PRBS Error Counter MSB Register	Device 4, Register 0x8019	Table 313, p. 238
SGMII Specific Control Register 2	Device 4, Register 0x801A	Table 314, p. 239
Packet Generation	Device 4, Register 0x801C	Table 315, p. 239
CRC Counters	Device 4, Register 0x801D	Table 316, p. 240
Checker Control	Device 4, Register 0x801E	Table 317, p. 240
Packet Generation 2	Device 4, Register 0x801F	Table 318, p. 240

Table 297: SGMII Control Register Device 4, Register 0x8000

Bits	Field	Mode	HW Rst	SW Rst	Description
15	SGMII Reset	R/W	0x0	SC	SGMII Software Reset. This affects 4.80xx registers. Writing 1 to this bit causes the PHY state machines to be reset. When the reset operation is complete, this bit is cleared to 0 automatically. The reset occurs immediately. 1 = PHY reset 0 = Normal operation
14	Loopback	R/W	0x0	0x0	When loopback is activated, the transmitter data presented on TXD of the internal bus is looped back to RXD of the internal bus. The link is broken when loopback is enabled. The loopback speed is determined by the mode in which the device is enabled. 1000BASE-X - loopback is always in 1000 Mbps. SGMII - loopback follows the current speed specified. 1 = Enable Loopback 0 = Disable Loopback
13	Speed Select (LSB)	RO, R/W	0x0	Retain	If register 4.8010.1:0 (MODE[1:0]) = 01 (1000BASE-X mode), then this bit is always 0. If register 4.8010.1:0 (MODE[1:0]) = 10 (SGMII mode), then this bit is 1 when the PHY is at 100 Mbps, else it is 0. This bit is undefined if register 4.8010.1:0 (MODE[1:0]) = 00 or 11.
12	Auto-Negotiation Enable	R/W	0x1	Retain	If the value of this bit is changed, then the link will be broken and Auto-Negotiation is restarted. For SGMII, Auto-Negotiation is enabled by default. For 1000BASE-X, Auto-Negotiation is off by default. When this bit gets set/reset, Auto-Negotiation is restarted (bit 4.0x8000.9 is set to 1). On hardware reset, this bit takes on the value of S_ANEG. 1 = Enable the Auto-Negotiation Process. 0 = Disable the Auto-Negotiation Process.
11	Power Down	R/W	See Description.	0x0	When the port is switched from power down to normal operation, software reset and Restart Auto-Negotiation are performed even when bits Reset (4.0x8000.15) and Restart Auto-Negotiation (4.0x8000.9) are not set by the user. On hardware reset, this bit assumes the value of ps_mode [1:0]. It will be power down when it is in RGMII mode. 1 = Power down. 0 = Normal operation
10	Isolate	RO	0x0	0x0	This function is not supported.
9	Restart SGMII Auto-Negotiation	R/W, SC	0x0	SC	Auto-Negotiation automatically restarts after hardware reset, software reset (4.0x8000.15), or a change in Auto-Negotiation enable (4.0x8000.12), regardless of whether the restart bit (4.0x8000.9) is set. The bit is set when Auto-Negotiation is enabled or disabled in 4.0x8000.12. 1 = Restart the Auto-Negotiation Process. 0 = Normal operation

Table 297: SGMII Control Register (Continued)
Device 4, Register 0x8000

Bits	Field	Mode	HW Rst	SW Rst	Description
8	Duplex Mode	R/W	0x1	Retain	Writing this bit has no effect unless one of the following events occurs: • A software reset is asserted (register 4.0x8000.15). • A Restart Auto-Negotiation is asserted (register 4.0x8000.9). • An Auto-Negotiation Enable changes (register 4.0x8000.12). • A power down (register 4.0x8000.11) transitions from power down to normal operation. 1 = Full duplex 0 = Half duplex
7	Collision Test	RO	0x0	0x0	This bit has no effect.
6	Speed Selection (MSB)	RO, R/W	0x1	Retain	If register 4.8010.1:0 (MODE[1:0]) = 01 (1000BASE-X mode) then this bit is always 1. If register 4.8010.1:0 (MODE[1:0]) = 10 (SGMII mode) then this bit is 1 when the PHY is at 1000 Mbps, else it is 0. This bit is undefined if register 4.8010.1:0 (MODE[1:0]) = 00 or 11.
5:0	Reserved	RO	Always 0x00	Always 0x00	This must be 0.

Table 298: SGMII Status Register
Device 4, Register 0x8001

Bits	Field	Mode	HW Rst	SW Rst	Description
15	100BASE-T4	RO	Always 0x0	Always 0x0	0 = The PHY is not able to perform 100BASE-T4.
14	100BASE-X Full Duplex	RO	Always 0x0	Always 0x0	0 = The PHY is not able to perform full-duplex 100BASE-X.
13	100BASE-X Half Duplex	RO	Always 0x0	Always 0x0	0 = The PHY is not able to perform half-duplex 100BASE-X.
12	10 Mbps Full Duplex	RO	Always 0x0	Always 0x0	0 = The PHY is not able to perform full-duplex 10BASE-T.
11	10 Mbps Half Duplex	RO	Always 0x0	Always 0x0	0 = The PHY is not able to perform half-duplex 10BASE-T.
10	100BASE-T2 Full Duplex	RO	Always 0x0	Always 0x0	0 = The PHY is not able to perform full-duplex 100BASE-T2.
9	100BASE-T2 Half Duplex	RO	Always 0x0	Always 0x0	0 = The PHY is not able to perform half-duplex 100BASE-T2.
8	Extended Status	RO	Always 0x1	Always 0x1	1 = Extended status information in register 4.800F
7	Reserved	RO	Always 0x0	Always 0x0	This must be 0.

Table 298: SGMII Status Register (Continued)
Device 4, Register 0x8001

Bits	Field	Mode	HW Rst	SW Rst	Description
6	MF Preamble Suppression	RO	Always 0x1	Always 0x1	1 = The PHY accepts management frames with preamble suppressed.
5	SGMII Auto-Negotiation Complete	RO	0x0	0x0	1 = The Auto-Negotiation process is complete. 0 = The Auto-Negotiation process is not complete. This bit is not set when link is up because of SGMII Auto-Negotiation Bypass or if Auto-Negotiation is disabled.
4	SGMII Remote Fault	RO, LH	Always 0x0	Always 0x0	1 = A remote fault condition is detected. 0 = A remote fault condition is not detected. This bit is always 0 in SGMII mode.
3	Auto-Negotiation Ability	RO	0x1	0x1	1 = The PHY is able to perform Auto-Negotiation. 0 = The PHY is not able to perform Auto-Negotiation.
2	SGMII Link Status	RO, LL	0x0	0x0	This register bit indicates when link was lost since the last read. For the current link status, either read this register back-to-back or read register 4.0x8011.10 Link Real Time. 1 = The link is up. 0 = The link is down.
1	Reserved	RO, LH	Always 0x0	Always 0x0	This must be 0.
0	Extended Capability	RO	Always 0x1	Always 0x1	1 = Extended register capabilities

Table 299: PHY Identifier Register 1
Device 4, Register 0x8002

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Organizationally Unique Identifier Bit 3:18	RO	0x002B	0x002B	The BRIGHTLANE™ OUI is 00:0A:C2. 0000 0000 0000 1010 1100 0010 ^ ^ bit 1.....bit 24 Register 2.[15:0] shows bits 3 to 18 of the OUI. 0000_0000_0010_1011 ^ ^ bit 3.....bit 18

Table 300: SGMII Auto-Negotiation Advertisement Register Device 4, Register 0x8004

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following occurs: A software reset is asserted (register 4.8000.15). Restart Auto-Negotiation is asserted (register 4.8000.9). Power down (register 4.8000.11) transitions from power down to normal operation. A link goes down. 1 = Advertise 0 = Not advertised
14	Reserved	RO	Always 0x0	Always 0x0	This is always 0.
13:12	Remote Fault 2/ Remote Fault 1	R/W	0x0	Retain	A write to this register bit does not take effect until any one of the following also occurs A software reset is asserted (register 4.8000.15). A Restart Auto-Negotiation is asserted (register 4.8000.9). Power down (register 4.8000.11) transitions from power down to normal operation A link goes down. The device has no ability to detect remote fault. 00 = No error, link OK (default) 01 = Link Failure 10 = Offline 11 = Auto-Negotiation Error
11:9	Reserved	RO	3'b000	3'b000	This is always set to 000.
8:7	Pause	R/W	See Description.	See Description.	A write to this register bit does not take effect until any one of the following also occurs: A software reset is asserted (register 4.8000.15). A Restart Auto-Negotiation is asserted (register 4.8000.9). Power down (register 4.8000.11) transitions from power down to normal operation A link goes down. 00 = No PAUSE 01 = Symmetric PAUSE 10 = Asymmetric PAUSE toward link partner 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward local device.
6	1000BASE-X Half Duplex	R/W	See Description.	See Description.	A write to this register bit does not take effect until any one of the following also occurs: A software reset is asserted (register 4.8000.15). A Restart Auto-Negotiation is asserted (register 4.8000.9). Power down (register 4.8000.11) transitions from power down to normal operation A link goes down. 1 = Advertise 0 = Not advertised

Table 300: SGMII Auto-Negotiation Advertisement Register (Continued)
Device 4, Register 0x8004

Bits	Field	Mode	HW Rst	SW Rst	Description
5	1000BASE-X Full Duplex	R/W	0x1	Retain	A write to this register bit does not take effect until any one of the following also occurs: A software reset is asserted (register 4.8000.15). A Restart Auto-Negotiation is asserted (register 4.8000.9) Power down (register 4.8000.11) transitions from power down to normal operation A link goes down. 1 = Advertise 0 = Not advertised
4:0	Reserved	R/W	0x00	0x00	Reserved bit is R/W to allow for forward compatibility with future IEEE standards.

Table 301: SGMII Link Partner Ability/SGMII Register Device 4, Register 0x8005

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	The register bit is cleared when the link goes down and loaded when a base page is received. Received Code Word Bit 15 1 = The link partner is capable of next page. 0 = The link partner is not capable of next page.
14	Acknowledge	RO	0x0	0x0	The register bit is cleared when the link goes down and loaded when a base page is received. Acknowledge Received Code Word Bit 14 1 = The link partner has received link code word. 0 = The link partner has not received link code word.
13:12	Remote Fault 2/ Remote Fault 1	RO	0x0	0x0	The register bit is cleared when the link goes down and loaded when a base page is received. Received Code Word Bit 13:12 00 = No error, link OK (default) 01 = Link Failure 10 = Offline 11 = Auto-Negotiation Error
11:9	Reserved	RO	0x0	0x0	The register bit is cleared when the link goes down and loaded when a base page is received. Received Code Word Bit 11:9
8:7	Asymmetric Pause	RO	0x0	0x0	The register bit is cleared when the link goes down and loaded when a base page is received. Received Code Word Bit 8:7 00 = No PAUSE 01 = Symmetric PAUSE 10 = Asymmetric PAUSE toward the link partner 11 = Both Symmetric PAUSE and Asymmetric PAUSE toward the local device.
6	1000BASE-X Half Duplex	R/W	0x0	0x0	The register bit is cleared when the link goes down and loaded when a base page is received. Received Code Word bit 6 1 = The link partner is capable of 1000BASE-X half duplex. 0 = The link partner is not capable of 1000BASE-X half duplex
5	1000BASE-X Full Duplex	RO	0x0	0x0	The register bit is cleared when the link goes down and loaded when a base page is received. Received Code Word bit 5 1 = The link partner is capable of 1000BASE-X full duplex. 0 = The link partner is not capable of 1000BASE-X full duplex.
4:0	Reserved	RO	0x00	0x00	The register bit is cleared when the link goes down and loaded when a base page is received. Received Code Word Bits 4:0 are always 0.

Table 302: SGMII Auto-Negotiation Expansion Register Device 4, Register 0x8006

Bits	Field	Mode	HW Rst	SW Rst	Description
15:4	Reserved	RO	0x000	0x000	This must be 00000000000.
3	Link Partner Next Page Able	RO	0x0	0x0	In SGMII mode, this bit is always 0. In 1000BASE-X mode, register 4.8006.3 is set when a base page is received and the received link control word has bit 15 set to 1. This bit is cleared when the link goes down. 1 = The link partner is Next Page able. 0 = The link partner is not Next Page able.
2	Local Next Page Able	RO	Always 0x1	Always 0x1	1 = The local device is Next Page able.
1	Page Received	RO, LH	0x0	0x0	Register 4.8006.1 is set when a valid page is received. 1 = A new page has been received. 0 = A new page has not been received.
0	Link Partner Auto-Negotiation Able	RO	0x0	0x0	This bit is set when there is sync status, the SERDES receiver has received three non-zero matching valid configuration code groups, and Auto-Negotiation is enabled in register 4.8000.12. 1 = The link partner is Auto-Negotiation able. 0 = The link partner is not Auto-Negotiation able.

Table 303: SGMII Next Page Transmit Register Device 4, Register 0x8007

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	R/W	0x0	0x0	A write to this register implicitly sets a variable in the Auto-Negotiation state machine indicating that the next page has been loaded. This register only has effect in 1000BASE-X mode. Transmit Code Word Bit 15
14	Reserved	RO	0x0	0x0	Transmit Code Word Bit 14
13	Message Page	R/W	0x0	0x0	Transmit Code Word Bit 13
12	Acknowledge2	R/W	0x0	0x0	Transmit Code Word Bit 12
11	Toggle	RO	0x0	0x0	Transmit Code Word Bit 11 This bit is internally set to the opposite value each time a page is received.
10:0	Message/Unformatted Field	R/W	0x001	0x001	Transmit Code Word Bit 10:0

Table 304: SGMII Link Partner Register Device 4, Register 0x8008

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Next Page	RO	0x0	0x0	This register only has effect in 1000BASE-X mode. The register is loaded only when a next page is received from the link partner. It is cleared each time the link goes down. Received Code Word Bit 15
14	Acknowledge	RO	0x0	0x0	Received Code Word Bit 14
13	Message Page	RO	0x0	0x0	Received Code Word Bit 13
12	Acknowledge2	RO	0x0	0x0	Received Code Word Bit 12
11	Toggle	RO	0x0	0x0	Received Code Word Bit 11
10:0	Message/Unformatted Field	RO	0x000	0x000	Received Code Word Bit 10:0

Table 305: SGMII SERDES Specific Control 1 Register Device 4, Register 0x8010

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	SERDES Transmit FIFO Depth	R/W	0x1	Retain	00 = This supports 2 KB at ±100 ppm. 01 = This supports 10 KB at ±100 ppm. 10 = This supports 18 KB at ±100 ppm. 11 = This supports 27 KB at ±100 ppm.
13	Block Carrier Extension Bit	R/W	0x0	Retain	The carrier extension and carrier extension with errors are converted to idle symbols on the RXD only during full-duplex mode. 1 = Enable block carrier extension. 0 = Disable block carrier extension.
12	SERDES Loopback	R/W	0x0	Retain	Register 4.8010.8 selects the line loopback path. 1 = Enable loopback from SERDES input to SERDES output. 0 = Normal operation
11	Assert CRS on Transmit	R/W	0x0	Retain	This bit has no effect in full-duplex mode. 1 = Assert on transmit. 0 = Never assert on transmit.
10	Force Link Good	R/W	0x0	Retain	If the link is forced to be good, then the link state machine is bypassed and the link is always up. 1 = The force link is good. 0 = Normal operation
9	Reserved	R/W	0x0	Retain	Set to 0.
8	SERDES Loopback Type	R/W	0x0	Retain	0 = Loopback through PCS (Tx and Rx can be asynchronous) 1 = Loopback raw 10-bit data (Tx and Rx must be synchronous)
7:6	Reserved	R/W	0x0	Retain	Set to 0.

Table 305: SGMII SERDES Specific Control 1 Register (Continued)
Device 4, Register 0x8010

Bits	Field	Mode	HW Rst	SW Rst	Description
5	Infineon Remote Fault Indication Enable	R/W	0x0	Retain	0 = Disable 1 = Enable, Remote Fault is indicated to the link partner in less than 2 ms, only one bit of bit 5:4 can be set to 1.
4	IEEE Remote Fault Indication Enable	R/W	0x0	Retain	0 = Disable 1 = Enable, Remote Fault is indicated to link partner after 20 ms according to IEEE standard, only one bit of bit 5:4 can be set to 1.
3:2	Reserved	R/W	0x1	Retain	This must be set to 1.
1:0	Mode	R/W	0x02	See Description.	The following modes of operation are supported: 00 = Reserved 01 = 1000BASE-X mode 10 = SGMII System mode 11 = Reserved

Table 306: SGMII Extended Status Register
Device 4, Register 0x800F

Bits	Field	Mode	HW Rst	SW Rst	Description
15	1000BASE-X Full Duplex	RO	0x1	0x1	1 = This is 1000BASE-X full-duplex capable. 0 = This is not 1000BASE-X full-duplex capable.
14	1000BASE-X Half Duplex	RO	0x1	0x1	1 = This is 1000BASE-X half-duplex capable. 0 = This is not 1000BASE-X half-duplex capable.
13	1000BASE-T Full Duplex	RO	0x0	0x0	0 = This is not 1000BASE-T full-duplex capable.
12	1000BASE-T Half Duplex	RO	0x0	0x0	0 = This is not 1000BASE-T half-duplex capable.
11:0	Reserved	RO	0x000	0x000	

Table 307: SGMII Specific Status Register
Device 4, Register 0x8011

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	Speed	RO	0x0	Retain	These status bits are valid only after resolved bit 4.0x8011.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 11 = Reserved 10 = 1000 Mbps 01 = 100 Mbps 00 = Reserved
13	Duplex	RO	0x0	Retain	This status bit is valid only after resolved bit 4.0x8011.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Full duplex 0 = Half duplex

Table 307: SGMII Specific Status Register (Continued)
Device 4, Register 0x8011

Bits	Field	Mode	HW Rst	SW Rst	Description
12	Page Received	RO	Always 0x0	Always 0x0	1 = Page is received. 0 = Page is not received.
11	Speed and Duplex Resolved	RO	0x0	0x0	When Auto-Negotiation is not enabled, this bit is always 1. 1 = This is resolved. 0 = This is not resolved.
10	Link (real time)	RO	0x0	0x0	1 = The link is up. 0 = The link is down.
9:8	Reserved	RO	Always 0x0	Always 0x0	This must be0x0.
7:6	Remote Fault Received	RO, LH	0x0	0x0	The mapping for this status is as follows: 00 = No fault has been detected. 01 = A link failure has been detected at the link partner. 10 = Offline 11 = Auto-Negotiation Error
5	Sync Status	RO	0x0	0x0	1 = Sync status 0 = No sync status
4	SGMII Energy Detect	RO	0x1	0x1	1 = No energy detected. 0 = Energy detected.
3	Transmit Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 4.8011.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Transmit pause is enabled. 0 = Transmit pause is disable.
2	Receive Pause Enabled	RO	0x0	0x0	This is a reflection of the MAC pause resolution. This bit is for information purposes and is not used by the device. This status bit is valid only after resolved bit 4.8011.11 = 1. The resolved bit is set when Auto-Negotiation is completed or Auto-Negotiation is disabled. 1 = Receive pause is enabled. 0 = Receive pause is disabled.
1:0	Reserved	RO	0x0	0x0	This must be 0x0.

Table 308: SGMII Interrupt Enable Register Device 4, Register 0x8012

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Reserved	RO	Always 0x0	Always 0x0	
14	Speed Changed Interrupt Enable	R/W	0x0	Retain	1 = The interrupt is enabled. 0 = The interrupt is disabled.
13	Duplex Changed Interrupt Enable	R/W	0x0	Retain	1 = The interrupt is enabled. 0 = The interrupt is disabled.
12	Page Received Interrupt Enable	R/W	0x0	Retain	1 = The interrupt is enabled. 0 = The interrupt is disabled.
11	Auto-Negotiation Completed Interrupt Enable	R/W	0x0	Retain	1 = The interrupt is enabled. 0 = The interrupt is disabled.
10	Link Status Changed Interrupt Enable	R/W	0x0	Retain	1 = The interrupt is enabled. 0 = The interrupt is disabled.
9	Symbol Error Interrupt Enable	R/W	0x0	Retain	1 = The interrupt is enabled. 0 = The interrupt is disabled.
8	False Carrier Interrupt Enable	R/W	0x0	Retain	1 = The interrupt is enabled. 0 = The interrupt is disabled.
7	FIFO Error Interrupt Enable	R/W	0x0	Retain	1 = The interrupt is enabled. 0 = The interrupt is disabled.
6	Reserved	RO	Always 0x0	Always 0x0	
5	Remote Fault Receive Interrupt Enable	R/W	0x0	0x0	1 = The interrupt is enabled. 0 = The interrupt is disabled.
4	SGMII Energy Detect Interrupt Enable	R/W	0x0	Retain	1 = The interrupt is enabled. 0 = The interrupt is disabled.
3:0	Reserved	RO	Always 0x0	Always 0x0	

Table 309: SGMII Interrupt Status Register Device 4, Register 0x8013

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	Reserved	RO	Always 0x0	Always 0x0	This must be 0.
12	Page Received	RO, LH	0x0	0x0	1 = Page is received. 0 = Page is not received.
11	Auto-Negotiation Completed	RO, LH	0x0	0x0	1 = Auto-Negotiation is completed. 0 = Auto-Negotiation is not completed.
10	Link Status Changed	RO, LH	0x0	0x0	1 = Link status has changed. 0 = Link status has not changed.
9	Symbol Error	RO, LH	0x0	0x0	1 = There is a symbol error. 0 = There is no symbol error.
8	False Carrier	RO, LH	0x0	0x0	1 = There is a false carrier. 0 = There is no false carrier.
7	FIFO Over/Underflow	RO, LH	0x0	0x0	1 = There is an overflow/underflow error. 0 = There is no FIFO error.
6	Reserved	RO	Always 0x0	Always 0x0	This must be 0.
5	Remote Fault Receive Interrupt Enable	RO, LH	Always 0x0	Always 0x0	1 = A remote fault received changed, read 4.8011.7:6 for details. 0 = No change on remote fault has been received.
4	SGMII Energy Detect Changed	RO, LH	0x0	0x0	1 = The Energy Detect state has changed. 0 = No Energy Detect state change has been detected.
3:0	Reserved	RO	Always 0x0	Always 0x0	

Table 310: SGMII Receive Error Counter Register Device 4, Register 0x8015

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	Receive Error Count	RO, LH	0x0000	Retain	The counter will peg at 0xFFFF and will not roll over. Both false carrier and symbol errors are reported.

Table 311: PRBS Control Register Device 4, Register 0x8017

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Reserved	R/W	0x00	Retain	Set to 0s.
7	Invert Checker Polarity	R/W	0x0	Retain	0 = Normal 1 = Invert
6	Invert Generator Polarity	R/W	0x0	Retain	0 = Normal 1 = Invert
5	PRBS Lock	R/W	0x0	Retain	0 = The counter runs freely. 1 = Do not start counting until PRBS locks first.
4	Clear Counter	R/W, SC	0x0	0x0	0 = Normal 1 = Clear counter.
3:2	Pattern Select	R/W	0x0	Retain	00 = PRBS 7 01 = PRBS 23 10 = PRBS 31 11 = Generate 1010101010... pattern.
1	PRBS Checker Enable	R/W	0x0	0x0	0 = Disable 1 = Enable
0	PRBS Generator Enable	R/W	0x0	0x0	0 = Disable 1 = Enable

Table 312: PRBS Error Counter LSB Register Device 4, Register 0x8018

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PRBS Error Count LSB	RO	0x0000	Retain	A read to this register freezes register 4.8019. This is cleared only when register 4.8017.4 is set to 1.

Table 313: PRBS Error Counter MSB Register Device 4, Register 0x8019

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PRBS Error Count MSB	RO	0x0000	Retain	These bits do not update unless register 4.8018 is read first. This is cleared only when register 4.8017.4 is set to 1.

Table 314: SGMII Specific Control Register 2
Device 4, Register 0x801A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:7	Reserved	R/W	0x00	0x00	Set to 0s.
6	Serial Interface Auto-Negotiation Bypass Enable	R/W	0x1	Update	Changes to this bit are disruptive to normal operation; so, any changes to these registers must be followed by a software reset to take effect. 1 = Bypass is allowed. 0 = No bypass is allowed.
5	Serial Interface Auto-Negotiation Bypass Status	RO	0x0	0x0	1 = The serial interface link came up because bypass mode timer timed out and SGMII Auto-Negotiation was bypassed. 0 = The serial interface link came up because regular SGMII Auto-Negotiation completed. If this bit is 1, then bit 4.0x8011.11 will be 0.
4	Reserved	R/W	0x0	0x0	Set to 0s.
3	SGMII Transmitter Disable	R/W	0x0	Retain	1 = Transmitter disable 0 = Transmitter enable
2:0	Reserved	R/W	0x2	Retain	

Table 315: Packet Generation
Device 4, Register 0x801C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Packet Burst	R/W	0x0	Retain	0x00 = Continuous 0x01 to 0xFF = Burst 1 to 255 packets
7	Packet Generator Transmit Trigger	R/W	0x0	Retain	This bit is only valid when all of the following are true: bit 6 = 1 bit 3 = 1 bit 15:8 is not equal to all 0s A read of this bit gives the following: 1 = Packet generator transmit done 0 = Packet generator is transmitting data When this bit is 1 a write of 0 will trigger the packet generator to transmit again. When this bit is 0 a write of 0 or 1 will have no effect.
6	Packet Generator Enable Self Clear Control	R/W	0x0	Retain	0 = Bit 3 will self clear after all packets are sent. 1 = Bit 3 will stay high after all packets are sent.
5	Reserved	R/W	0x0	Retain	
4	Enable CRC Checker	R/W	0x0	Retain	1 = Enable 0 = Disable
3	Enable Packet Generator	R/W	0x0	Retain	1 = Enable 0 = Disable
2	Payload of Packet to Transmit	R/W	0x0	Retain	0 = Pseudo-random 1 = 5A,A5,5A,A5,…

Table 315: Packet Generation (Continued)
Device 4, Register 0x801C

Bits	Field	Mode	HW Rst	SW Rst	Description
1	Length of Packet to Transmit	R/W	0x0	Retain	1 = 1518 bytes 0 = 64 bytes
0	Transmit an Errored Packet	R/W	0x0	Retain	1 = Tx packets with CRC errors and symbol error 0 = No error

Table 316: CRC Counters
Device 4, Register 0x801D

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	Packet Count	RO	0x00	Retain	0x00 = No packets have been received. 0xFF = 256 packets are received (maximum count). Bit 4.801C.4 must be set to 1 for the register to be valid.
7:0	CRC Error Count	RO	0x00	Retain	0x00 = No CRC errors were detected in the packets received. 0xFF = 256 CRC errors were detected in the packets received (maximum count). Bit 4.801C.4 must be set to 1 for the register to be valid.

Table 317: Checker Control
Device 4, Register 0x801E

Bits	Field	Mode	HW Rst	SW Rst	Description
15:5	Reserved	R/W	0x000	Retain	
4	CRC Counter Reset	R/W, SC	0x0	Retain	1 = Reset This bit will self-clear after writing 1.
3:0	Reserved	R/W	0x0	Retain	

Table 318: Packet Generation 2
Device 4, Register 0x801F

Bits	Field	Mode	HW Rst	SW Rst	Description
15	Constant Packet Payload Enable	R/W	0x0	Retain	This enables a constant payload for packets generated by the packet generator. 1 = Enable constant packet payload. 0 = Use other payload options.
14	Constant Packet Payload Type	R/W	0x0	Retain	This bit selects the type of constant payload to use and is valid only when 4.801F.15 = 1. 1 = Use all 1s packet payload. 0 = Use all 0s packet payload.
13:8	Reserved	R/W	0x00	Retain	
7:0	IPG Length	R/W	0x0B	Retain	The number in bit [7:0]+1 is the number of bytes for IPG.

3.10 PTP Registers

Table 319: Summary Register Map for PTP Registers

Register Name	Register Address	Table and Page
PTP CTRL0	Device 0x1F, Register 0xA000	Table 320, p. 243
PTP CTRL1	Device 0x1F, Register 0xA001	Table 321, p. 243
PTP_MAC_ADDR0	Device 0x1F, Register 0xA002	Table 321, p. 243
PTP_MAC_ADDR1	Device 0x1F, Register 0xA003	Table 322, p. 243
PTP_MAC_ADDR2	Device 0x1F, Register 0xA004	Table 323, p. 244
PTP Port Config Register 1	Device 0x1F, Register 0xA800	Table 325, p. 244
PTP Port Config Register 2	Device 0x1F, Register 0xA801	Table 326, p. 248
PTP Port Config Register 3	Device 0x1F, Register 0xA802	Table 327, p. 250
PTP Port Config Register 4	Device 0x1F, Register 0xA803	Table 328, p. 252
PTP Port Config Register 5	Device 0x1F, Register 0xA807	Table 329, p. 253
PTP Port Status Register 22	Device 0x1F, Register 0xA808	Table 330, p. 254
PTP Port Status Register 23	Device 0x1F, Register 0xA809	Table 331, p. 255
PTP Port Status Register 24	Device 0x1F, Register 0xA80A	Table 332, p. 256
PTP Port Status Register 25	Device 0x1F, Register 0xA80B	Table 333, p. 256
PTP Port Status Register 26	Device 0x1F, Register 0xA80C	Table 334, p. 257
PTP Port Status Register 27	Device 0x1F, Register 0xA80D	Table 335, p. 258
PTP Port Status Register 28	Device 0x1F, Register 0xA80E	Table 336, p. 259
PTP Port Status Register 29	Device 0x1F, Register 0xA80F	Table 337, p. 259
PTP Port Status Register 30	Device 0x1F, Register 0xA810	Table 338, p. 260
PTP Port Status Register 31	Device 0x1F, Register 0xA811	Table 339, p. 261
PTP Port Status Register 32	Device 0x1F, Register 0xA812	Table 340, p. 262
PTP Port Status Register 33	Device 0x1F, Register 0xA813	Table 341, p. 262
PTP Port Status Register 34	Device 0x1F, Register 0xA814	Table 342, p. 262
PTP Port Status Register 35	Device 0x1F, Register 0xA815	Table 343, p. 263
ReadPlus Command Register – PTP Global	Device 0x1F, Register 0xA86E	Table 344, p. 264
ReadPlus Data Register – PTP Global	Device 0x1F, Register 0xA86F	Table 345, p. 264
Ingress Mean Path Delay 36	Device 0x1F, Register 0xA81C	Table 346, p. 264
Ingress Path Delay Asymmetry 37	Device 0x1F, Register 0xA81D	Table 347, p. 265
Egress Path Delay Asymmetry 38	Device 0x1F, Register 0xA81E	Table 348, p. 265
TAI Global Config 22	Device 0x1F, Register 0xA840	Table 349, p. 266
TAI Global Config 23	Device 0x1F, Register 0xA841	Table 350, p. 272
TAI Global Config 24	Device 0x1F, Register 0xA842	Table 351, p. 273
TAI Global Config 25	Device 0x1F, Register 0xA843	Table 352, p. 274
TAI Global Config 26	Device 0x1F, Register 0xA844	Table 353, p. 274
TAI Global Config 27	Device 0x1F, Register 0xA845	Table 354, p. 275
TAI Global Config 28	Device 0x1F, Register 0xA846	Table 355, p. 276
TAI Global Config 29	Device 0x1F, Register 0xA847	Table 356, p. 277

Table 319: Summary Register Map for PTP Registers (Continued)

Register Name	Register Address	Table and Page
TAI Global Config 30	Device 0x1F, Register 0xA848	Table 357, p. 278
TAI Global Status 31	Device 0x1F, Register 0xA849	Table 358, p. 278
TAI Global Status 32	Device 0x1F, Register 0xA84A	Table 359, p. 280
TAI Global Status 33	Device 0x1F, Register 0xA84B	Table 360, p. 280
TAI Global Config 1	Device 0x1F, Register 0xA84C	Table 361, p. 281
TAI Global Config 2	Device 0x1F, Register 0xA84E	Table 362, p. 281
TAI Global Config 3	Device 0x1F, Register 0xA84F	Table 363, p. 281
TAI Global Config 4	Device 0x1F, Register 0xA850	Table 364, p. 282
TAI Global Config 5	Device 0x1F, Register 0xA851	Table 365, p. 282
TAI Global Config 6	Device 0x1F, Register 0xA852	Table 366, p. 283
TAI Global Config 7	Device 0x1F, Register 0xA853	Table 367, p. 284
TAI Global Config 8	Device 0x1F, Register 0xA854	Table 368, p. 284
TAI Global Config 9	Device 0x1F, Register 0xA855	Table 369, p. 284
TAI Global Config 10	Device 0x1F, Register 0xA856	Table 370, p. 285
PTP Global Time Array 11	Device 0x1F, Register 0xA857	Table 371, p. 285
TAI Global Config 12	Device 0x1F, Register 0xA85E	Table 372, p. 286
TAI Global Config 13	Device 0x1F, Register 0xA85F	Table 373, p. 287
PTP Global Config 39	Device 0x1F, Register 0xA860	Table 374, p. 287
PTP Global Config 40	Device 0x1F, Register 0xA861	Table 375, p. 288
PTP Global Config 41	Device 0x1F, Register 0xA862	Table 376, p. 288
PTP Global Config 42	Device 0x1F, Register 0xA867	Table 377, p. 289
PTP Status 5	Device 0x1F, Register 0xA868	Table 378, p. 290
PTP Global Status 6	Device 0x1F, Register 0xA869	Table 379, p. 291
PTP Global Time Array 7	Device 0x1F, Register 0xA870	Table 380, p. 291
PTP Global Time Array 8	Device 0x1F, Register 0xA871	Table 381, p. 292
PTP Global Time Array 9	Device 0x1F, Register 0xA872	Table 382, p. 292
PTP Global Time Array 10	Device 0x1F, Register 0xA873	Table 383, p. 293
PTP Global Time Array 11	Device 0x1F, Register 0xA874	Table 384, p. 293
PTP Global Time Array 12	Device 0x1F, Register 0xA875	Table 385, p. 294
PTP Global Time Array 13	Device 0x1F, Register 0xA876	Table 386, p. 294
PTP Global Time Array 14	Device 0x1F, Register 0xA877	Table 387, p. 294
PTP Global Time Array 15	Device 0x1F, Register 0xA878	Table 388, p. 295
PTP Global Time Array 16	Device 0x1F, Register 0xA879	Table 389, p. 295
PTP Global Time Array 17	Device 0x1F, Register 0xA87A	Table 390, p. 295
PTP Global Time Array 18	Device 0x1F, Register 0xA87B	Table 391, p. 296
PTP Global Time Array 19	Device 0x1F, Register 0xA87C	Table 392, p. 296
PTP Global Time Array 20	Device 0x1F, Register 0xA87D	Table 393, p. 297
PTP Global Time Array 21	Device 0x1F, Register 0xA87E	Table 394, p. 297

Table 320: PTP CTRL0
Device 0x1F, Register 0xA000

Bits	Field	Mode	HW Reset	SW Reset	Description
15:14	JUMBO_MODE	R/W	0x0	NA	Define PTP JUMBO_MODE pins.
13	CHK_PREAM	R/W	0x1	NA	Define PTP CHK_PREAM pin.
12	IGR_PREEMPT_EN	R/W	0x1	NA	Define PTP IGR_PREEMPT_EN pin.
11	KEEP_S_AFT_D	R/W	0x0	NA	Define PTP KEEP_S_AFT_D pin.
10:9	TCAM_MODE	R/W	0x0	NA	Define PTP TCAM_MODE[1:0] pins.
8	PORT_SPEED_OW	R/W	0x0	NA	When set, PTP port_speed[2:0] and alt_speed pins are overwritten by this register.
7:5	PORT_SPEED	R/W	0x0	NA	port_speed[2:0] overwrite
4	ALT_SPEED	R/W	0x0	NA	alt_speed pin overwrite
3:0	RESERVED	R/W	0x00	NA	Reserved

Table 321: PTP CTRL1
Device 0x1F, Register 0xA001

Bits	Field	Mode	HW Reset	SW Reset	Description
15	REDUCE_PTP	R/W	0x0	NA	Define PTP reduce_ptp pin.
14	PHY_ACTIVE	R/W	0x0	NA	Define PTP phy_active pin.
13	TEST_SPEEDUP	R/W	0x0	NA	Define PTP test_speedup pin.
12	ONE_STEP_EN	R/W	0x1	NA	Define PTP one_step_enable pin.
11:10	UNUSED	RO	0x0	NA	
9	REDUCE_PTP_TS	R/W	0x0	NA	Define PTP reduce_ptp_ts pin.
8	REDUCE_PTP_1588	R/W	0x0	NA	Define PTP reduce_ptp_1588 pin.
7:0	UNUSED	RO	0x00	NA	

Table 322: PTP_MAC_ADDR0
Device 0x1F, Register 0xA002

Bits	Field	Mode	HW Reset	SW Reset	Description
15:0	MAC_ADDR	R/W	0x00	NA	Define PTP mac_addr[15:0]

Table 323: PTP_MAC_ADDR1
Device 0x1F, Register 0xA003

Bits	Field	Mode	HW Reset	SW Reset	Description
15:0	MAC_ADDR	R/W	0x00	NA	Define PTP mac_addr[31:16]

Table 324: PTP_MAC_ADDR2
Device 0x1F, Register 0xA004

Bits	Field	Mode	HW Reset	SW Reset	Description
15:0	MAC_ADDR	R/W	0x00	NA	Define PTP mac_addr[47:32]

Table 325: PTP Port Config Register 1
Device 0x1F, Register 0xA800

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	TRANSSPEC	R/W	0x0	0x0	PTP Transport Specific value. The Transport Specific bits present in PTP Common header are used to differentiate between IEEE 1588, IEEE 802.1AS, and so on, frames. This is to differentiate between various timing protocols running on either Layer2 or higher protocol layers. In addition to comparing the EtherType to determine that the incoming frame is a PTP frame, the TransSpec bits are compared to the incoming PTP common headers Transport Specific bits. If there is a match, then hardware logic time stamps the frames indicated by MsgTypeEn and optionally interrupts the CPU. If there is no match and Transport Spec checking is enabled (see DisTSpecCheck bit below), then the hardware will not perform any operations in the PTP core. For IEEE 1588 networks, this is expected to be configured to a 0x0 and for IEEE 802.1AS networks this is expected to be configured to 0x1. **NOTE:** The only valid TransSpec values for PTP hardware acceleration (PTP Port offset 0x02) are 0x0 and 0x1.

Table 325: PTP Port Config Register 1 (Continued)
Device 0x1F, Register 0xA800

Bits	Field	Mode	HW Rst	SW Rst	Description
11	DISTSPECCHECK	R/W	0x0	0x0	Disable Transport Specific Check. 0 = Enable checking for Transport Spec. 1 = Disable checking for Transport Spec. When this bit is cleared to a zero, the Transport Spec part of the PTP Common header of incoming frames must match the configured TransSpec (above) for time stamping to occur (PTP hardware accelerated or not accelerated). This setting limits PTP time stamping to frames containing a TransSpec value that matches the value in the TransSpec register above. This allows time stamping to be limited to only IEEE 1588 or to only IEEE 802.1AS per their frame's Transport Specs (assuming their value is contained in the TransSpec register above). When this bit is set to a one, the Transport Spec checking of the PTP frames is not performed before time stamping occurs. This setting allows PTP time stamping for all TransSpec values (although PTP hardware acceleration, PTP Port offset 0x02, only functions on IEEE 1588 and IEEE 802.1AS TransSpec values).
10	PTPMACSECEN	R/W	0x0	0x0	PTP MACsec Support Enable 0 = Disable PTP MACsec support. 1 = Enable PTP MACsec support. When this bit is set to a one, PTP will process MACsec-tagged PTP frames and automatically skip the MACsec tag to continue processing. When this bit is cleared to a zero, PTP will not process MACsec-tagged PTP frames. **NOTE:** When PTP MACsec support is enabled, PTP only supports basic timestamping in register function, hardware acceleration and timestamp insertion are not supported. When PTP MACsec support is disabled, PTP will use registers ETJump and IPJump below to continue processing.
9	PREEMPTIONTIMESTAMP	R/W	0x0	0x0	Preemption Timestamp select This register is used to select if timestamp group (PTP Port Register offset 0x8 – 0x13) is from express frames or preemption frames as follows: 0 = Select express frame timestamp group. 1 = Select preemption frame timestamp group. **NOTE:** In the future when register is extended to 32 bits, expand this index register to assign dedicated preemption timestamp register space.
8	ONESTEPSYNC	R/W	0x0	0x0	One Step on Sync frames only. 0 = When OneStep is enabled, it is enabled for all appropriate frames. 1 = When OneStep is enabled, it is enabled for Sync frames only. When OneStep is enabled (Index 0x00) this bit determines which frame types support OneStep operation. This bit supports IEEE 802.1AS-Rev where one step is supported on Sync frames only. **NOTE:** Changing the value contained in this field will cause the PTP Action Vectors (PTP Port Config Register Index 0x07) for all Time Domains to be reset to their default settings for the selected PTP Mode and can only occur when a port is in the Disabled Port State (Port Offset 0x04).

Table 325: PTP Port Config Register 1 (Continued)
Device 0x1F, Register 0xA800

Bits	Field	Mode	HW Rst	SW Rst	Description
7	ONESTEPEGRESS	R/W	0x0	0x0	OneStep Enable for Egress. Supported on devices that support OneStep ONLY! (see Note!) This bit is used to enable hardware OneStep support for Egress PTP frames in the mode selected by the PTPMode bits below as follows: 0 = Hardware accelerate using AutoFollowUp Two Step frame formats. 1 = Hardware accelerate using OneStep frame formats. **NOTE:** This device does not support the receiving of One Step frames and the hardware conversion of these frames into Two Step when the PTPMode is End to End Transparent Clock. **NOTE:** This bit must not be able to be set to a one on One-Step disabled devices (OneStepEnable is a pad bond option or fuse that can disable One-Step support), for example, hardware must prevent this bit from being set to a one when the OneStepEnable bond pad or fuse is grounded/blown. **NOTE:** Changing the value contained in this field will cause the PTP Action Vectors (PTP Port Config Register Index 0x07) for all Time Domains to be reset to their default settings for the selected PTP Mode and can only occur when a port is in the Disabled Port State (Port Offset 0x04).
6	ONESTEPINGRESS	R/W	0x0	0x0	OneStep Enable for Ingress. Supported on devices that support 1-Step ONLY (see Note). This bit is used to enable hardware One Step support for Ingress PTP frames in the mode selected by the PTPMode bits below as follows: 0 = Hardware accelerate using AutoFollowUp Two Step frame formats. 1 = Hardware accelerate using One Step frame formats. **NOTE:** This device does not support the receiving of One Step frames and the hardware conversion of these frames into Two Step when the PTPMode is End to End Transparent Clock. **NOTE:** This bit must not be able to be set to a one on One-Step disabled devices (OneStepEnable is a pad bond option or fuse that can disable One-Step support), for example, hardware must prevent this bit from being set to a one when the OneStepEnable bond pad or fuse is grounded/blown. **NOTE:** Changing the value contained in this field will cause the PTP Action Vectors (PTP Port Config Register Index 0x07) for all Time Domains to be reset to their default settings for the selected PTP Mode and can only occur when a port is in the Disabled Port State (Port Offset 0x04).
5	PTPMIRRORMODE	R/W	0x0	0x0	Mirror Mode for pass-through PTP frames This bit is used when the CPU must acquire a copy of pass-through PTP frames. 0 = Ingress PTP frames passed through the switch will only be directed to hardware acceleration enabled ports. 1 = Ingress PTP frames passed through the switch will be directed to hardware acceleration enabled ports and also mirrored to CPU ports set by PTPDest.

Table 325: PTP Port Config Register 1 (Continued)
Device 0x1F, Register 0xA800

Bits	Field	Mode	HW Rst	SW Rst	Description
4	TSFORMAT	R/W	0x0	0x0	Time Stamp Format 0x0 = Timestamp in 32-bit global timer 0x1 = Timestamp in 32-bit 2-sec ToD or 1722 This bit is valid only when HWAccel = 1(PTP Port Config Register offset 0x02 bit 6) and is used to choose which timestamp format to put in arrival (PTP Port Config Register offset 0x09 - 0x0A and PTP Port Config Register offset 0x0D - 0x0E) or departure (PTP Port Config Register offset 0x11 - 0x12) timestamp register. When this bit is set to 1 and hardware acceleration is enabled, time stamp format is 32-bit 2-sec ToD or 1722 is selected by the register IntPTPTime (PTP Global Offset 0x07, index01, bit 6).
3:2	PTPPREEMPTCTRL	R/W	0x0	0x0	PTP Preemption Control 0x0 = Only process the express PTP frames. 0x1 = Only process the preemptable PTP frame. 0x2 = Process both express and preemptable PTP frames. 0x3 = Reserved This register is valid when switch preemption is enabled. On the ingress side, it's enabled by register “Preempt Enable”, switch port register offset 0x15 bit 10); on the egress side, it is enabled when register “Preempt Queue” (switch port register offset 0x15 bit 0 - 7) is not 0x0.
1	DISTSOVERWRITE	R/W	0x0	0x0	Disable Time Stamp Counter Overwriting. 0 = Overwrite unread Time Stamps in the registers with new data. 1 = Keep unread Time Stamps in the registers until read. When this bit is cleared to a zero, PTPArr0Time, PTPArr1Time, PTPDepTime values get overwritten even though their corresponding valid bits (defined in PTP Port Status Data Structure below), are not cleared. When this bit is set to one, PTPArr0Time, PTPArr1Time, PTPDepTime values do not get overwritten with new time stamps until their corresponding valid bits (defined in PTP Port Status Data Structure below), are cleared.
0	DISPTP	R/W	0x0	0x0	Disable Precise Time Stamp logic. 0 = PTP logic on this port is enabled. 1 = PTP logic on this port is disabled. When PTP logic is disabled the hardware does not recognize or timestamp PTP frames. Even interrupt generation logic is disabled. This disable disables all modes of PTP on this port (including PTP hardware acceleration if enabled - PTP Port offset 0x02).Note: PTP should not be enabled on Half Duplex ports when ArrTSMode or HWAccel (PTP Port offset 0x02) are non zero as the timing of CRS and COL are not delayed to keep them lined up with the rest of the frame data.

Table 326: PTP Port Config Register 2
Device 0x1F, Register 0xA801

Bits	Field	Mode	HW Rst	SW Rst	Description
13:8	IPJUMP	R/W	0x0	0x0	Internet Protocol Jump added to ETJump below. Set this register to point to the start of the frame's IP Version byte (802.1Q tagged frames are automatically compensated by ETJump).This field specifies how many bytes to skip starting at the first byte of the frame's EtherType (for example, where ETJump, below, left off) in order to jump to the beginning of the IPv4 or IPv6 headers in the frame. If an IPv4 or IPv6 version is found at this location of the frame, Layer 4 PTP processing occurs from there. This allows flexibility in the hardware to skip past the protocol chains that are specific to customer networks including MPLS, and so on. For example if ETJump is programmed to 0xC and IPJump is programmed to 0x16, this indicates to hardware to skip 0x22 bytes in order to get to the IP header. It can either be IPv4 or IPv6 header. **NOTE:** A value of 0x0 (default), 0x1 and 0x2 is a special case that prevents further frame searching if ETJump did not find a match (for example, a zero value in IPJump prevents the IPJump mechanism from searching further).
7:5	ALTETJUMP	R/W	0x0	0x0	Alternate EtherType Jump for MACsec tagged frames This register specifies how many bytes in the unit of 2 bytes to skip starting from the end of the MACsec tag to get to the Ethertype after MACsec tag. Frames found with an 0x8100 EtherType (802.1Q tag) at this location are automatically searched 4 bytes further into the frame for the next EtherType to compare (this extension is done once). This register is only used when MACsecEn is set to 1. If the PTPEType value (PTP Global offset 0x00) is found as the Ether Type in the frame, Layer 2 PTP processing occurs. If 0x0800 or 0x86DD is found the Layer 4 PTP processing occurs. If none of these values are found, PTP frame decoding is passed to the IPJump field above. This allows flexibility in the hardware to skip past any protocol chains after MACsec tag that are specific to customer networks including DSA-Tag, IEEE 802.1Q tag, Provider tag, and so on.

Table 326: PTP Port Config Register 2 (Continued)
Device 0x1F, Register 0xA801

Bits	Field	Mode	HW Rst	SW Rst	Description
4:0	ETJUMP	R/W	0x0	0x0	EtherType Jump points to the start of the frame's EtherType (assuming it is not 802.1Q tagged). This field specifies how many bytes to skip starting from the start of the MAC-DA of the frame to get to the first byte of the EtherType of the frame. Frames found with an 0x8100 EtherType (802.1Q tag) at this location are automatically searched 4 bytes further into the frame for the next EtherType to compare (this extension is done once). If PTPMACsecEn bit (PTP Port offset 0x00) is set to 1, frames found with an 0x88E5 EtherType (MACsec tag) at this location are automatically skipped to the next EtherType to compare if E and C MACsec flags are both 0. If the PTPEType value (PTP Global offset 0x00) is found as the Ether Type in the frame, Layer 2 PTP processing occurs. If 0x0800 or 0x86DD is found the Layer 4 PTP processing occurs. If none of these values are found, PTP frame decoding is passed to the IPJump field above. This allows flexibility in the hardware to skip past the protocol chains that are specific to customer networks including DSA-Tag, IEEE802.1Q tag, Provider tag, and so on.

Table 327: PTP Port Config Register 3
Device 0x1F, Register 0xA802

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	ARRTSMODE	R/W	0x0	0x0	Arrival Time Stamp Mode. This field is used to configure the Arrival Time Stamp mode as follows: 0x00: Arrival Time Stamp frame modification is disabled. Device functions the same manner as in PTP Gen 2.x – assuming the TCAM is disabled on the port. 0x01 to 0x0F: Reserved for future use. 0x10: Overwrite the PTPArrTime associated with enabled PTP Event frames into the frame into the four Reserved bytes in the PTP Common Header. 0x11 to 0xFF: Reserved for future use. **NOTE:** All frames will be processed using the above settings unless the frame can be hardware accelerated via setting the HWAccel bit below to a one. Changing this register's value can only occur when a port is in the Disabled Port State (Port offset 0x04). This register must be zero if ExtHWAccel (below) is set to a one. **NOTE:** Setting this register to a non-zero value adds a 8 byte FIFO to the receive path. **NOTE:** All frame's previous FCS needs to be checked for errors and if an error was detected, the frame's new FCS needs to be bit wise inverted in the last byte such that no bad frame should be made good when the new FCS is computed. **NOTE:** The TCAM will ‘see' the modified frame, both its contents and it increased size. **NOTE:** An undersized frame must not be modified in its size. **NOTE:** It is best if the MIB counters count the bytes on the ‘wire' prior to any frame size increase, but if this is not possible it is OK to count the bytes of the modified frame size.
7	FILTERACT	R/W	0x0	0x0	Filter LED Activity. 0 = LED Activity is activated for all frames. 1 = LED Activity is not activated for most IEEE 802.1 frames. This bit can filter all or most of the 802.1 Protocol frames from the Port's Activity LEDs. When this bit is set to a one, all 802.1 protocol frames (those with a DA = 01:80:C2:00:00:0x) will be potentially filtered from the port's Activity LED as determined by the ArrLEDCtrl and DepLEDCtrl registers (PTP Port offset 0x03). When this bit is cleared to a zero, only the 802.1 gPTP protocol frames will be potentially filtered from the port's Activity LED. **NOTE:** This bit affects the port's LEDs only. The frames themselves are not filtered inside the switch because of this bit.

Table 327: PTP Port Config Register 3 (Continued)
Device 0x1F, Register 0xA802

Bits	Field	Mode	HW Rst	SW Rst	Description
6	HWACCEL	R/W	0x0	0x0	Port PTP Hardware Acceleration enable. 0 = No or only Ingress PTP hardware acceleration 1 = Ingress and Egress PTP hardware acceleration is enabled. Setting this bit to a one enables PTP hardware acceleration on this port (this bit can be set to a one prior to a Time Arrays being configured or after they are configured). PTP hardware acceleration will automatically occur in the selected PTPMode (PTP Global offset 0x07) for the enabled PTP Domains once a Time Array (PTP Global offsets 0x12 to 0x1D) is configured and enabled. Even then PTP hardware acceleration will only occur for the Transport Specs enabled on this port (PTP Port offset 0x00). In this mode, any frame that cannot be hardware accelerated will be processed using the settings defined by ArrTSMode above (a type of fallback mode).Clearing this bit to a zero causes all frames to be processed using the settings defined by ArrTSMode above. Do not set this bit to a one if ExtHWAccel (below) is set to a one. **NOTE:** PTP Hardware Acceleration requires that the Time Stamping Clock Period (TAI offset 0x01) be 8000 picoseconds (8 ns) or 4000 picoseconds (4 ns) +/- 100 PPM. If the PTP_EXTCLK (external clock) is used (TAI offset 0x08), it must also be within this range before enabling PTP Hardware Acceleration. Changing this register's value can only occur when a port is in the Disabled Port State (Port offset 0x04). Setting this register to a one inserts an 8-byte FIFO to the receive path and a 12- or 46-byte FIFO to the transmit paths (assuming Full Check below is cleared to zero, else a 46-byte FIFO is inserted).
5	KEEPSA	R/W	0x0	0x0	Keep Frame's SA. 0 = Place Port’s SA into modified egressing PTP frames. 1 = Keep the frame’s SA even for modified egressing PTP frames. Typically, when the Data portion of a frame (the part of the frame between the EtherType and the CRC) is modified the address of the modifying entity is placed into the Source Address (SA) field of egressing frames. This is the result for modified PTP frames when this bit is cleared to 0. When this bit is set to 1, the SA portion of PTP frames is not modified.
4:2	Reserved	R/W	0x0	0x0	
1	PTPDEPINTEN	R/W	0x0	0x0	Precise Time Protocol Port Departure Interrupt enable. 0 = Disable PTP Departure capture interrupts. 1 = Enable PTP Departure capture interrupts. This field enables the per-port interrupt for outgoing PTP frame from this port. When this bit is set to a one, and this port's PTPDepTimeValid bit (PTP Port offset 0x10) is set to a one a PTP interrupt for this port will be indicted in PTP Global offset 0x08. **NOTE:** Hardware logic only time stamps the PTP frames when configured to do so by MsgTypeEn field (see PTP Global offset 0x00).

Table 327: PTP Port Config Register 3 (Continued)
Device 0x1F, Register 0xA802

Bits	Field	Mode	HW Rst	SW Rst	Description
0	PTPARRINTEN	R/W	0x0	0x0	Precise Time Protocol Port Arrival Interrupt enable. 0 = Disable PTP Arrival capture interrupts. 1 = Enable PTP Arrival capture interrupts. This field enabled the per-port interrupt for incoming PTP frames from this port. When this bit is set to a one, and this port's PTPArr0TimeValid bit (PTP Port offset 0x08) or its PTPArr1TimeValid bit (PTP Port offset 0x0C) is set to a one a PTP interrupt for this port will be indicted in PTP Global offset 0x08. **NOTE:** Hardware logic only time stamps the PTP frames when configured to do so by MsgTypeEn field (see PTP Global offset 0x00).

Table 328: PTP Port Config Register 4
Device 0x1F, Register 0xA803

Bits	Field	Mode	HW Rst	SW Rst	Description
15:8	ARRLEDCTRL	R/W	0x0	0x0	LED control for packets entering the device. When 0x0, if a received frame is classified as a PTP frame or an 802.1 protocol frame, the LED does not blink. But it blinks for every non-PTP or non-802.1 protocol frame. When 0x1, the LED blinks for every received frame classified as a PTP frame or an 802.1 protocol frame. It also blinks for every non-PTP frame or non-802.1 protocol frame. When 0xn, the LED blinks once for every n received frames classified as PTP or 802.1 protocol. It also blinks for every non-PTP frame or non-802.1 protocol frame. **NOTE:** This tracks all received PTP frames (even though the PTP core time stamps only the PTP event messages) and not just PTP frames that need time stamping or it tracks all received 802.1 protocol frames (any frame with a DA = 01:80:C2:00:00:0x). The FilterAct bit in PTP Port offset 0x02 controls which frames are tracked. This register affects the port's Activity LED only. It does not change how the frames progress through the switch.

Table 328: PTP Port Config Register 4 (Continued)
Device 0x1F, Register 0xA803

Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	DEPLEDCTRL	R/W	0x0	0x0	LED control for packets departing the device. When 0x0, if a transmitting frame is classified as a PTP frame or an 802.1 protocol frame, the LED does not blink. But it blinks for every non-PTP frame or non-802.1 protocol. When 0x1, the LED blinks for every transmitting frame classified as a PTP frame or an 802.1 protocol frame. It also blinks for every non-PTP frame or non-802.1 protocol frame. When 0xn, the LED blinks once for every n transmitting frames classified as PTP or 802.1 protocol. It also blinks for every non-PTP frame or non-802.1 protocol frame. **NOTE:** This tracks all transmitting PTP frames (even though the PTP core time stamps only the PTP event messages) and not just PTP frames that need time stamping or it tracks all transmitted 802.1 protocol frames (any frame with a DA = 01:80:C2:00:00:0x). The FilterAct bit in PTP Port offset 0x02 controls which frames are tracked. This register affects the port's Activity LED only. It does not change how the frames progress through the switch.

Table 329: PTP Port Config Register 5
Device 0x1F, Register 0xA807

Bits	Field	Mode	HW Rst	SW Rst	Description
15	UPDATE	R/W	0x0	0x0	Update Data. When this bit is set to a one, the data written to bits 7:0 will be loaded into the PTP Port Config register referenced by the Pointer bits below. After the write has occurred, this bit self clears to zero.
14:8	POINTER	R/W	0x0	0x0	Pointer to the desired octet of PTP Port Config. These bits select one of the possible PTP Port Config registers for both read and write operations. A write operation occurs if the Update bit is a one (the registers can be written to by writing this register in a single operation). Otherwise a read of the current Pointer occurs and the data found there is placed in the Data bits below (the desired register can be read by first writing to this register, with Update = 0, and then reading this register). The Pointer bits are used to access the Index registers as follows: 0x00: PTP Port Control Register 0x01 to 0x5F: Reserved for future use 0x60 to 0x67: IEEE 1588 Ingress Action Vectors 0x68 to 0x6F: IEEE 1588 Egress Action Vectors 0x70 to 0x77: IEEE 802.1AS Ingress Action Vectors 0x78 to 0x7F: IEEE 802.1AS Egress Action Vectors
7:0	DATA	R/W	0x0	0x0	Octet Data of the PTP Port Config register referenced by the Pointer bits above.

Table 330: PTP Port Status Register 22
Device 0x1F, Register 0xA808

Bits	Field	Mode	HW Rst	SW Rst	Description
2:1	PTPARR0INTSTATUS	R/W	0x0	0x0	Precise Time Protocol Arrival Time 0 Interrupt Status. This register indicates the timestamp status when the PTPArr0TimeValid bit below gets set for a given port when an incoming PTP frame is time stamped in PTPArr0Time counter as long as that frame was not hardware accelerated (see HWAccel in PTP Port offset 0x02). When PreemptionTimestamp bit is set to 1, this bit will be read as preemption PTP frame's timestamp status. 0x0 = Normal for example, none of the error conditions stated below are valid for this packet. 0x1 = If the PTPArr0Time counter with its associated valid and SequenceID got overwritten as there were more than one PTP frame that needed to use arrival0 counters arrived into the switch through this port before CPU cleared the corresponding valid and counter bits for the previous PTP frame(s). 0x2 = If the incoming frame could not be time stamped in hardware because the DisTSOverwrite was set to a 0x1 and PTPArr0TimeValid was 0x1 when this PTPFrame was processed in hardware logic. This can occur when there is more than one PTP frame that requires time stamping into arrival 0 counters arrives into the switch core before CPU clears the valid bits for the previous frame. 0x3 = Reserved **NOTE:** If the PTP frame gets discarded inside the switch for policy, CRC, queue congestion or any other reasons then one of the PTP arrival discard counters get updated (PTPNonTSArrDisCtr or PTPTSArrDisCtr). See the discard counter descriptions (PTP Port offset 0x15) for further details.

Table 330: PTP Port Status Register 22 (Continued)
Device 0x1F, Register 0xA808

Bits	Field	Mode	HW Rst	SW Rst	Description
0	PTPARR0TIMEVALID	R/W	0x0	0x0	Precise Time Protocol Arrival 0 Time Valid. When the PTPArr0Time value is updated by hardware (which it will not do as long as the frame is hardware accelerated – see HWAccel in PTP Port offset 0x02), this bit is set to a 0x1 validating the time counter. If PreemptionTimestamp bit is set to 0, this register being 1 validates Express PTP frame's arrival 0 timestamp. If PreemptionTimestamp bit is set to 1, this register being 1 validates Preemption PTP frame's arrival 0 timestamp. 0x0: PTPArr0Time is not valid. 0x1: PTPArr0Time is valid and PTPArr0IntStatus represents the status information for the PTPArr0Time counter. **NOTE:** This is set by hardware for the frames which are assured to reach the CPU. For frames with CRC error, and so on, this bit will not be set but either PTPNonTSArrCtr or PTPTSArrCtr is updated. **NOTE:** This valid bit must be cleared by software after reading the value and hardware does not provide any auto-clearing mechanisms. This is because hardware has no method to figure out if software has completed reading all the relevant registers for a particular Time counter before clearing the valid bit. **NOTE:** When this bit is set to a one, it will generate a PTP Interrupt for this port (PTPInt – PTP Global offset 0x08) if this port's PTPArrIntEn bit is set to a one (PTP Port offset 0x02).

Table 331: PTP Port Status Register 23
Device 0x1F, Register 0xA809

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PTPARR0TIME_15_0	R/W	0x0	0x0	Precise Time Protocol Arrival 0 Time counter bits 15 to 0 of a 32-bit register. This register indicates the PTP Arrival 0 time stamp value that is captured by the PTP logic for a PTP frame that must be time stamped. The captured time stamp value is from a Global Timer counter running off of a switch internal clock. When the PreemptionTimestamp bit is set to 1, this register is timestamped for preemption PTP frame. The value in this counter is validated by PTPArr0TimeValid bit and PTPArr0IntStatus indicates the status of the PTP frame through the device as described above. **NOTE:** Maximum jitter associated with time stamping within the hardware is one Time Stamping Clock period. The upper 16-bits of this register are contained in the register below.

Table 332: PTP Port Status Register 24
Device 0x1F, Register 0xA80A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PTPARR0TIME_31_16	R/W	0x0	0x0	Precise Time Protocol Arrival 0 Time counter bits 31 to 16 of a 32-bit register. This register indicates the PTP Arrival 0 time stamp value that is captured by the PTP logic for a PTP frame that must be time stamped. The captured time stamp value is from a Global Timer counter running off of a switch internal clock. When PreemptionTimestamp bit is set to 1, this register is timestamped for preemption PTP frame. The value in this counter is validated by PTPArr0TimeValid bit and PTPArr0IntStatus indicates the status of the PTP frame through the device as described above. **NOTE:** Maximum jitter associated with time stamping within the hardware is one Time Stamping Clock period.The lower 16-bits of this register are contained in the register above.

Table 333: PTP Port Status Register 25
Device 0x1F, Register 0xA80B

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PTPARR0SEQID	R/W	0x0	0x0	Precise Time Protocol Arrival 0 Sequence Identifier. This register indicates the sequence identifier (extracted in hardware from incoming frames PTPCommonHeader) for the frame whose time stamp information has been captured by hardware logic in PTPArr0Time register. When PreemptionTImestamp bit is set to 1, this register indicates sequence identifier for preemption PTP frames.

Table 334: PTP Port Status Register 26
Device 0x1F, Register 0xA80C

Bits	Field	Mode	HW Rst	SW Rst	Description
2:1	PTPARR1INTSTATUS	R/W	0x0	0x0	Precise Time Protocol Arrival Time 1 Interrupt Status. This register indicates the timestamp status when the PTPArr1TimeValid bit below gets set for a given port when an incoming PTP frame is time stamped in PTPArr1Time counter as long as that frame was not hardware accelerated (see HWAccel in PTP Port offset 0x02). When the PreemptionTimestamp bit is set to 1, this bit will be read as preemption PTP frame's timestamp status. 0x0 = Normal for example, none of the error conditions stated below are valid for this packet. 0x1 = If the PTPArr1Time counter with its associated valid and SequenceID got overwritten as there were more than one PTP frame that needed to use arrival1 counters arrived into the switch through this port before CPU cleared the corresponding valid and counter bits for the previous PTP frame(s). 0x2 = If the incoming frame could not be time stamped in hardware because the DisTSOverwrite was set to a 0x1 and PTPArr1TimeValid was 0x1 when this PTPFrame was processed in hardware logic, then this can occur when there is more than one PTP frame that requires time stamping into arrival 1 counters arrives into the switch core before CPU clears the valid bits for the previous frame. 0x3 = Reserved **NOTE:** If the PTP frame gets discarded inside the switch for policy, CRC, queue congestion or any other reasons then one of the PTP arrival discard counters get updated (PTPNonTSArrDisCtr or PTPTSArrDisCtr). See the discard counter description (PTP Port offset 0x15) for details.

Table 334: PTP Port Status Register 26 (Continued)
Device 0x1F, Register 0xA80C

Bits	Field	Mode	HW Rst	SW Rst	Description
0	PTPARR1TIMEVALID	R/W	0x0	0x0	Precise Time Protocol Arrival 1 Time Valid. When the PTPArr1Time value is updated by hardware (which it will not do as long as the frame is hardware accelerated – see HWAccel in PTP Port offset 0x02), this bit is set to a 0x1 validating the time counter. If the PreemptionTimestamp bit is set to 0, then this register being 1 validates Express PTP frame's arrival 1 timestamp. If the PreemptionTimestamp bit is set to 1, then this register being 1 validates Preemption PTP frame's arrival 1 timestamp. 0x0: PTPArr1Time is not valid. 0x1: PTPArr1Time is valid and PTPArr1IntStatus represents the status information for the PTPArr1Time counter. **NOTE:** This is set by hardware for the frames which are assured to reach the CPU. For frames with CRC error, and so on, this bit will not be set but either PTPNonTSArrCtr or PTPTSArrCtr is updated. **NOTE:** This valid bit must be cleared by software after reading the value and hardware does not provide any auto-clearing mechanisms. This is because hardware has no method to figure out if software has completed reading all the relevant registers for a particular Time counter before clearing the valid bit. **NOTE:** When this bit is set to a one, it will generate a PTP Interrupt for this port (PTPInt – PTP Global offset 0x08) if this port's PTPArrIntEn bit is set to a one (PTP Port offset 0x02).

Table 335: PTP Port Status Register 27
Device 0x1F, Register 0xA80D

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PTPARR1TIME_15_0	R/W	0x0	0x0	Precise Time Protocol Arrival 1 Time counter bits 15 to 0 of a 32-bit register. This register indicates the PTP Arrival 1 time stamp value that is captured by the PTP logic for a PTP frame that must be time stamped. The captured time stamp value is from a Global Timer counter running off of a switch internal clock. When the PreemptionTimestamp bit is set to 1, this register is timestamped for preemption PTP frame. The value in this counter is validated by PTPArr1TimeValid bit and PTPArr1IntStatus indicates the status of the PTP frame through the device as described above. **NOTE:** Maximum jitter associated with time stamping within the hardware is one Time Stamping Clock period. The upper 16 bits of this register are contained in the register below.

Table 336: PTP Port Status Register 28
Device 0x1F, Register 0xA80E

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PTPARR1TIME_31_16	R/W	0x0	0x0	Precise Time Protocol Arrival 1 Time counter bits 31 to 16 of a 32-bit register. This register indicates the PTP Arrival 1 time stamp value that is captured by the PTP logic for a PTP frame that must be time stamped. The captured time stamp value is from a Global Timer counter running off of a switch internal clock. When the PreemptionTimestamp bit is set to 1, this register is timestamped for preemption PTP frame. The value in this counter is validated by PTPArr1TimeValid bit and PTPArr1IntStatus indicates the status of the PTP frame through the device as described above. **NOTE:** Maximum jitter associated with time stamping within the hardware is one Time Stamping Clock period. The lower 16 bits of this register are contained in the register above.

Table 337: PTP Port Status Register 29
Device 0x1F, Register 0xA80F

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PTPARR1SEQID	R/W	0x0	0x0	Precise Time Protocol Arrival 1 Sequence Identifier. This register indicates the sequence identifier (extracted in hardware from incoming frames PTPCommonHeader) for the frame whose time stamp information has been captured by hardware logic in PTPArr1Time register. When the PreemptionTImestamp bit is set to 1, this register indicates sequence identifier for preemption PTP frames.

Table 338: PTP Port Status Register 30
Device 0x1F, Register 0xA810

Bits	Field	Mode	HW Rst	SW Rst	Description
2:1	PTPDEPINTSTATUS	R/W	0x0	0x0	Precise Time Protocol Departure Time Interrupt Status. This register indicates the timestamp status when the PTP Departure Time Valid bit below gets set for a given port when an incoming PTP frame is time stamped in PTPDepTime counter as long as that frame was not hardware accelerated (see HWAccel in PTP Port offset 0x02). When PreemptionTimestamp bit is set to 1, this bit will be read as preemption PTP frame's timestamp status. 0x0 = Normal, for example, none of the error conditions stated below are valid for this packet. 0x1 = If the PTPDepTime counter with its associated valid and SequenceID got overwritten as there were more than one PTP frame that are required to use departure counter departed out of the switch through this port before CPU cleared the corresponding valid and counter bits for the previous PTP frame(s). 0x2 = If the outgoing frame could not be time stamped in hardware because the DisTSOverwrite was set to a 0x1 and PTPDepTimeValid was 0x1 when this PTPFrame was processed in hardware logic, then this can occur when there is more than one PTP frame that requires time stamping into departure counter leaves the switch core before CPU clears the valid bits for the previous frame. 0x3 = Reserved **NOTE:** If the PTP frame gets discarded inside the switch for CRC reasons then the PTP departure discard counter gets updated (PTPNonTSDepDisCtr or PTPTSDepDisCtr). See the discard counter description (PTP Port offset 0x15) for further details.

Table 338: PTP Port Status Register 30 (Continued)
Device 0x1F, Register 0xA810

Bits	Field	Mode	HW Rst	SW Rst	Description
0	PTPDEPTIMEVALID	R/W	0x0	0x0	Precise Time Protocol Departure Time Valid. When the PTPDepTime value is updated by hardware (which it will not do as long as the frame is hardware accelerated – see HWAccel in PTP Port offset 0x02), this bit is set to a 0x1 validating the time counter. If the PreemptionTimestamp bit is set to 0, then this register being 1 validates Express PTP frame's departure timestamp. If the PreemptionTimestamp bit is set to 1, then this register being 1 validates Preemption PTP frame's departure timestamp. 0x0: PTPDepTime is not valid. 0x1: PTPDepTime is valid and PTPDepIntStatus represents the status information for the PTPDepTime counter. **NOTE:** This is set by hardware for the PTP event frames (those defined in MsgTypeEn – PTP Global offset 0x01) which depart the port. For frames with CRC error, and so on, this bit will not be set but either PTPNonTSDepCtr or PTPTSDepCtr is updated. **NOTE:** This valid bit must be cleared by software after reading the value and hardware does not provide any auto-clearing mechanisms. This is because hardware does not have the means to determine if software has completed reading all the relevant registers for a particular Time counter before clearing the valid bit. **NOTE:** When this bit is set to a one, it will generate a PTP Interrupt for this port (PTPInt – PTP Global offset 0x08) if this port's PTPDepIntEn bit is set to a one (PTP Port offset 0x02).

Table 339: PTP Port Status Register 31
Device 0x1F, Register 0xA811

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PTPDEPTIME_15_0	R/W	0x0	0x0	Precise Time Protocol Departure Time counter bits 15 to 0 of a 32-bit register. This register indicates the PTP Departure time stamp value that is captured by the PTP logic for a PTP frame that needs to be time stamped. The captured time stamp value is from a Global Timer counter running off of a switch internal clock. When the PreemptionTimestamp bit is set to 1, this register is timestamped for preemption PTP frame. The value in this counter is validated by PTPDepTimeValid bit and PTPDepIntStatus indicates the status of the PTP frame through the device described above. **NOTE:** Maximum jitter associated with time stamping within the hardware is one Time Stamping Clock period. The upper 16 bits of this register are contained in the register below.

Table 340: PTP Port Status Register 32
Device 0x1F, Register 0xA812

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PTPDEPTIME_31_16	R/W	0x0	0x0	Precise Time Protocol Departure Time counter bits 31 to 16 of a 32-bit register. This register indicates the PTP Departure time stamp value that is captured by the PTP logic for a PTP frame that must be time stamped. The captured time stamp value is from a Global Timer counter running off of a switch internal clock. When the PreemptionTimestamp bit is set to 1, this register is timestamped for preemption PTP frame. The value in this counter is validated by PTPDepTimeValid bit and PTPDepIntStatus indicates the status the PTP frame through the device described above. **NOTE:** Maximum jitter associated with time stamping within the hardware is one Time Stamping Clock period. The lower 16 bits of this register are contained in the register above.

Table 341: PTP Port Status Register 33
Device 0x1F, Register 0xA813

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PTPDEPSEQID	R/W	0x0	0x0	Precise Time Protocol Departure Sequence Identifier. This register indicates the sequence identifier (extracted in hardware from incoming frames PTPCommonHeader) for the frame whose time stamp information has been captured by hardware logic in PTPDepTime register. When the PreemptionTImestamp bit is set to 1, this register indicates sequence identifier for preemption PTP frames.

Table 342: PTP Port Status Register 34
Device 0x1F, Register 0xA814

Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	PTPOUTFCSERR	R/W	0x0	0x0	Precise Time Protocol Output FCS (CRC) Error counter. This counter is incremented whenever PTP egress forces a bad CRC on a hardware accelerated frame (HWAccel is set to a one in PTP Port offset 0x02 & DoNotCorrupt is cleared to a zero – PTP Port offset 0x02). See the description of what frames could get a bad CRC in the DoNotCorrupt register (PTP Port offset 0x02). This counter wraps around in hardware.

Table 343: PTP Port Status Register 35
Device 0x1F, Register 0xA815

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	PTPTSDEPDISCTR	R/W	0x0	0x0	Precise Time Protocol Departure frame discard counter for PTP frames that requires hardware time stamping. This counter is incremented whenever it discards a PTP frame that requires hardware time stamping (for example, PTPEtype is a match and MsgTypeEn bit for the corresponding MsgId field in the PTP frame is set). The PTP frame could be discarded because of CRC reasons in egress pipe. This counter wraps around in hardware.
11:8	PTPNONTSDEPDISCTR	R/W	0x0	0x0	Precise Time Protocol Departure frame discard counter for PTP frames that do not require hardware time stamping. This counter is incremented whenever it discards a PTP frame that does not require time stamping (for example, PTPEtype is a match, but MsgTypeEn bit for the corresponding MsgId field in the PTP frame is not set). The PTP frame could be discarded because of CRC reasons in egress pipe. This counter wraps around in hardware.
7:4	PTPTSARRDISCTR	R/W	0x0	0x0	Precise Time Protocol arrival frame discard counter for PTP frames that requires hardware time stamping. **NOTE:** This counter is incremented whenever it discards a PTP frame that requires hardware time stamping (for example, PTPEtype is a match and MsgTypeEn bit for the corresponding MsgId field in the PTP frame is set). The PTP frame could be discarded because of CRC, Policy or Queue congestion (Policy and Queue congestion discards are detected only if the port is not using the TCAM, for example, the Port's TCAM Mode = 0x0 in Port offset 0x0D). As an IP PTP block, there is no TCAM, Policy and/or Queue congestion signal so the only way this counter get incremented is by CRC errors. This counter wraps around in hardware.
3:0	PTPNONTSARRDISCTR	R/W	0x0	0x0	Precise Time Protocol Non time stamp Arrival frame discard counter. **NOTE:** This counter is incremented whenever it discards a PTP frame that does not require hardware time stamping (for example, PTPEtype is a match but MsgTypeEn bit for the corresponding MsgId field in the PTP frame is not set). The PTP frame could be discarded because of CRC, Policy or Queue congestion (Policy and Queue congestion discards are detected only if the port is not using the TCAM, for example, the Port's TCAM Mode = 0x0 in Port offset 0x0D). As an IP PTP block, there is no TCAM, Policy and/or Queue congestion signal so the only way this counter get incremented is by CRC errors. This counter wraps around in hardware.

Table 344: ReadPlus Command Register – PTP Global
Device 0x1F, Register 0xA86E

Bits	Field	Mode	Description
15	Read Plus Enable	R/W	Read Plus Enable 1 = Enable 0 = Disable
14:12	Reserved	Res	Reserved
11:8	PTPReg	R/W	PTP Registers 0x0 for 4.88xx – 4.89xx 0xE for 4.8Cxx – 4.8Dxx 0xF for 4.8Exx – 4.8Fxx **NOTE:** These registers must use ReadPlus command otherwise readback value is not correct Register 4.8F00 to 4.8F1F, PTP Global Time Array Registers Registers 4.8C1E and 4.8C0F, PTP Global Time[31:0] Registers 4.8D01 and 4.8D02, Event Capture Time[31:0] Registers 4.8808 to 4.880B, PTP Arrival 0 Registers 4.880C, 4.881D, 4.881E and 4.880F, PTP Arrival 1 Registers 4.8900 to 4.8903, PTP Departure
7:5	Reserved	RES	
4:0	PTPAddr	R/W	PTP Address PTPAddr[3:0] = Lower four bits of the address of the PTP registers to be read. For 4.88xx, PTPAddr[4] = ‘0’ For 4.89xx, PTPAddr[4] = ‘1’ For 4.8Cxx, PTPAddr[4] = ‘0’ For 4.8Dxx, PTPAddr[4] = ‘1’ For 4.8Exx, PTPAddr[4] = ‘0’ For 4.8Fxx, PTPAddr[4] = ‘1’

Table 345: ReadPlus Data Register – PTP Global
Device 0x1F, Register 0xA86F

Bits	Field	Mode	Description
15:0	Read Plus Data	R/W	Read Plus Data This register is used to read out the ReadPlus Data. To read 32-bit wide PTP registers, read from this register back-to-back.

Table 346: Ingress Mean Path Delay 36
Device 0x1F, Register 0xA81C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	MEANPATHDELAY	R/W	0x0	0x0	Ingress Mean Path Delay register. This indicates the cable delay between this port and its link partner in unsigned nanoseconds. This is used in HWAccel PTP mode (PTP Port offset 0x02).

Table 347: Ingress Path Delay Asymmetry 37
Device 0x1F, Register 0xA81D

Bits	Field	Mode	HW Rst	SW Rst	Description
15	IPDASIGN	R/W	0x0	0x0	Ingress Path Delay Asymmetry Sign. 0 = The Ingress Path Delay Asymmetry number is added. 1 = The Ingress Path Delay Asymmetry number is subtracted. This indicates the sign of the asymmetry value (below) beyond the Mean Path Delay (PTP Port offset 0x1C) that must be adjusted for more accurate cable measurements.
14:0	INGRESSPATHDELAYASYMMETRY	R/W	0x0	0x0	Ingress Path Delay Asymmetry register. This indicates the asymmetry value beyond the Mean Path Delay (PTP Port offset 0x1C) that must be added for more accurate cable measurements. This register is in unsigned nanoseconds.

Table 348: Egress Path Delay Asymmetry 38
Device 0x1F, Register 0xA81E

Bits	Field	Mode	HW Rst	SW Rst	Description
15	EPDASIGN	R/W	0x0	0x0	Egress Path Delay Asymmetry Sign. 0 = The Egress Path Delay Asymmetry number is added. 1 = The Egress Path Delay Asymmetry number is subtracted. This indicates the sign of the asymmetry value (below) beyond the Mean Path Delay (PTP Port offset 0x1C) that must be adjusted for more accurate cable measurements.
14:0	EGRESSPATHDELAYASYMMETRY	R/W	0x0	0x0	Egress Path Delay Asymmetry register. This indicates the asymmetry value beyond the Mean Path Delay (PTP Port offset 0x1C) that must be subtracted for more accurate cable measurements. This register is in unsigned nanoseconds.

Table 349: TAI Global Config 22
Device 0x1F, Register 0xA840

Bits	Field	Mode	HW Rst	SW Rst	Description
15	EVENTCAPOV	R/W	0x0	0x0	Event Capture Overwrite. 0 = Capture & Hold first PTP Event. 1 = Capture all PTP Events & Retain the last PTP Event. When this bit is cleared to a zero, it configures the hardware to capture a single event, for example, take a snapshot of PTP Global Timer value at the first EventReq (see EventPhase below) and wait for software to read the EventCapRegister before capturing another event. This mode returns the data from the first EventReq. When this bit is set to a one, it enables overwriting the EventCap registers (TAI offsets 0x09 to 0x0B) whenever an EventReq occurs (see EventPhase below). In this mode, the hardware will overwrite the EventCapRegister even if the previously captured event register data has not been read by the software. This mode returns the data from the last EventReq.
14	EVENTCTRSTART	R/W	0x0	0x0	Event Counter Start. 0 = Do not increment the Event Capture Counter. 1 = Increment the Event Capture Counter on EventReqs. When this bit is cleared to zero, the EventCapCtr is not modified even when EventReq occurs (see EventPhase below). When this bit is set to a one, it enables incrementing the EventCapCtr register (TAI offset 0x09) whenever an EventReq occurs (see EventPhase below).
13	EVENTPHASE	R/W	0x0	0x0	Event Phase. 0 = Event Requests occur on the rising edge of the PTP_EVREQ GPIO pin 1 = Event Requests occur on the falling edge of the PTP_EVREQ GPIO pin. When this bit is cleared to a zero when an EventReq occurs on the rising edge of the PTP_EVREQ input or on the leading edge of PTP_TRIG when internally sampled (see the CaptureTrig bit in TAI Register 1F.A849). When this bit is set to a one when an EventReq occurs on the falling edge of the PTP_EVREQ input or on the trailing edge of PTP_TRIG when internally sampled. When PTP_TRIG is selected to be internally captured (instead of using the PTP_EVREQ GPIO pin – see Capture Trig in TAI Register 1F.A849), this Event Phase is used to invert the value of the normal internal PTP_TRIG that is captured. When Event Phase = 0, the leading edge (or normal rising edge) of the internal PTP_TRIG is captured. When Event Phase = 1, the trailing edge (or normal falling edge) of the internal PTP_TRIG is captured.

Table 349: TAI Global Config 22 (Continued)
Device 0x1F, Register 0xA840

Bits	Field	Mode	HW Rst	SW Rst	Description
12	TRIGPHASE	R/W	0x0	0x0	Trigger Phase. 0 = The PTP Trigger output is active high on the PTP_TRIG GPIO pin 1 = The PTP Trigger output is active low on the PTP_TRIG GPIO pin When this bit is cleared to a zero the active phase of the PTP_TRIG output to the GPIO is normal active high. For example, the pulse mode of PTP_TRIG will be normally low with a high pulse and the 50% duty cycle's leading edge is the rising edge. When this bit is set to a one the active phase of the PTP_TRIG output to the GPIO is inverted to be active low. For example, the pulse mode of PTP_TRIG will be normally high with a low pulse and the 50% duty cycle's leading edge is the falling edge. **NOTE:** This bit has no effect on the internal phase of PTP_TRIG or any other signal used in the internal blocks of the device.
11	Reserved	R/W	0x0	0x0	
10	IRLCLKGENREQ	R/W	0x0	0x0	Ingress Rate Limiter's Clock Generation Request/Enable. When this bit is set to a one, it enables a 50 duty cycle clock generation for the Ingress Rate Limiter's logic (IRL Clk) as configured by the IRLClkGenAmt, IRLClkComp (both ps & Sub ps) and IRLGenTime fields. On Reset, this IRL Clock defaults to a 3.125 µs rate. This rate can be changed at any time by updating the IRLClkGenAmt &/or IRLClkComp (ps & Sub ps) registers. If a particular phase of this of this clock is desired, then set the desired start edge time in IRLGenTime (TAI offsets 0x14 & 0x15) and toggle this bit to a zero and then to a one again. The hardware supports this, but it is hidden as the current IRL ITSM block uses a minimum of 20 IRL Clks to form a window. So setting this edge does not actually align it to anything until the IRL ITMS block gets updated later.
9	TRIGGENINTEN	R/W	0x0	0x0	Trigger Generator Interrupt Enable. 0 = Mask interrupts generated by the PTP Trigger logic 1 = Enable interrupts generated by the PTP Trigger logic When this bit is cleared to zero, no interrupts are generated by the TrigGen logic. When this bit is set to a one, the TAI block will generate an interrupt whenever a TrigGen pulse event has occurred. This interrupt will appear in the Trigger Mode Interrupt in PTP Global Register 1F.A868.
8	EVENTCAPINTEN	R/W	0x0	0x0	Event Capture Interrupt Enable. 0 = Mask interrupts generated by the PTP Event Capture logic 1 = Enable interrupts generated by the PTP Event Capture logic When this bit is cleared to zero, no interrupts are generated by the EventCap logic. When this bit is set to a one, the TAI block will generate an interrupt whenever an EventReq occurs. This interrupt will appear in the Event Capture Interrupt in PTP Global Register 1F.A868.

Table 349: TAI Global Config 22 (Continued)
Device 0x1F, Register 0xA840

Bits	Field	Mode	HW Rst	SW Rst	Description
7	TRIGLOCK	R/W	0x0	0x0	Trigger Lock. When this bit is set to a one, the leading edge of PTP_TRIG (see TrigPhase above) will be adjusted to the value contained in the TrigGenTime register (TAI offsets 0x10 & 0x11) if and only if the leading edge of PTP_TRIG occurs +/- the number of PTP Clocks as defined in the TrigLockRange register below and PTP_TRIG is enabled (TrigGenReq, below, is set to a one) and the TrigGenTime register is non-zero. A correction will also be made to the rising edge of IRL_Clk by setting it to the value contained in the IRLGenTime register (TAI offsets 0x14 & 0x15) if and only if the leading edge of IRL_Clk occurs +/- the number of PTP Clocks as defined in the TrigLockRange register below and IRL_Clk is enabled (IRLClkGenReq, above, is set to a one) and the IRLGenTime register is non-zero. **NOTE:** The TrigLockRange, the TrigGenTime and the IRLGenTime registers must be configured before this bit is set to a one. When the TrigGenTime and IRLGenTime are both past in time, this bit will self clear (for example, it will be active for only one possible correction per wrap around of the 32-bit Global Timer). This bit will clear if the Global time has passed even if a correction was not required or completed. When this bit clears, the Lock correction amount, if any, will be registered in the Lock Correction fields for PTP_TRIG and IRL_Clk (TAI offsets 0x12 & 0x16). The hardware monitors both TrigGen and IRL_Clk's times and if both are enabled, whichever is first is processed 1st and this bit will clear only after both times have past.
6:4	TRIGLOCKRANGE	R/W	0x0	0x0	Trigger Locking Range. These bits are used along with the previously described TrigLock bit. They determine the +/- error limit to adjust and re-center the leading edge of PTP_TRIG in PTP_CLK increments (8 ns if using the internal clock) or PTP_EXTCLK increments (if using an external PTP clock).

Table 349: TAI Global Config 22 (Continued)
Device 0x1F, Register 0xA840

Bits	Field	Mode	HW Rst	SW Rst	Description
3	BLOCKUPDATE	R/W	0x0	0x0	Block Update. 0 = Update the 50 duty cycle clock mode registers as written. 1 = Update the 50 duty cycle clock mode registers as a block. When the 50 duty cycle clock mode is enabled (see TrigMode below), the following registers are used to configure that mode: TrigGenAmt (TAI offsets 0x02 & 0x03), TrigClkComp (TAI offset 0x04) and TrigClkCompSubPs (TAI offset 0x05). To compensate for PPM drift between this node's crystal and the Grand Master's crystal, these registers may must be updated periodically. The same is true for the IRL clock which is configured using IRLClkGenAmt (TAI offset 0x06), IRLClkComp (TAI offset 0x07) and IRLClkCompSupPs (TAI offset 0x08). Setting this register bit to a one allows the updated values in these register groups (TAI offset 0x02 to 0x05 and TAI offset 0x06 to 0x08) to be presented to the hardware together at the same time and at a time when the hardware is not using these register values. This mode insures smooth, glitch free, updates when the contents of more than one register must change during an update. The contents of the TRIG registers (TAI offsets 0x02 to 0x05) are presented to the hardware as a block whenever the TrigClkCompSubPs register is written to (at TAI offset 0x05). The contents of the IRL_Clk registers (TAI offsets 0x06 to 0x08) are presented to the hardware as a block whenever the IRLClkCompSubPs register is written to (at TAI offset 0x08). This means that the software does not need to write all of these registers during an update. Only the registers that are changing need to be written to (it is assumed that the sub-picosecond register must be adjusted for each update, so writing to this register triggers the update).
2	MULTIPTPSYNC	R/W	0x0	0x0	Multiple PTP device sync mode. Used in systems where multiple PTP enabled devices must synchronize their PTP Global Time counters (TAI offsets 0x0E & 0x0F). 0 = Normal Event Request mode. 1 = Enable Multiple PTP device sync mode. When this bit is cleared to zero, the EventRequest interface operates normally (for example, an EventReq transfers the value of the PTP Global Time[31:0] register to the EventCapTime[31:0] register based on the setting of the EventCapOv register above). When this bit is set to a one, an EventReq (see EventPhase above) transfers the value in TrigGenAmt[31:0] (TAI offsets 0x02 & 0x03) into the PTP Global Time[31:0] register (TAI offsets 0x0E & 0x0F). The EventCapTime[31:0] (TAI offsets 0x0A & 0x0B) is also updated at the same time with the previous value that the PTP Global Time[31:0] register contained prior to be updated.

Table 349: TAI Global Config 22 (Continued)
Device 0x1F, Register 0xA840

Bits	Field	Mode	HW Rst	SW Rst	Description
1	TRIGMODE	R/W	0x0	0x0	Trigger Mode. 0 = 50 duty cycle clock mode 1 = Pulse (one-shot) mode When this bit is cleared to zero, the 50 duty cycle clock mode is enabled. In this mode the value specified in the TrigGenAmt is used as the period for generating a 50 duty cycle clock on the PTP_TRIG signal. **NOTE:** The minimum clock period that can be generated on the PTP_TRIG signal is four 4 times the TSClkPer amount. When register TrigGenTimerSel below is set to 0x0, the frequency of this clock can be adjusted in ps increments (see TrigClkComp, TAI offset 0x04) and it can be realigned to a specific time (see TrigLock bit above). The first leading edge of the 50 duty cycle clock will occur the first time the PTP Global Time (PTP TAI offsets 0x0E & 0x0F) equals the value in the non-zero TrigGenTime register (PTP TAI offsets 0x10 and 0x11) after TrigGenReq, below, is set to a one. This leading edge control occurs as long as the TrigGenTime register is non-zero. If it is zero, then the leading edge will occur when the TrigGenReq bit below is set to a one without regard to the PTP Global Time. The phase of the leading edge is controlled by the TrigPhase bit above. When register TrigGenTimerSel below is set to 0x1 or 0x2, the generated clock is locked to the selected Time Array's (See TrigGenDomain below) compensated ToD or 1722 Timer. The first leading edge of the 50 duty cycle clock will occur the first time the PTP ToD/1722 Time (PTP Global offsets 0x13, 0x14, 0x15, 0x18, 0x19 & 0x1A) is larger than or equal to the value in the non-zero TrigGenTime register (PTP TAI offsets 0x10 & 0x11) after TrigGenReq, below, is set to a one. This leading edge control occurs as long as the TrigGenTime register is non-zero. If it is zero, then the leading edge will occur when the TrigGenReq bit below is set to a one without regard to the PTP ToD/1722 Time. The phase of the leading edge is controlled by the TrigPhase bit above. When this bit is set to a one, Pulse mode is enabled. This mode matches the PTP Global Timer (TAI offsets 0x0E and 0x0F) and the TrigGenAmt register (TAI offsets 0x02 and 0x03) to generate a pulse at that time on the PTP_TRIG signal. The width of the pulse is specified by PulseWidth & PulseWitdhRange (TAI offset 0x05). **NOTE:** The minimum pulse width that can be generated is one TSClkPer amount (TAI offset 0x01) and the maximum pulse width is more than 30 million times the TSClkPer. The phase of the pulse is controlled by TrigPhase bit above.

Table 349: TAI Global Config 22 (Continued)
Device 0x1F, Register 0xA840

Bits	Field	Mode	HW Rst	SW Rst	Description
0	TRIGGENREQ	R/W	0x0	0x0	Trigger Generation Request/Enable. When this bit is set to a one, it enables a one-shot pulse or the 50 duty cycle clock generation on PTP_TRIG as previously configured by the TrigGenAmt, TrigMode, TrigClkComp (ps & Sub ps), PulseWidth, and TrigGenTime and TrigGenDelay fields. If TrigMode (above) is set to a one (pulse mode), then this bit will self clear after the pulse occurs (for example, the trailing edge of the pulse as defined by the Pulse Width and Pulse Width Range registers – TAI offset 0x05). If TrigMode is cleared to a zero, then the 50 duty cycle clock will continue running as long as this bit is set to a one. **NOTE:** The Self Clearing of this bit when in pulse mode has been changed. This is to prevent a problem with re-triggering when the pulse is still active (which could easily be a problem with the new Pulse Width Range select registers).

Table 350: TAI Global Config 23
Device 0x1F, Register 0xA841

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	TSCLKPER	RO	0x0	0x0	Time Stamping Clock Period in picoseconds. This field specifies the clock period for the time stamping clock supplied to the PTP hardware. When this device is using the 250 MHz internally generated clock for the PTP hardware, the value of this register must be 0x0FA0, or 4000 decimal which indicates a clock period of 4000 ps or 4 ns (or 250 MHz). When this device's PTP hardware is clocked by an external clock (using PTP_EXTCLK – see PtpExtClk in TAI offset 0x1E), this register must be set to the number of ps in that clock's period. If hardware accelerated PTP is being used (HWAccel or ExtHWAccel, both in PTP Port offset 0x02), then the external PTP clock input to the PTP hardware must be 125 MHz, so the value of this register must be 0x1F40 or 8000 decimal which indicates a clock period of 8000 ps or 8 ns (or 125 MHz). This register is used to know when the accumulated TrigClkComp values have exceeded a full clock period so that an extra clock can be added or subtracted during the next PTP_TRIG clock cycle (when PTP_TRIG is in 50% duty cycle clock mode – TrigMode in TAI offset 0x00). This supports adjusting the PTP_TRIG in very small ppm amounts in both the positive and negative directions. This register is also used in the Time of Day/1722 Time Arrays to know if the PTP clock cycle is 8 ns or 4 ns – which are the only sampling clock rates supported by the Time of Day/1722 Time Arrays. This register is also used in the Time of Day/1722 Time Arrays to know if the PTP clock cycle is 8 ns or 4 ns. It configures to a 4 ns PTP clock cycle time if bits 15:12 of this register = 0x0, else is configures to an 8 ns PTP clock cycle. Bits 11:0 of this register are not used for detecting the PTP clock cycle amount. For 100 MHz, use an RWS value of 0x2710, for 125 MHz use an RWS value of 0x1F40, for 200 MHz use an RWS value of 0x1388 and for 250 MHz, use an RWS value of 0x0FA0.

Table 351: TAI Global Config 24
Device 0x1F, Register 0xA842

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	TRIGGENAMT_15_0	R/W	0x0	0x0	Trigger Generation Amount bits 15 to 0 of a 32-bit register. This field specifies the PTP Time Application Interface trigger generation time amount. When TrigMode is set to one, the value specified in this field is compared with the PTP Global Timer (TAI offset 0x09 & 0x0A) and when it matches the first time, a pulse is generated on PTP_TRIG whose width is controlled by PulseWidth (TAI offset 0x05). In this mode, there is an internal delay of two Time Stamping Clock periods before the leading edge of the pulse will be seen on the PTP_TRIG output pin. When TrigMode is cleared to zero and register TrigGenTimerSel below is set to 0x0, the value in this field is used as a clock period in Time Stamping Clock period increments to generate an output clock on the PTP_TRIG signal (see TrigPhase in TAI offset 0x00). In this mode, the TrigClkComp amount (TAI offset 0x04) and TrigClkCompSubPs (TAI offset 0x05) gets accumulated once per TrigGenAmt cycle and when this accumulated value exceeds the value specified in TSClkPer, one TSClkPer amount gets added to or subtracted from the next trailing edge of PTP_TRIG clock output. TrigGenAmt smaller than 0x4 is not supported. When TrigMode is cleared to zero and register TrigGenTimerSel below is set to 0x1 or 0x2, the value in this field is used as a clock period in nanoseconds to generate an output clock on the PTP_TRIG signal (see TrigPhase in TAI offset 0x00). In this mode, TrigGenAmt smaller than two times the TSClkPer time and larger than 1 second is not supported. **NOTE:** The clock period may not always be 50 duty cycle due to compensation and may have an inaccuracy of up to 3 ns for 250 MHz PTP Clock and 7 ns for 125 MHz PTP Clock. Note: In 50 duty cycle clock mode the contents of this register can be presented to the hardware at the same time all the other 50 duty cycle registers are. See BlockUpdate in TAI offset 0x00. The upper 16-bits of this register are contained in the register below.

Table 352: TAI Global Config 25
Device 0x1F, Register 0xA843

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	TRIGGENAMT_31_16	R/W	0x0	0x0	Trigger Generation Amount bits 31:16 of a 32-bit register. This field specifies the PTP Time Application Interface trigger generation time amount. See the description above. The lower 16 bits of this register are contained in the register above.

Table 353: TAI Global Config 26
Device 0x1F, Register 0xA844

Bits	Field	Mode	HW Rst	SW Rst	Description
15	TRIGCOMPDIR	R/W	0x0	0x0	Trig Clock Compensation Direction. When the accumulated TrigClkComp amount (below) exceeds the value in TSClkPer (TAI offset 0x01), one TSClkPer amount gets added to or subtracted from the next PTP_TRIG clock output. This bit determines the former or the latter as follows: 0 = Add one TSClkPer to the next PTP_TRIG cycle. 1 = Subtract one TSClkPer from the next PTP_TRIG cycle.
14:0	TRIGCLKCOMP	R/W	0x0	0x0	Trigger mode Clock Compensation Amount. This value is in picoseconds as an unsigned number. This field is used in 50 duty cycle clock mode only (when TrigMode is cleared to zero and TrigGenReq is set to one). This field specifies the remainder amount in ps for the clock that is being generated with a period specified by the TrigGenAmt (TAI offset 0x02 and 0x03). This field must be set as an absolute error number in ps (that is, it is a magnitude difference) regardless if the local clock is too fast or too slow compared to the reference clock. The direction of the clock compensation is configured in the CompDir bit above. In the 50 duty cycle clock mode, this register gets accumulated once per TrigGenAmt cycle and when this accumulated value exceeds the value specified in TSClkPer (TAI offset 0x01), one Time Stamping Clock period amount gets added to or subtracted from the next PTP_TRIG clock output. This requires that the absolute value of TrigClkComp must not exceed the size of the TSClkPer. If it does, the TSClkPer must be adjusted in size (either up or down) until the remainder that remains is less that the TSClkPer and that value gets put into this register. **NOTE:** In 50 duty cycle clock mode, the contents of this register can be presented to the hardware at the same time all the other 50 duty cycle registers are. See BlockUpdate in TAI offset 0x00.

Table 354: TAI Global Config 27
Device 0x1F, Register 0xA845

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	PULSEWIDTH	R/W	0x0	0x0	Pulse width for PTP_TRIG. This pulse width is in units of Time Stamping Clock periods. This specifies the width of the pulse that gets generated on PTP_TRIG (see TrigPhase in TAI offset 0x00) when the one shot pulse mode is selected (TrigMode is set to one and TrigGenReq is set to one). If the PTP_EXTCLK is not used (for example, the internal clock is being used - see PtpExtClk in TAI offset 0x08) the TSClkPer, or Pulse Width unit is 8 ns (assuming the Pulse Width Range, below, is 0x0). **NOTE:** Setting this register to 0x0 will cause unpredictable results.
10:8	PULSEWIDTHRANGE	R/W	0x0	0x0	Pulse Width Range for the PTP_TRIG signal. This register selects the units of time used to define the Pulse Width (above) as follows (each higher numbered selection generates units that are 8x larger than the previous lower numbered selection): 0x0 = 4 ns units for a 250 MHz PTP clock 0x1 = 32 ns units for a 250 MHz PTP clock 0x2 = 256 ns units for a 250 MHz PTP clock 0x3 = 2,048 ns units for a 250 MHz PTP clock 0x4 = 16.384 µs units for a 250 MHz PTP clock 0x5 = 131.072 µs units for a 250 MHz PTP clock 0x6 = 1.049 ms units for a 250 MHz PTP clock 0x7 = 8.388 ms units for a 250 MHz PTP clock The narrowest width is 4 ns (by setting this register to 0x0 and the Pulse Width register, above, to 0x1). The widest width is 125 ms or just a bit over 1/8th second (by setting this register to 0x7 and the Pulse Width register to 0xF). The maximum number is 31,457,280 Time Stamping Clock periods. **NOTE:** All these numbers are multiplied by 2 if the PTP clock is at a rate of 125 MHz instead of its default value of 250 MHz. Basically these numbers are in increments of the Time Stamping Clock period (which could be supplied by an external clock). **NOTE:** When this register is non-zero, the resulting pulse width is 1 clock wider than the math or 8 ns longer for a 125 MHz PTP clock.

Table 354: TAI Global Config 27 (Continued)
Device 0x1F, Register 0xA845

Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	TRIGCLKCOMPSUBPS	R/W	0x0	0x0	Trigger mode Clock Compensation Amount. This value is in Sub Picoseconds as an unsigned number. This field is used in 50 duty cycle clock mode only (when TrigMode is cleared to zero and TrigGenReq is set to one). This field specifies the remainder amount in sub ps increments for the clock that is being generated with a period specified by the TrigGenAmt (TAI offset 0x02 & 0x03). This field must be set as an absolute error number in Sub ps (that is, it is a magnitude difference) regardless if the local clock is too fast or too slow compared to the reference clock. The direction of the clock compensation is configured in the CompDir bit above. Each unit in this register is 1/256th of a ps or approximately 4 femtoseconds (actual number is 3.90625 femtoseconds per unit). In the 50 duty cycle clock mode, this register gets accumulated once per TrigGenAmt cycle and when this accumulated value exceeds on ps, one ps gets added to the accumulated Trig Clock Compensation (TAI offset 0x04). **NOTE:** In 50 duty cycle clock mode, the contents of this register can be presented to the hardware at the same time all the other 50 duty cycle registers are. The writing to this register is used to transfer this data as a block. See BlockUpdate in TAI offset 0x00.

Table 355: TAI Global Config 28
Device 0x1F, Register 0xA846

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	IRLCLKGENAMT_15_0	R/W	0x0	0x0	Ingress Rate Limiter Clock Generation Amount bits 15 to 0. The value in this field is used as a clock period in TSClkPer increments (TAI register 1F.0xA841). In this mode, the IRLClkComp amount (TAI register 1F.0xA847) and IRLClkCompSubPs (TAI register 1F.0xA848) gets accumulated once per IRLClkGenAmt cycle and when this accumulated value exceeds the value specified in TSClkPer, one TSClkPer amount gets added to or subtracted from the next trailing edge of IRL clock. **NOTE:** The default value of this register (along with the IRLClkComp register below) generates a 3.125 ms clock assuming the device's internal 250 MHz clock is being used. When this device's PTP hardware is clocked by an external clock (using PTP_EXTCLK – see PtpExtClk in TAI register 1F.0xA848), this register must be set to the number of PTP external clocks required to generate a 3.125 ms period.

Table 356: TAI Global Config 29
Device 0x1F, Register 0xA847

Bits	Field	Mode	HW Rst	SW Rst	Description
15	IRLCOMPDIR	R/W	0x0	0x0	IRL Clock Compensation Direction. When the accumulated IRLClkComp amount (below) exceeds the value in TSClkPer (TAI offset 0x01), one TSClkPer amount gets added to or subtracted from the next IRL clock. This bit determines the former or the latter as follows: 0 = Add one TSClkPer to the next IRL clock cycle. 1 = Subtract one TSClkPer from the next IRL clock cycle.
14:0	IRLCLKCOMP	R/W	0x0	0x0	IRL Clock Compensation Amount. This value is in picoseconds as an unsigned number. This field specifies the remainder amount in ps for the clock that is being generated with a period specified by the IRLClkGenAmt (TAI offset 0x06). This field must be set as an absolute error number in ps (that is, it is a magnitude difference) regardless if the local clock is too fast or too slow compared to the reference clock. The direction of the clock compensation is configured in the CompDir bit above. This register gets accumulated once per TrigGenAmt cycle and when this accumulated value exceeds the value specified in TSClkPer (TAI offset 0x01), one TSClkPer amount gets added to or subtracted from the next IRL clock. This requires that the absolute value of IRLClkComp must not exceed the size of the TSClkPer. If it does, the TSClkPer must be adjusted in size (either up or down) until the remainder that remains is less that the TSClkPer and that value gets put into this register. **NOTE:** The contents of this register can be presented to the hardware at the same time all the other IRL_Clk registers are. See BlockUpdate in TAI offset 0x00. **NOTE:** The default value of this register (along with the IRLClkGenAmt register above) generates a 3.125 µs clock assuming the device's internal 250 MHz clock is being used. When this device's PTP hardware is clocked by an external clock (using PTP_EXTCLK – see PtpExtClk in TAI offset 0x08) this register must be set to the remainder of whole PTP external clocks required to generate a 3.125 µs period. This value is specified in ps. If hardware accelerated PTP is being used (HWAccel or ExtHWAccel, both in PTP Port offset 0x02), then the external PTP clock input to the PTP hardware must be 125 MHz, so the value of this register must be 0x1388, or 0.625 of an 8000 ps clock period (which is 5000 decimal or 0x1388 hexadecimal).

Table 357: TAI Global Config 30
Device 0x1F, Register 0xA848

Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	IRLCLKCOMPSUBPS	R/W	0x0	0x0	IRL Clock Compensation Amount. This value is in Sub Picoseconds as an unsigned number. This field specifies the remainder amount in sub ps increments for the clock that is being generated with a period specified by the IRLGenAmt (TAI offset 0x06). This field must be set as an absolute error number in Sub ps (that is, it is a magnitude difference) regardless if the local clock is too fast or too slow compared to the reference clock. The direction of the clock compensation is configured in the CompDir bit above. Each unit in this register is 1/256th of a ps or approximately 4 femtoseconds (actual number is 3.90625 femtoseconds per unit). This register gets accumulated once per IRLClkGenAmt cycle and when this accumulated value exceeds on ps, one ps gets added to the accumulated IRL Clock Compensation (TAI offset 0x07). **NOTE:** The contents of this register can be presented to the hardware at the same time all the other IRL_Clk registers are. The writing to this register is used to transfer this data as a block. See BlockUpdate in TAI offset 0x00.

Table 358: TAI Global Status 31
Device 0x1F, Register 0xA849

Bits	Field	Mode	HW Rst	SW Rst	Description
14	CAPTURETRIG	R/W	0x0	0x0	Capture Trig. 0 = Capture PTP_EVREQ pin events. 1 = Capture PTP_TRIG internal events. When this bit is cleared to a zero, the Event Capture register looks at events on the PTP_EVREQ pin. When this bit is set to a one, the Event Capture register looks at events from the waveform generated by PTP_TRIG. This allows observing the rising or falling edge of the PTP_TRIG (the EventPhase register is still active, PTP TAI offset 0x00) without the need of using pins. This is used to insure the edges have not drifted over time so they can be re-aligned if required.
13:12	EVENTCAPFORMAT	R/W	0x0	0x0	Event Capture Format This register is used to select which format of PTP timer to capture into EventCapRegister when an EventReq occurs. 0x0 = Capture 4-byte PTP Global Time 0x1 = Capture 5-byte ToD Time 0x2 = Capture 5-byte 1722 Time 0x3 = Reserved for future use.

Table 358: TAI Global Status 31 (Continued)
Device 0x1F, Register 0xA849

Bits	Field	Mode	HW Rst	SW Rst	Description
11	EVENTCAPDOMAIN	R/W	0x0	0x0	Event Capture Domain When EventCapFormat above is set to 0x1 or 0x2, this register is used to select which Time Array of ToD or 1722 Timer to capture. 0 = Select Time Array 0 to capture. 1 = Select Time Array 1 to capture.
9	EVENTCAPERR	R/W	0x0	0x0	Event Capture Error. This bit gets set by the hardware logic when an EventReq has occurred (see EventPhase in TAI offset 0x00) where the EventCapValid bit, below, is already set to a one and the EventCapOv bit (TAI offset 0x00) is cleared to a zero. This condition could occur if the EventReqs are occurring faster than the local CPU can process them (and clear the EventCapValid bit before the next EventReq). Some number of missed EventReq can be seen in the EventCapCtr, below, if its enabled.
8	EVENTCAPVALID	R/W	0x0	0x0	Event Capture Valid. This bit is set to a one whenever the EventCap (Event Capture – TAI offsets 0x0A and 0x0B) register contains the time of a captured event. Software must clear this bit to a zero to enable the EventCap Register to be able to acquire a subsequent event if the EventCapOv (Event Capture Override – TAI offset 0x00) is not enabled. Clearing this bit to a zero also clears the EventInt (Event Capture Interrupt – PTP Global offset 0x08).
7:0	EVENTCAPCTR	R/W	0x0	0x0	Event Capture Counter. This field is incremented once by each EventReq (see EventPhase in PTP TAI offset 0x00) as long as EventCtrStart (PTP TAI offset 0x00) is set to one. This counter wraps around and can be cleared by writing zeros to it.

Table 359: TAI Global Status 32
Device 0x1F, Register 0xA84A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	EVENTCAPREGISTER_15_0	R/W	0x0	0x0	Event Capture Register bits 15 to 0 of a 40-bit register. When EventCapFormat is set to 0x0, this register captures the value of the PTP Global Timer (TAI offsets 0x0E and 0x0F) when an EventReq (see EventPhase in TAI offset 0x00) has occurred. When EventCapFormat is set to 0x1, this register captures the value of the selected Time Array's (see EventCapDomain above) PTP ToD Timer (PTP Global offset 0x13, 0x14, and 0x15) when an EventReq (see EventPhase in TAI offset 0x00) has occurred. When EventCapFormat is set to 0x2, this register captures the value of the selected Time Array's (see EventCapDomain above) PTP 1722 Timer (PTP Global offset 0x18, 0x19, and 0x1A) when an EventReq (see EventPhase in TAI offset 0x00) has occurred. If the EventCapOv (TAI offset 0x00) is set to a one, then this register indicates the time captured for the last event. When EventCapErr is set to a one, the contents in this register no longer represent the time of the first event. **NOTE:** The maximum jitter for the EventCapRegister time amount with respect to the EventReq on a GPIO pin is one TSClkPer amount. **NOTE:** The minimum EventReq GPIO input signal high or low width has to be equal to or greater than 1.5 times the TSClkPer amount. **NOTE:** For hardware to capture the EventReq on the GPIO input signal, the minimum gap between two consecutive events has to be 150 ns (seven times clk_sysp, in Harmony clk_sysp is 83 MHz or 84.33 ns, but margin has been since Melody at 100 MHz is 120 ns) plus five times the Time Stamping Clock period. The upper 32-bits of this register are contained in the register below.

Table 360: TAI Global Status 33
Device 0x1F, Register 0xA84B

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	EVENTCAPREGISTER_31_16	R/W	0x0	0x0	Event Capture Register bits 31 to 16 of a 40-bit register. This register captures the value of the PTP Global Timer (TAI offsets 0x0E and 0x0F) or the PTP ToD/1722 Timer when an EventReq (see EventPhase in TAI offset 0x00) has occurred. See the previous description.The lower 16 bits of this register are contained in the register above and the upper 16 bits of this register are contained in the register below.

Table 361: TAI Global Config 1
Device 0x1F, Register 0xA84C

Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	EVENTCAPREGISTER_39_32	R/W	0x0	0x0	Event Capture Register bits 39 to 32 of a 40-bit register. This register is only used when EventCapFormat is set to 0x1 or 0x2. This register captures the value of the selected Time Array's (see EventCapDomain above) PTP ToD Timer (PTP Global offset 0x13, 0x14, and 0x15) or PTP 1722 Timer (PTP Global offsets 0x18, 0x19, and 0x1A) when an EventReq (see EventPhase in TAI offset 0x00) has occurred. See the description above. The lower 32 bits of this register are contained in the register above.

Table 362: TAI Global Config 2
Device 0x1F, Register 0xA84E

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PTPGLOBALTIME_15_0	RO	0x0	0x0	Precise Time Protocol Global Timer bits 15 to 0 of a 32-bit register. This indicates the global timer value that is running off of the free running switch core clock. This counter wraps around in hardware. To support synchronization of PTP Global Time between multiple devices in a system, this register gets updated with the value specified in TrigGenAmt when MultiPTPSync is set to a one (TAI offset 0x00) and an EventReq occurs (see EventPhase in TAI offset 0x00). Based on PTP protocol time of day computations, this field can be either incremented or decremented using the TimeIncDecAmt (TAI offset 0x05) by enabling TimeIncDecEn (TAI offset 0x00) and by selecting an increment or a decrement operation using TimeIncDecOp (TAI offset 0x05). This register is updated in the same cycle as when TimeIncDecEn goes high. This register can also be written to for test purposes. The upper 16 bits of this register are contained in the register below.

Table 363: TAI Global Config 3
Device 0x1F, Register 0xA84F

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PTPGLOBALTIME_31_16	RO	0x0	0x0	Precise Time Protocol Global Timer bits 31 to 16 of a 32-bit register. This indicates the global timer value that is running off of the free running switch core clock. This counter wraps around in hardware. See the description above. The lower 16 bits of this register are contained in the register above.

Table 364: TAI Global Config 4
Device 0x1F, Register 0xA850

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	TRIGGENTIME_15_0	R/W	0x0	0x0	Trigger Generation Time bits 15 to 0 of a 40-bit register. When register TrigGenTimerSel is set to 0x0, this field specifies the PTP Global Time (TAI offsets 0x0E & 0x0F) where the first leading edge of PTP_TRIG will occur (with a three TSClkPer latency) when PTP Trig is in the continuous square wave mode (for example, when TrigMode is 0x0, offset 0x00 above) as long as this register's value is non-zero. If its value is zero, the first leading edge of PTP_TRIG will occur when TrigGenReg is set to a one (TAI offset 0x00).This register is also used to for relocking the leading edge of the square wave (see TrigLock in TAI offset 0x00). When register TrigGenTimerSel is set to 0x1 or 0x2, this field specifies the selected Time Array's (See TrigGenDomain below) 5-byte ToD or 1722 time where the first leading edge of PTP_TRIG will occur (with an maximum inaccuracy of 3 ns for 250 MHz PTP Clock or 7 ns for 125 MHz PTP Clock) when PTP Trig is in the continuous square wave mode as long as this register this register's value is non-zero. If its value is zero, then the first leading edge of PTP_TRIG will occur when TrigGenReq is set to a one (TAI offset 0x00). The upper 32 bits of this register are contained in the register below. **NOTE:** When register TrigGenTimerSel is set to 0x0, only lower 32 bits of this register is used for PTP Global Time. When register TrigGenTimerSel is set to 0x1, the lower 4 bytes of this register is used for ToD time nanosecond field, which wraps around at 1 second and the upper 1 byte of this register is used for ToD time second field. When register TrigGenTimer is set to 0x2, all 5 bytes of this register is used for 1722 time in nanosecond. This is a change from the Difference Doc. This new circuit will not always use this register's value to start the first rising edge. If this register = zero, then the time in this register is ignored and the 50 duty cycle square wave will start as soon as it is enabled (just as it did before this circuit was added). Also, if this register's value is zero, then the Trigger Lock Enable will not attempt to lock this clock.

Table 365: TAI Global Config 5
Device 0x1F, Register 0xA851

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	TRIGGENTIME_31_16	R/W	0x0	0x0	Trigger Generation Time bits 31 to 16 of a 40-bit register. See the previous description. The lower 16 bits of this register are contained in the register above.

Table 366: TAI Global Config 6
Device 0x1F, Register 0xA852

Bits	Field	Mode	HW Rst	SW Rst	Description
7	TRIGGENDOMAIN	R/W	0x0	0x0	PTP Trigger Generation Domain When TrigGenTimerSel is set to 0x1 or 0x2, this register is used to select the Time Array of ToD or 1722 Timer for trigger generation function. 0 = Select Time Array 0. 1 = Select Time Array 1.
6:5	TRIGGENTIMERSEL	R/W	0x0	0x0	PTP Trigger Generation Timer Select This register is used to select which format of PTP timer to use for trigger generation function when TrigMode = 0. 0x0 = Trigger Generation clock is based on PTP Global Timer. 0x1 = Trigger Generation clock is based on PTP ToD Timer. 0x2 = Trigger Generation clock is based on PTP 1722 Timer. 0x3 = Reserved for future use.
4	LOCKCORRVALID	R/W	0x0	0x0	Trig Lock Correction Valid. 0 = Trig Lock Correction is not valid or did not occur. 1 = Trig Lock Correction is valid and did occur. When a Trigger Lock is enabled (TAI offset 0x00), this bit is cleared to zero. When the Trigger Lock completes, this bit will be set to a one if and only if a Trigger Lock occurred for PTP_TRIG. In this case, the Lock Correction value below will show the amount of adjustment that was made (if any).
3:0	LOCKCORRECTION	R/W	0x0	0x0	Trig Lock Correction amount. When the TrigLock bit is set to a one (TAI offset 0x00) enabling a potential clock adjustment, these bits are cleared to zero. When the TrigLock bit is cleared to zero (indicating that the requested clock adjustment is now past in time), these bits will reflect the magnitude and direction that was applied to the PTP_TRIG leading edge of the generated clock. A value of zero means no adjustment was necessary. If bit 3 is a one, then the leading edge of the clock was moved n number of clocks earlier in time where n is shown in bits 2:0. If bit 3 is a zero, then the leading edge of the clock was moved n number of clocks later in time where n is shown in bits 2:0.

Table 367: TAI Global Config 7
Device 0x1F, Register 0xA853

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	TRIGGENDELAY	R/W	0x0	0x0	Trigger Generation Delay. This field specifies the number of PTP clocks the PTP_TRIG Delayed waveform is delayed from the PTP_TRIG waveform. A value of 0x0000 is zero clocks delay and if the Delay is greater than the PTP_TRIG cycle time, then the delay is considered zero. This delay time can optional be used by the Qav Shapers as a Deblocking Window (see the TimeAwareDeBlock bit in Qav Port offsets 0x00 to 0x06).

Table 368: TAI Global Config 8
Device 0x1F, Register 0xA854

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	IRLGENTIME_15_0	R/W	0x0	0x0	IRL Generation Time bits 15 to 0 of a 32-bit register. This field specifies the PTP Global Time (TAI offsets 0x0E and 0x0F) where the first leading edge of IRL_Clk will occur (with a three TSClkPer latency) as long as this register's value is non-zero. If its value is zero, the first leading edge of IRL_Clk will occur when IRLClkGenReg is set to a one (TAI offset 0x00). This register is also used to for re-locking the leading edge of the square wave (see TrigLock in TAI offset 0x00). The upper 16-bits of this register are contained in the register below. This circuit will not always use this register's value to start the first rising edge. If this register = zero, then the time in this register is ignored and the 50 duty cycle square wave will start as soon as its enabled (just as it would before this circuit was added). Also, if this register's value is zero. the Trigger Lock Enable will not try to lock this clock.

Table 369: TAI Global Config 9
Device 0x1F, Register 0xA855

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	IRLGENTIME_31_16	R/W	0x0	0x0	IRL Generation Time bits 31:16 of a 32-bit register. See the description above. The lower 16 bits of this register are contained in the register above.

Table 370: TAI Global Config 10
Device 0x1F, Register 0xA856

Bits	Field	Mode	HW Rst	SW Rst	Description
4	IRLLOCKCORRVALID	RO	0x0	0x0	IRL_Clk Lock Correction Valid. 0 = IRL_Clk Lock Correction is not valid or did not occur 1 = IRL_Clk Lock Correction is valid and did occur. When an IRL_Clk Lock is enabled (TAI offset 0x00), this bit is cleared to zero. When the Trigger Lock completes, this bit will be set to a one if and only if a Trigger Lock occurred for IRL_Clk. In this case, the Lock Correction value below will show the amount of adjustment that was made (if any).
3:0	IRLLOCKCORRECTION	RO	0x0	0x0	IRL_Clk Correction amount. When the TrigLock bit is set to a one (TAI offset 0x00) enabling a potential clock adjustment, these bits are cleared to zero. When the TrigLock bit is cleared to zero (indicating that the requested clock adjustment is now past in time), these bits will reflect the magnitude and direction that was applied to the PTP_TRIG 2 leading edge of the generated clock. A value of zero means no adjustment was necessary. If bit 3 is a one, then the leading edge of the clock was moved n number of clocks earlier in time where n is shown in bits 2:0. If bit 3 is a zero, then the leading edge of the clock was moved n number of clocks later in time where n is shown in bits 2:0.

Table 371: TAI Global Config 11
Device 0x1F, Register 0xA857

Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	TRIGGENTIME_39_32	R/W	0x0	0x0	Trigger Generation Time bits 39 to 32 of a 40-bit register. This register is only used when TrigGenTimerSel is set to 0x1 or 0x2. See the register description above at TAI offset 0x10. The lower 32-bits of this register are contained in the register above at TAI offset 0x10 and 0x11.

Table 372: TAI Global Config 12
Device 0x1F, Register 0xA85E

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	RESERVED	R/W	0x1	0x1	RESERVED
13	TRIGWINDOW	R/W	0x0	0x0	Trigger Window. 0 = PTP_TRIG & PTP_1PPS on GPIOs 1 = WINDOW & WINDOW2 (really IRL_Clk) on GPIOs When this bit is cleared to a zero, the PTP_TRIG and PTP_1PPS GPIO options (selection 0x1 and 0x6, respectively) output the waveforms as they are named. When this bit is set to a one, these GPIO options output WINDOW and WINDOW2 (really IRL_Clk) waveforms respectively instead. A Window waveform goes high one clock after the rising edge of the TRIG and goes low one clock after the rising edge of the Delayed TRIG.
12:8	RESERVED	R/W	0x1F	0x1F	RESERVED
7	TRIG2SIGNAL	R/W	0x0	0x0	Triger2 Signal. 0 = PTP_TRIG & PTP_1PPS on GPIOs 1 = PTP_TRIG & IRL_Clk on GPIOs When this bit is cleared to a zero, the PTP_TRIG and PTP_1PPS GPIO options (selection 0x1 and 0x6, respectively) output the waveforms as they are named. When this bit is set to a one, these GPIO options output PTP_TRIG and IRL_Clk waveforms respectively instead. **NOTE:** This bit has no effect if Trig Window (above) is set to a one).
4:0	RESERVED	R/W	0x1F	0x1F	RESERVED

Table 373: TAI Global Config 13
Device 0x1F, Register 0xA85F

Bits	Field	Mode	HW Rst	SW Rst	Description
11	TIMEINCDECOP	R/W	0x0	0x0	Time increment decrement operation. When this bit is set to one, TimeIncDecAmt below is a decrement amount that must be subtracted from the current PTP Global Time Counter when TimeIncDec (TAI offset 0x00) is set to a one. When this bit is cleared to zero, TimeIncDecAmt is an increment amount that needs to be added to the current PTP Global Time Counter when TimeIncDec is set to a one. All updates are completed within the same cycle of TimeIncDec changing state from 0x0 to 0x1. This function has been made hidden as it is bad to change the PTP Global Time as it is used in many blocks that will not know that a step function occurred to this counter.
10:0	TIMEINCDECAMT	R/W	0x0	0x0	Time Increment decrement amount. This field is valid only when TimeIncDec is set to a one. This field specifies the number of units of PTP Global Time that must be incremented or decremented based upon TimeIncDecOp above. This is used for adjusting the PTP Global Time counter value by a certain amount.

Table 374: PTP Global Config 39
Device 0x1F, Register 0xA860

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	PTPETYPE	RO	0x0	0x0	Precise Time Protocol EtherType. All layer 2 PTP frames are recognized using a combination of a specific EtherType and MessageType values (part of the PTP Common Header). This field is used to identify the EtherType on these frames. The MsgTypeEn (specified below in offset 0x01) qualifies the types of frames that the hardware requires to time stamp. For IEEE 802.1AS and IEEE1588 over Layer 2 Ethernet, the EtherType is expected to be programmed to 0x88F7.

Table 375: PTP Global Config 40
Device 0x1F, Register 0xA861

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	MSGTYPEEN	R/W	0x0	0x0	Message Type Time Stamp Enable. MessageType is part of the PTP common header. This is also referred to in some instances as sub-type field. There are PTP frames which must be time stamped, while other PTP frames are not required to be time stamped. This field identifies the PTP frame types that must be time stamped for frames that are not hardware accelerated – see HWAccel in PTP Port offset 0x02). The MessageType read from PTP frames is vectorized[1] and then used to access the appropriate bit in this register. If the selected bit is set to a one, then that frame type will be time stamped both in ingress and egress. Else that frame type will not be time stamped. For example, if MessageType field (in the PTP common header) with a value of 0x4 must be time stamped in hardware, then MsgTypeEn[4] should be set to a one. Then the incoming PTP frames with a MessageTypefield of 0x4 will get time stamped into one of the port's two available arrival capture registers (either PTPArr0Time or PTPArr1Time as identified by TSArrPtr[4] bit below). All outgoing PTP frames with the MessageType field of 0x4 will be timestamped into the Port's PTPDepTime capture register.

Table 376: PTP Global Config 41
Device 0x1F, Register 0xA862

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	TSARRPTR	R/W	0x0	0x0	Time Stamp Arrival Time Capture Pointer. If the incoming PTP frame must be time stamped (based on MsgTypeEn), this field determines whether the hardware logic should use PTPArr0Time or PTPArr1Time for storing the arriving frames' time stamp information. This field corresponds to the sixteen combinations of the vectorized MessageType. For example, if TSArrPtr[2] is set to a one, it indicates to the hardware that if MsgTypeEn [2] is set to a one then PTP frames with MessageType = 0x2 will use PTPArr1Time counter for storing the incoming PTP frames' time stamp. On the contrary: if TSArrPtr[2] is cleared to a zero that indicates to the hardware that if MsgTypeEn[2] is set to a one, then PTP frames with MessageType = 0x2 will use PTPArr0Time counter for storing the incoming PTP frames' time stamp.

Table 377: PTP Global Config 42
Device 0x1F, Register 0xA867

Bits	Field	Mode	HW Rst	SW Rst	Description
15	UPDATE	R/W	0x0	0x0	Update Data. When this bit is set to a one, the data written to bits 7:0 will be loaded into the PTP Global Config register referenced by the Pointer bits below. After the write has occurred, this bit self clears to zero.
14:8	POINTER	R/W	0x0	0x0	Pointer to the desired octet of PTP Global Config. These bits select one of the possible PTP Global Config registers for both read and write operations. A write operation occurs if the Update bit is a one (the registers can be written to by writing this register in a single operation). Otherwise a read of the current Pointer occurs and the data found there is placed in the Data bits below (the desired register can be read by first writing to this register, with Update = 0, and then reading this register). The Pointer bits are used to access the Index registers as follows: 0x00: PTP Mode Register 0x01: PTP External Time Format 0x02: PTP Mode 2 Register 0x01 to 0x02: Reserved for future use 0x03 PTP Mode 3 Register 0x04 to 0x5F: Reserved for future use 0x60 to 0x67: Reserved for future use 0x68 to 0x6F: Reserved for future use 0x70 to 0x77: Reserved for future use 0x78 to 0x7F: Reserved for future use
7:0	DATA	R/W	0x0	0x0	Octet Data of the PTP Global Config register referenced by the Pointer bits above.

Table 378: PTP Status 5
Device 0x1F, Register 0xA868

Bits	Field	Mode	HW Rst	SW Rst	Description
15	TRIGGENINT	RO	0x0	0x0	Trigger generate mode Interrupt. The TrigGenInt bit gets set by the TAI block when the TrigGenIntEn is set to a one (TAI offset 0x00) and when the one shot pulse is generated (TrigMode is set to one in TAI offset 0x00). It gets cleared by the reading of this register.
14	EVENTINT	RO	0x0	0x0	Event Capture Interrupt. This bit gets set by the TAI block when the EventIntEn is set to a one (TAI offset 0x00) and when an EventReq is captured in the EventCap Register. It gets cleared by writing a zero to the EventCapValid register (TAI offset 0x09). **NOTE:** This interrupt bit will also be set to a one, if enabled, whenever the EventCapValid bit (TAI offset 0x09) is set to a one. This allows software to test its interrupt routine.
13:11	Reserved	RO	0x0	0x0	
10:1	PTPINT_10_1	RO	0x0	0x0	Precise Time Protocol Interrupt for Ports 10 to 1. These PTP Interrupt bits gets set for a given port when an incoming PTP frame is time stamped and PTPArrIntEn for that port is set to a one (PTP Port offset 0x02). Similarly, the PTP Interrupt bits get set for a given port when an outgoing PTP frame is time stamped and PTPDepIntEn for that port is set to a one (PTP Port offset 0x02). The hardware logic sets this per port bit based on above criteria and gets cleared upon software reading and clearing the corresponding time counter valid bits that are valid for that port. Bit 1 is for Port 1, bit 2 is for Port 2, and so on.

Table 379: PTP Global Status 6
Device 0x1F, Register 0xA869

Bits	Field	Mode	HW Rst	SW Rst	Description
15:1	PTPINT_26_12	RO	0x0	0x0	Precise Time Protocol Interrupt for Ports 26 to 12. These PTP Interrupt bits gets set for a given port when an incoming PTP frame is time stamped and PTPArrIntEn for that port is set to a one. Similarly, the PTP Interrupt bits get set for a given port when an outgoing PTP frame is time stamped and PTPDepIntEn for that port is set to a one. The hardware logic sets this per port bit based on above criteria and gets cleared upon software reading and clearing the corresponding time counter valid bits that are valid for that port. Bit 1 is for Port 12, bit 2 is for Port 13, and so on. These interrupts are connected to the UpperPortsInt (PTP Global offset 0x08).
0	PTPINT_11	RO	0x0	0x0	Precise Time Protocol Interrupt for Port 11. This PTP Interrupt bit gets set for Port 11 when an incoming PTP frame is time stamped and PTPArrIntEn for Port 11 is set to a one. Similarly, this PTP Interrupt bit gets set for Port 11 when an outgoing PTP frame is time stamped and PTPDepIntEn for Port 11 is set to a one. The hardware logic sets this bit based on above criteria and gets cleared upon software reading and clearing the corresponding time counter valid bits that are valid for Port 11. This interrupt is connected to the UpperPortsInt (PTP Global offset 0x08).

Table 380: PTP Global Time Array 7
Device 0x1F, Register 0xA870

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	TODLOADPT_15_0	R/W	0x0	0x0	Time of Day Load Point Register bits 15 to 0 of a 32-bit register. The ToDLoadPt register is used in multiple ways, but its contents are always relative to the PTP Global Time (all so known as H/W Time) found in TAI Global offsets 0x0E & 0x0F. This register is used as follows in the various ToD Operations:ToD Store All Registers – it is used to determine the instant in time that the selected Time Array is loaded. The load occurs at the instant the PTP Global Time (TAI Global offset 0x0E & 0x0F) matches the contents of this register plus 1 TSClkPer (TAI Global offset 0x01).ToD Capture – it is used to capture the instant in time that the Capture occurred. On each ToD Capture, the contents of this register will be loaded with the current value contained in the PTP Global Time (TAI Global offsets 0x0E & 0x0F). The upper 16-bits of this register are contained in the register below.

Table 381: PTP Global Time Array 8
Device 0x1F, Register 0xA871

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	TODLOADPT_31_16	R/W	0x0	0x0	Time of Day Load Point Register bits 31 to 16 of a 32-bit register. Value to be matched with global timer value – used to either load or capture the TOD. See the description above. The lower 16-bits of this register are contained in the register above.

Table 382: PTP Global Time Array 9
Device 0x1F, Register 0xA872

Bits	Field	Mode	HW Rst	SW Rst	Description
15	TODBUSY	R/W	0x0	0x0	Time of Day Busy. This bit must be set to a one to start a ToD operation (see ToD Op below). Only one ToD operation can be executing at one time so this bit must be zero before setting it to a one. When the requested ToD operation completes, this bit will automatically be cleared to a zero.
14:12	TODOP	R/W	0x0	0x0	Time of Day Opcode. The following ToD Opcodes are supported and are applied to the selected Time Array as indicated as follows: 0x0 = Store Comp register only to selected TimeArray (clean[2]) 0x1 = Store All Registers to selected TimeArray @ ToDLoadPt (dirty[3]) 0x2 = Store Comp register only to selected TimeArray[4] (dirty) 0x3 = Store All Registers to selected TimeArray @ ToDLoadPt[5] (clean) 0x4 = Capture selected TimeArray, Comp=Comp & ToDLoadPt=PTPGT[6] 0x5 = Capture selected TimeArray, Comp=AccErr & ToDLoadPt=PTPGT[7] 0x6 = Reserved for future use 0x7 = Reserved for future use **NOTE:** A Store ToDOp will start the timer if ClkActive below is set to a one.
11:10	RESERVEDTIMEARRAY	R/W	0x0	0x0	Reserved for future use. Reserved for an extra TimeArray bit so that a total of eight Time Arrays can be supported in the future.
9	TIMEARRAY_0	R/W	0x0	0x0	Time Array. The above ToD operation is performed to/from the physical Time Array specified by this register. The device contains multiple independent Time Arrays where each Time Array consists of the following: 10-byte ToD time (PTP Global offsets 0x13 to 0x17), 8-byte 1722 time (PTP Global offset 0x18 to 0x1B), 4-byte Compensation (PTP Global offset 0x1C to 0x1D), 1-byte Domain Number (bits 7:0 below), and a 1-bit Clock Valid (bit 8 below).

Table 382: PTP Global Time Array 9 (Continued)
Device 0x1F, Register 0xA872

Bits	Field	Mode	HW Rst	SW Rst	Description
8	CLKACTIVE	R/W	0x0	0x0	Clock Active. When this bit is set to a one and then stored to a Time Array (by using ToDOp Store All Registers), the selected Time Array will start keeping time using the parameters loaded and that Time Array will be considered active, When this bit is cleared to a zero and then stored to a Time Array, the selected Time Array will stop keeping time and it will be considered inactive. **NOTE:** This bit is transferred to the selected TimeArray on every ToDOp.
7:0	DOMAINNUMBER	R/W	0x0	0x0	Domain Number. This is the IEEE 1588 or IEEE 802.1ASbt frame Domain Number that is to be associated with the selected Time Array. It is used to select which Time Array is to be used when processing PTP frames in hardware. This Domain number will only be used on active Time Arrays (for example, Time Arrays whose ClkActive bit above is set to a one).

Table 383: PTP Global Time Array 10
Device 0x1F, Register 0xA873

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	TODNANO_15_0	R/W	0x0	0x0	Time Array Time of Day, Nanosecond portion, bits 15 to 0 of a 32-bit register. The five ToD registers (at PTP Global offsets 0x13 to 0x17) contain the 10-byte representation of time used in IEEE 1588 and IEEE 802.1AS frames. These registers are used to load this representation of time into the selected Time Array on ToD Store All Registers operations. They contain the selected Time Array's representation of this time after ToD Capture operations complete. The upper 16-bits of this register are contained in the register below.

Table 384: PTP Global Time Array 11
Device 0x1F, Register 0xA874

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	TODNANO_31_16	R/W	0x0	0x0	Time Array Time of Day, Nanosecond portion, bits 31 to 16 of a 32-bit register. See the description above. The lower 16 bits of this register are contained in the register above.

Table 385: PTP Global Time Array 12
Device 0x1F, Register 0xA875

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	TODSEC_15_0	R/W	0x0	0x0	Time Array Time of Day, Seconds portion, bits 15 to 0 of a 48-bit register. See the description above. The upper 32 bits of this register are contained in the registers below.

Table 386: PTP Global Time Array 13
Device 0x1F, Register 0xA876

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	TODSEC_31_16	R/W	0x0	0x0	Time Array Time of Day, Seconds portion, bits 31 to 16 of a 48-bit register. See the description above. The lower 16 bits of this register are contained in the register above. The upper 16 bits of this register are contained in the register below.

Table 387: PTP Global Time Array 14
Device 0x1F, Register 0xA877

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	TODSEC_47_32	R/W	0x0	0x0	Time Array Time of Day, Seconds portion, bits 47 to 32 of a 48-bit register. See the description above. The lower 32 bits of this register are contained in the registers above.

Table 388: PTP Global Time Array 15
Device 0x1F, Register 0xA878

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	NANO_15_0	R/W	0x0	0x0	Time Array 1722 Time of Day in Nanoseconds, bits 15 to 0 of a 64-bit register. The four 1722 ToD registers (at PTP Global offsets 0x18 to 0x1B) contain an 8-byte representation of time used in IEEE 1722 frames (IEEE1722 uses only the lower 32 bits of this time. The 64-bit representation is used in PCIe and it is a simple extension of the IEEE 1722 representation of time that wraps). These registers are used to load this representation of time into the selected Time Array on ToD Store All Registers operations. They contain the selected Time Array's representation of this time after ToD Capture operations complete. The upper 48 bits of this register are contained in the registers below.

Table 389: PTP Global Time Array 16
Device 0x1F, Register 0xA879

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	NANO_31_16	R/W	0x0	0x0	Time Array 1722 Time of Day in Nanoseconds, bits 31 to 16 of a 64-bit register. See the description above. The lower 16 bits of this register are contained in the register above. The upper 32 bits of this register are contained in the registers below.

Table 390: PTP Global Time Array 17
Device 0x1F, Register 0xA87A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	NANO_47_32	R/W	0x0	0x0	Time Array 1722 Time of Day in Nanoseconds, bits 47 to 32 of a 64-bit register. See the description above. The lower 32 bits of this register are contained in the registers above. The upper 16 bits of this register are contained in the register below.

Table 391: PTP Global Time Array 18
Device 0x1F, Register 0xA87B

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	NANO_63_48	R/W	0x0	0x0	Time Array 1722 Time of Day in Nanoseconds, bits 63 to 48 of a 64-bit register. See the description above. The lower 48 bits of this register are contained in the registers above.

Table 392: PTP Global Time Array 19
Device 0x1F, Register 0xA87C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	TODCOMP_15_0	R/W	0x0	0x0	Time Array Time of Day Compensation bits 15 to 0 of a 32-bit register. The two Time of Day Compensation registers (at PTP Global offsets 0x1C or 0x1D) are used to define the PPM difference between the local crystal clocking this PTP block and the PTP Grand Master device that this Time Array is tracking. Bits 30:0 of this register are used to define the difference between these two clocks in increments of 465.661 zeptoseconds (or 4.65661E-19 seconds which is less than a single attosecond. For reference, picoseconds is 10-12, femptoseconds is 10-15, attoseconds is 10-18 and zeptoseconds is 10-21). Set this register to the amount of time needed to be added or subtracted to each local 250 MHz or 125 MHz PTP clock period in order to make it match its associated Grand Master's rate (for example, the PPM difference between the two). A difference of 1 PPM for a 125 MHz local PTP clock is 8 femtoseconds (8.0E-15 seconds) or a setting of 17,182 decimal (0x431E) in this register. The full range of this register (0x7FFF FFFF) results in 1.0 ns of compensation per local PTP Clock. Bit 31 of this register is used to indicate the direction of the difference: 0 = Local clock is slow (need to add the Comp to each cycle). 1 = Local clock is fast (need to subtract the Comp from each cycle). These registers are used to load the needed Compensation to the selected Time Array on ToD Store All Registers and on ToD Store only the Comp registers operations. They contain the selected Time Array's Compensation after a ToD Capture operation using OpCode 0x4 completes. They will contain the lower 31-bits (bit 31 = 0) of the selected Time Array's current Accumulated Error after a ToD Capture operation using OpCode 0x5 completes. When a Time Array is set active, use the ToD Store only the Comp register operation to update any detected changes in the PPM difference between the local crystal and its associated Grand Master. This register keeps track of the sub-ns portion of the Accumulated Error. The ns portion is read back in the lower 2 or 3 bits of the ToD & 1722 Nano Seconds. The upper 16-bits of this register are contained in the register below.

Table 393: PTP Global Time Array 20
Device 0x1F, Register 0xA87D

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	TODCOMP_31_16	R/W	0x0	0x0	Time Array Time of Day Compensation bits 31 to 16 of a 32-bit register. See the description above. The lower 16 bits of this register are contained in the register above.

Table 394: PTP Global Time Array 21
Device 0x1F, Register 0xA87E

Bits	Field	Mode	HW Rst	SW Rst	Description
15:12	ONEPPSWIDTH	R/W	0x0	0x0	Pulse Width for the 1 Pulse Per Second on the Second signal. This register defines the pulse width of the selected 1 PPS signal (see 1 PPS Select bits below) in the units defined by the 1 PPS Width Range bits below. A value of 0x1 in this register selects 1 unit. A value of 0x0 selects 0 units (for example, stops the clock).
11	ALTTCAMTIMESEL	R/W	0x0	0x0	Alternate TCAM Time Select. 0 = Use PTP_TRIG, IRL_CLK & Seconds selection for TCAM Time Sel 1 = Use 1722 16 µs to 536 µs selection for TCAM Time Sel This bit is used to select which set of 16 options are used for the TCAM Time Sel, below.
10:8	ONEPPSWIDTHRANGE	R/W	0x0	0x0	Pulse Width Range for the 1 Pulse Per Second on the Second signal. This register selects the units of time used to define the 1PPS Width (above) as follows (each higher numbered selection generates units that are 8x larger than the previous lower numbered selection): 0x0 = 4 ns units for a 250 MHz PTP clock 0x1 = 32 ns units for a 250 MHz PTP clock 0x2 = 256 ns units for a 250 MHz PTP clock 0x3 = 2,048 ns units for a 250 MHz PTP clock 0x4 = 16.384 µs units for a 250 MHz PTP clock 0x5 = 131.072 µs units for a 250 MHz PTP clock 0x6 = 1.049 ms units for a 250 MHz PTP clock 0x7 = 8.388 ms units for a 250 MHz PTP clock The narrowest width is 4 ns (by setting this register to 0x0 and the 1 PPS Width register to 0x1). The widest width is 125 ms or just a bit over 1/8th second (by setting this register to 0x7 and the 1 PPS Width register to 0xF). **NOTE:** All these numbers are multiplied by 2 if the PTP clock is at a rate of 125 MHz instead of its default value of 250 MHz. Basically, these numbers are in increments of the Time Stamping Clock period (which could be supplied by an external clock).

Table 394: PTP Global Time Array 21 (Continued)
Device 0x1F, Register 0xA87E

Bits	Field	Mode	HW Rst	SW Rst	Description
7:4	TCAMTIMESEL	R/W	0x0	0x0	TCAM Time Select. This register, along with the Alt TCAM Time Sel register, above, is used to select the TCAM Time Key (TCAM Page 0 offset 0x02) as follows: Alt TCAM Time Sel = 0 Alt TCAM Time Sel = 1 0x0 = PTP_TRIG = 32.768 µs 0x1 = IRLClk = 65.536 µs 0x2 = Reserved = 131.072 µs 0x3 = Reserved = 262.144 µs 0x4 = Reserved = 524.288 µs 0x5 = Reserved = 1.049 ms 0x6 = Reserved = 2.097 ms 0x7 = Reserved = 4.194 ms 0x8 = 2.000 Sec = 8.389 ms 0x9 = 4.000 Sec = 16.777 ms 0xA = 8.000 Sec = 33.554 ms 0xB = 16.000 Sec = 67.109 ms 0xC = 32.000 Sec = 134.218 ms 0xD = 64.000 Sec = 268.436 ms 0xE = 128.000 Sec = 536.871 ms 0xF = 256.000 Sec = 1.073s The default selection is PTP_TRIG. This signal can be a one-shot at a specific time or a square wave (~50 duty cycle) of a specific frequency and phase. It is configured in PTP TAI offsets 0x00 to 0x05 and 0x10 and 0x11. This signal is also used to generate the timing for the Qbv Time Aware Shaper. IRLClk can be a square wave (~50 duty cycle) of a specific frequency and it is configured in PTP TAI offsets 0x00, and 0x06 to 0x08. This signal is also used to generate IRL's ITSM reference windows. The 2 to 256 second frequency selections are square wave (~50 duty cycle) signals that come from the ToD Seconds register (PTP Global offset 0x15). Bits 0 to 7 The 33 microsecond to 1.073 second frequency selections are square wave (~50 duty cycle) signals that come from the 1722 Nano Seconds register (PTP Global offset 0x18 & 0x19). Bits 14 to 29
3	ONEPPSPHASE	R/W	0x0	0x0	Phase of the 1 Pulse Per Second on the Second signal. This register defines the phase of the selected 1 PPS signal (see 1 PPS Select bits below). When this bit is set to a one, the leading edge of the 1 PPS signal (the edge that occurs at the exact start of each second) is the falling edge of the signal. When this bit is cleared to a zero, the leading edge of the 1 PPS signal is the rising edge of the signal.
2	TIMEARRAYSEL	R/W	0x0	0x0	Time Array Select The above TCAM Time Select operation is performed to/from the physical Time Array specified by this register.

Table 394: PTP Global Time Array 21 (Continued)
Device 0x1F, Register 0xA87E

Bits	Field	Mode	HW Rst	SW Rst	Description
1	RESERVEDFORONEPPSSELECT	R/W	0x0	0x0	Reserved for Select for the 1 Pulse Per Second on the Second signal. This register selects the Time Array that is used to generate the 1 PPS signal. Any of the Time Arrays can be selected, but only one at a time can be selected. The selected Time Array will output the leading edge of the 1 PPS signal when its ToD Seconds (PTP Global offsets 0x15 to 0x17) gets incremented. This increment occurs whenever the Time Array's ToD Nano Seconds (PTP Global offsets 0x13 & 0x14) reaches 1,000,000 ns such that this 1 PPS signal occurs at the exact start of each second. The selected 1 PPS signal is available on any of the GPIO pins (this signal replaces the previous PTP_TRIG2 signal in the GPIO matrix).
0	ONEPPSSELECT	R/W	0x0	0x0	Select which 1PPS to configure. This register selects which Time Array's 1PPS to configure using the above registers 1PPSWidth, 1PPSWidthRange and 1PPSPhase. 0 = Configure Time Arrays 0's 1PPS. 1 = Configure Time Arrays 1's 1PPS.

3.11 MMAC Registers

Table 395: Summary Register Map for MMAC Registers

Register Name	Register Description	Register Address	Table and Page
SLC_CFG_GEN	MMAC Slice Configuration Register	Device 0x1F, Register 0x8000	Table 396, p. 303
PAUSE_CTL	Control Register for Flow Control by Pause Frame	Device 0x1F, Register 0x800E	Table 397, p. 304
EDB_THRESH	Egress Drop Buffer Threshold for XON/XOFF	Device 0x1F, Register 0x8010	Table 398, p. 305
IDB_THRESH	Ingress Drop Buffer Threshold for XON/XOFF	Device 0x1F, Register 0x8012	Table 399, p. 305
CFG_VLAN_ET	Configure IPG between packets	Device 0x1F, Register 0x8048	Table 400, p. 306
QOS_FC	QoS / Flow Control Register	Device 0x1F, Register 0x80A4	Table 401, p. 306
QOS_ETHERTYPE	Configure Ether Type for QoS	Device 0x1F, Register 0x80A6	Table 402, p. 306
LINK_RESET_CFG	Soft Reset for individual MMAC sub-blocks	Device 0x1F, Register 0x80B2	Table 403, p. 307
SMC_MAC_PREEMPT_CTRL	System MAC Preemption Control Register	Device 0x1F, Register 0x80DE	Table 404, p. 308
WMC_MAC_PREEMPT_CTRL	Wire MAC Preemption Control Register	Device 0x1F, Register 0x80EA	Table 405, p. 308
GOODOCTETS	Sys MAC RX MIB – Good Frame Octets	Device 0x1F, Register 0x9000	Table 406, p. 309
ERROROCTETS	Sys MAC RX MIB – Bad Frame Octets	Device 0x1F, Register 0x9004	Table 407, p. 309
JABBER	Sys MAC RX MIB – Packet > MTU w/ Bad CRC	Device 0x1F, Register 0x9008	Table 408, p. 309
FRAGMENT	Sys MAC RX MIB – Packet < 64B w/ Bad CRC	Device 0x1F, Register 0x900C	Table 409, p. 309
UNDERSIZE	Sys MAC RX MIB – Packet < 64B w/ Good CRC	Device 0x1F, Register 0x9010	Table 410, p. 309
OVERSIZE	Sys MAC RX MIB – Packet > MTU w/ Good CRC	Device 0x1F, Register 0x9014	Table 411, p. 309
RXERROR	Sys MAC RX MIB – Seq, code, symbol errors	Device 0x1F, Register 0x9018	Table 412, p. 309
CRCERR_TXUNDERRUN	Sys MAC RX MIB – Bad CRC	Device 0x1F, Register 0x901C	Table 413, p. 310
RXOVERRUN_BADFC	Sys MAC RX MIB – Bad Flow Control Packets	Device 0x1F, Register 0x9020	Table 414, p. 310
GOODPKTS	Sys MAC RX MIB – Good Packets	Device 0x1F, Register 0x9024	Table 415, p. 310
FCPKT	Sys MAC RX MIB – Flow Control Packets	Device 0x1F, Register 0x9028	Table 416, p. 310

Table 395: Summary Register Map for MMAC Registers (Continued)

Register Name	Register Description	Register Address	Table and Page
BROADCAST	Sys MAC RX MIB – Broadcast Packets	Device 0x1F, Register 0x902C	Table 417, p. 310
MULTICAST	Sys MAC RX MIB – Multicast Packets	Device 0x1F, Register 0x9030	Table 418, p. 310
INPASSEMBLYERR	Sys MAC RX MIB – Preemption Assembly Errors	Device 0x1F, Register 0x9034	Table 419, p. 310
INPFRAMES	Sys MAC RX MIB – Preemption Packets	Device 0x1F, Register 0x9038	Table 420, p. 311
INPFRAGS	Sys MAC RX MIB – Preemption Fragments	Device 0x1F, Register 0x903C	Table 421, p. 311
INPBADFRAGS	Sys MAC RX MIB – Preemption Fragments with Bad CRC	Device 0x1F, Register 0x9040	Table 422, p. 311
GOODOCTETS	Sys MAC TX MIB – Good Frame Octets	Device 0x1F, Register 0x9080	Table 406, p. 309
ERROROCTETS	Sys MAC TX MIB – Bad Frame Octets	Device 0x1F, Register 0x9084	Table 407, p. 309
JABBER	Sys MAC TX MIB – Packet > MTU w/ Bad CRC	Device 0x1F, Register 0x9088	Table 408, p. 309
FRAGMENT	Sys MAC TX MIB – Packet < 64B w/ Bad CRC	Device 0x1F, Register 0x908C	Table 409, p. 309
UNDERSIZE	Sys MAC TX MIB – Packet < 64B w/ Good CRC	Device 0x1F, Register 0x9090	Table 410, p. 309
OVERSIZE	Sys MAC TX MIB – Packet > MTU w/ Good CRC	Device 0x1F, Register 0x9094	Table 411, p. 309
RXERROR	Sys MAC TX MIB – Seq, code, symbol errors	Device 0x1F, Register 0x9098	Table 412, p. 309
CRCERR_TXUNDERRUN	Sys MAC TX MIB – Bad CRC	Device 0x1F, Register 0x909C	Table 413, p. 310
RXOVERRUN_BADFC	Sys MAC TX MIB – Bad Flow Control Packets	Device 0x1F, Register 0x90A0	Table 414, p. 310
GOODPKTS	Sys MAC TX MIB – Good Packets	Device 0x1F, Register 0x90A4	Table 415, p. 310
FCPKT	Sys MAC TX MIB – Flow Control Packets	Device 0x1F, Register 0x90A8	Table 416, p. 310
BROADCAST	Sys MAC TX MIB – Broadcast Packets	Device 0x1F, Register 0x90AC	Table 417, p. 310
MULTICAST	Sys MAC TX MIB – Multicast Packets	Device 0x1F, Register 0x90B0	Table 418, p. 310
OUTPFRAGS	Sys MAC TX MIB – Preemption Fragments	Device 0x1F, Register 0x90B4	Table 436, p. 313
OUTPFRAMES	Sys MAC TX MIB – Preemption Packets	Device 0x1F, Register 0x90B8	Table 437, p. 313
DROPPEDPKTS	Wire MAC RX MIB – all dropped packets	Device 0x1F, Register 0x9184	Table 438, p. 313

Table 395: Summary Register Map for MMAC Registers (Continued)

Register Name	Register Description	Register Address	Table and Page
OCTETS	Wire MAC RX MIB – all packet octets	Device 0x1F, Register 0x9188	Table 439, p. 313
JABBER	Wire MAC RX MIB – Packet > MTU w/ Bad CRC	Device 0x1F, Register 0x918C	Table 440, p. 313
FRAGMENT	Wire MAC RX MIB – Packet < 64B w/ Bad CRC	Device 0x1F, Register 0x9190	Table 441, p. 314
UNDERSIZE	Wire MAC RX MIB – Packet < 64B w/ Good CRC	Device 0x1F, Register 0x9194	Table 442, p. 314
RXERROR	Wire MAC RX MIB – Seq, code, symbol errors	Device 0x1F, Register 0x9198	Table 443, p. 314
CRCERROR	Wire MAC RX MIB – Bad CRC	Device 0x1F, Register 0x919C	Table 444, p. 314
FCPKTS	Wire MAC RX MIB – Bad Flow Control Packets	Device 0x1F, Register 0x91A0	Table 445, p. 314
BROADCASTPKTS	Wire MAC RX MIB – Broadcast Packets	Device 0x1F, Register 0x91A4	Table 446, p. 314
MULTICASTPKTS	Wire MAC RX MIB – Multi-cast Packets	Device 0x1F, Register 0x91A8	Table 447, p. 314
INPASSEMBLYERR	Wire MAC RX MIB – Pre-emption Assembly Errors	Device 0x1F, Register 0x91DC	Table 448, p. 315
INPFRAMES	Wire MAC RX MIB – Pre-emption Packets	Device 0x1F, Register 0x91E0	Table 449, p. 315
INPFRAGS	Wire MAC RX MIB – Pre-emption Fragments	Device 0x1F, Register 0x91E4	Table 450, p. 315
INPBADFRAGS	Wire MAC RX MIB – Pre-emption Fragments with Bad CRC	Device 0x1F, Register 0x91E8	Table 451, p. 315
PKTS	Wire MAC TX MIB – All packets	Device 0x1F, Register 0x9380	Table 452, p. 315
DROPPEDPKTS	Wire MAC TX MIB – all dropped packets	Device 0x1F, Register 0x9384	Table 453, p. 315
OCTETS	Wire MAC TX MIB – all packet octets	Device 0x1F, Register 0x9388	Table 454, p. 315
JABBER	Wire MAC TX MIB – Packet > MTU w/ Bad CRC	Device 0x1F, Register 0x938C	Table 455, p. 316
FRAGMENT	Wire MAC TX MIB – Packet < 64B w/ Bad CRC	Device 0x1F, Register 0x9390	Table 456, p. 316
UNDERSIZE	Wire MAC TX MIB – Packet < 64B w/ Good CRC	Device 0x1F, Register 0x9394	Table 457, p. 316
RXERROR	Wire MAC TX MIB – Seq, code, symbol errors	Device 0x1F, Register 0x9398	Table 458, p. 316
CRCERROR	Wire MAC TX MIB – Bad CRC	Device 0x1F, Register 0x939C	Table 459, p. 316

Table 395: Summary Register Map for MMAC Registers (Continued)

Register Name	Register Description	Register Address	Table and Page
FCPKTS	Wire MAC TX MIB – Bad Flow Control Packets	Device 0x1F, Register 0x93A0	Table 460, p. 316
BROADCASTPKTS	Wire MAC TX MIB – Broadcast Packets	Device 0x1F, Register 0x93A4	Table 461, p. 316
MULTICASTPKTS	Wire MAC TX MIB – Multi-cast Packets	Device 0x1F, Register 0x93A8	Table 462, p. 317
OUTPFRAGS	Wire MAC TX MIB – Pre-emption Fragments	Device 0x1F, Register 0x93DC	Table 463, p. 317
OUTPFRAMES	Wire MAC TX MIB – Pre-emption Fragments with Bad CRC	Device 0x1F, Register 0x93E0	Table 464, p. 317

Table 396: SLC_CFG_GEN
Device 0x1F, Register 0x8000

Bits	Field	Mode	HW Rst	SW Rst	Description
31	TEST_INT	R/W	0x0	0x0	Test interrupt. When set, triggers interrupt in global_intr register. This bit must be cleared prior to clearing the interrupt in global_ intr, or the interrupt will re-trigger.
30	HALT_ON_ERROR	R/W	0x1	0x1	If any of the memories receives a double-bit error, then the pipeline is halted and signal an interrupt is signaled.
29	WMC_STAT_TX_ CLR_RD	R/W	0x1	0x1	WMC Cfg clr on read
28	WMC_STAT_RX_ CLR_RD	R/W	0x1	0x1	WMC Cfg clr on read
27	SMC_STAT_TX_CLR_ RD	R/W	0x1	0x1	SMC Cfg clr on read
26	SMC_STAT_RX_CLR_ RD	R/W	0x1	0x1	SMC Cfg clr on read
25	L_EXGMII_EN	R/W	0x1	0x1	Local exgmii en. It will be ANDed with input port signals.
24	SMC_ANEG_EN	R/W	0x0	0x0	Enable auto negotiation for system MAC
23	WMC_ANEG_EN	R/W	0x1	0x1	Enable auto-negotiation for wire MAC
22	MIB_TIMEOUT_CFG	R/W	0x1	0x1	Enable MIB watchdog timeout config reg
21	GLB_INTR_EN	R/W	0x0	0x0	Global interrupt enable
20	SER_TIMEOUT_CFG	R/W	0x1	0x1	Enable Serial watchdog timeout config reg
19	SER_RESET	R/W	0x0	0x0	Reset Serial SM reg
18	SMC_LOAD_CFG	R/W	0x0	0x0	Reset Sys MAC config regs
17	WMC_LOAD_CFG	R/W	0x0	0x0	Reset Wire MAC config regs
16	SIG_LOAD_CFG	R/W	0x0	0x0	Reset Sigaba config regs

Table 396: SLC_CFG_GEN (Continued)
Device 0x1F, Register 0x8000

Bits	Field	Mode	HW Rst	SW Rst	Description
15	IDB_RESET	R/W	0x0	0x0	Reserved
14	EDB_RESET	R/W	0x0	0x0	Reserved
13	SMC_CFG_PKT_ UNDER_SIZE	R/W	0x0	0x0	System XGMAC enable receive under_size packets less then 64 oct with good CRC
12	WMC_CFG_PKT_ UNDER_SIZE	R/W	0x0	0x0	Wire XGMAC enable receive under_size packets less then 64 oct with good CRC
11	SMC_CFG_STRIP_ CRC	R/W	0x0	0x0	System MAC strip crc (last 4 bytes of packet)
10	WMC_CFG_STRIP_ CRC	R/W	0x0	0x0	Wire MAC strip crc (last 4 bytes of packet)
9	SMC_CFG_ADD_ CRC	R/W	0x0	0x0	System XGMAC addition crc to the packet
8	WMC_CFG_ADD_ CRC	R/W	0x0	0x0	Wire XGMAC addition CRC to the packet
7:6	SMC_MUX_FC_EN	R/W	0x0	0x0	Flow control enable for system MAC mux. When set to 1, the mux will backpressure (flow control) the sender. When set to 0, the mux will drop packets arriving on this interface if the other interface is busy.
5:4	WMC_MUX_FC_EN	R/W	0x0	0x0	Flow control enable for wire MAC mux. When set to 1, the mux will backpressure (flow control) the sender. When set to 0, the mux will drop packets arriving on this interface if the other interface is busy.
3	IGR_SF_ENABLE	R/W	0x1	0x1	Store and forward enable for ingress drop FIFO.
2	EGR_SF_ENABLE	R/W	0x1	0x1	Store and forward enable for egress drop FIFO.
1	SMC_XG_SELECT	R/W	0x1	0x1	Set to 1, low_latency/low_power is determined by PTP CSR low_latency_mode (31.A008.4). Set to 0 to override PTP CSR low_latency_mode, low_ latency or low_power will be determined by MMAC CSR bit wmc_xg_select instead
0	WMC_XG_SELECT	R/W	0x1	0x1	When smc_xg_select=0, set to 1 to select low_latency_ mode, 0 to select low_power_mode

Table 397: PAUSE_CTL
Device 0x1F, Register 0x800E

Bits	Field	Mode	HW Rst	SW Rst	Description
11:8	CFG_MAC_SPEED	R/W	0x2	0x2	MAC speed config for both wire MAC and SMC MAC.
7	SMC_PERIODIC_FC_ TRIG	R/W	0x0	0x0	No description

Table 397: PAUSE_CTL
Device 0x1F, Register 0x800E

Bits	Field	Mode	HW Rst	SW Rst	Description
6	WMC_PERIODIC_FC_TRIG	R/W	0x0	0x0	No description
5	SMC_FC_VAL	R/W	0x0	0x0	Value to force flow control. 0=off 1=on
4	WMC_FC_VAL	R/W	0x0	0x0	Value to force flow control. 0=off 1=on
3:2	SMC_PAUSE_SRC	R/W	0x1	0x1	Source for system MAC pause input. 0=Pause from WMC RX (LATENCY_REDUCTION_FC) or (only if smc_fc_val==0) Egress Drop Buffer almost full 1=Pause from SMC RX 2=EDB almost full (CLOSED_LOOP_FC) 3=force by smc_fc_val
1:0	WMC_PAUSE_SRC	R/W	0x0	0x0	Source for wire MAC pause input. 0=Pause from WMC RX 1=Pause from SMC RX (LATENCY_REDUCTION_FC) or (only if wmc_fc_val==0) Ingress Drop Buffer almost full 2=IDB almost full (CLOSED_LOOP_FC) 3=force by wmc_fc_val

Table 398: EDB_THRESH
Device 0x1F, Register 0x8010

Bits	Field	Mode	HW Rst	SW Rst	Description
23:12	EDB_ON_THRESH	R/W	0x080	0x080	Egress Drop buffer XON threshold, defaults to XON on on-quarter full. Threshold is in units of 16B
11:0	EDB_OFF_THRESH	R/W	0x180	0x180	Egress Drop buffer XOFF threshold, defaults to XOFF on three-quarter. Threshold is in units of 16B.

Table 399: IDB_THRESH
Device 0x1F, Register 0x8012

Bits	Field	Mode	HW Rst	SW Rst	Description
23:12	IDB_ON_THRESH	R/W	0x080	0x080	Ingress Drop buffer XON threshold, defaults to XON on, on-quarter full. Threshold is in units of 16B
11:0	IDB_OFF_THRESH	R/W	0x180	0x180	Ingress Drop buffer XOFF threshold, defaults to XOFF on three-quarter. Threshold is in units of 16B

Table 400: CFG_VLAN_ET
Device 0x1F, Register 0x8048

Bits	Field	Mode	HW Rst	SW Rst	Description
15:13	CFG_IPG_FRAG2	R/W	0x3	0x3	Configure min IPG between mid-frag and its follower, which is equal to (cfg_ipg_cnt+3) - 8*(cfg_ipg_frag2+1); When cfg_ipg_frag2 is set to 7, min ipg in all cases list above is equal to cfg_ipg_cnt+3
12	CFG_SCH_EN	R/W	0x1	0x1	Set 1 to enable the scheduler to enforce cfg_ipg_cnt; otherwise, egr_sys_ifg_t2 is applied.
11:10	CFG_IPG_FRAG1	R/W	0x1	0x1	Configure min IPG between the last frag and its following pkt/frag, which is equal to (cfg_ipg_cnt+3) - 8*(cfg_ipg_frag1+1)
9:8	CFG_IPG_FRAG0	R/W	0x1	0x1	Configure min IPG between the 1st frag and its following pkt/frag, which is equal to (cfg_ipg_cnt+3) - 8*(cfg_ipg_frag0+1)
7:0	CFG_IPG_CNT	R/W	0x29	0x29	Configure min IPG at MMAC to PTP, which is equal to cfg_ipg_cnt+3

Table 401: QOS_FC
Device 0x1F, Register 0x80A4

Bits	Field	Mode	HW Rst	SW Rst	Description
5:3	QOS_DEFAULT_CLASS	R/W	0x0	0x0	When qos_stats is enable, default entry for pkt without VLAN tag.
2	QOS_STATS_EN	R/W	0x0	0x0	QoS stats enable
1	QBB_EN	R/W	0x0	0x0	802.1Qbb flow control enable. Automatically drop Qbb pause frame
0	X_DROP_EN	R/W	0x0	0x0	802.3x flow control pkt drop enable

Table 402: QOS_ETHERTYPE
Device 0x1F, Register 0x80A6

Bits	Field	Mode	HW Rst	SW Rst	Description
31:16	DOT1S_TAG	R/W	0x8100	0x8100	802.1s ethertype
15:0	DOT1Q_TAG	R/W	0x8100	0x8100	802.1Q ethertype

Table 403: LINK_RESET_CFG
Device 0x1F, Register 0x80B2

Bits	Field	Mode	HW Rst	SW Rst	Description
26	TAI_HRESET_CFG	R/W	0x0	0x0	TAI hard reset override.
25	CFG_CLR_RESET	R/W	0x1	0x1	When this bit is set, clear the statistics when soft reset
24	PTL_RST_EN	R/W	0x1	0x1	When this bit is set, enable state machine partially soft-reset, which allow register access during soft reset is active.
23	BLK_RST_EN	R/W	0x0	0x0	When this bit is set, block soft-reset during register access, which allow register access during soft reset is active.
22	IDB_RESET_CFG	R/W	0x1	0x1	Ingress Path Drop Buffer soft reset
21	EDB_RESET_CFG	R/W	0x1	0x1	Egress Path Drop Buffer soft reset
20	IPTP_RESET_CFG	R/W	0x0	0x0	Ingress Path PTP soft reset
19	EPTP_RESET_CFG	R/W	0x0	0x0	Egress Path PTP soft reset
18	IMCS_RESET_CFG	R/W	0x1	0x1	Ingress Path MCS soft reset
17	EMCS_RESET_CFG	R/W	0x1	0x1	Egress Path MCS soft reset
16	WMC_MAC_RESET_CORE_CFG	R/W	0x1	0x1	WMC MAC core logic soft reset
15	SMC_MAC_RESET_CORE_CFG	R/W	0x1	0x1	SMC MAC core logic soft reset
14	WMC_MAC_TX_RESET_CFG	R/W	0x1	0x1	WMC Tx MAC logic soft reset
13	WMC_MAC_RX_RESET_CFG	R/W	0x1	0x1	WMC Rx MAC logic soft reset
12	SMC_MAC_TX_RESET_CFG	R/W	0x1	0x1	SMC Tx MAC logic soft reset
11	SMC_MAC_RX_RESET_CFG	R/W	0x1	0x1	SMC Rx MAC logic soft reset
10	SMC_CORE_EIF_RESET_CFG	R/W	0x1	0x1	Egress Path SMC I/F core clock domain logic soft reset
9	SMC_CORE_IIF_RESET_CFG	R/W	0x1	0x1	Ingress Path SMC I/F core clock domain logic soft reset
8	WMC_CORE_EIF_RESET_CFG	R/W	0x1	0x1	Egress Path WMC I/F core clock domain logic soft reset
7	WMC_CORE_IIF_RESET_CFG	R/W	0x1	0x1	Ingress Path WMC I/F core clock domain logic soft reset
6	SMC_MAC_EIF_RESET_CFG	R/W	0x1	0x1	Egress Path SMC I/F Mac clock domain logic soft reset

Table 403: LINK_RESET_CFG (Continued)
Device 0x1F, Register 0x80B2

Bits	Field	Mode	HW Rst	SW Rst	Description
5	SMC_MAC_IIF_ RESET_CFG	R/W	0x1	0x1	Ingress Path SMC I/F Mac clock domain logic soft reset
4	WMC_MAC_EIF_ RESET_CFG	R/W	0x1	0x1	Egress Path WMC I/F Mac clock domain logic soft reset
3	WMC_MAC_IIF_ RESET_CFG	R/W	0x1	0x1	Ingress Path WMC I/F Mac clock domain logic soft reset
2	ENDL_RESET_CFG	R/W	0x1	0x1	Egress Path NDL soft reset
1	INDL_RESET_CFG	R/W	0x1	0x1	Ingress Path NDL soft reset
0	MISC_RESET_CFG	R/W	0x1	0x1	Misc Block Soft Reset

Table 404: SMC_MAC_PREEMPT_CTRL
Device 0x1F, Register 0x80DE

Bits	Field	Mode	HW Rst	SW Rst	Description
11	SMC_PREEMPT_ HOLD	R/W	0x0	0x0	See xgmac specification.
10	SMC_PREEMPT_EN	R/W	0x0	0x0	See xgmac specification.
9	SMC_PREEMPT_ DROP	R/W	0x0	0x0	See xgmac specification.
8	SMC_PREEMPT_ VERIFY	R/W	0x0	0x0	See xgmac specification.
7:0	SMC_PREEMPT_ VERIFY_TIMER	R/W	0x00	0x00	See xgmac specification.

Table 405: WMC_MAC_PREEMPT_CTRL
Device 0x1F, Register 0x80EA

Bits	Field	Mode	HW Rst	SW Rst	Description
11	WMC_PREEMPT_ HOLD	R/W	0x0	0x0	See xgmac spec
10	WMC_PREEMPT_EN	R/W	0x0	0x0	See xgmac spec
9	WMC_PREEMPT_ DROP	R/W	0x0	0x0	See xgmac spec
8	WMC_PREEMPT_ VERIFY	R/W	0x0	0x0	See xgmac spec
7:0	WMC_PREEMPT_ VERIFY_TIMER	R/W	0x00	0x00	See xgmac spec

Table 406: GOODOCTETS
Device 0x1F, Register 0x9000

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	GOODOCTETS	R/W	0x0	0x0	Good frame octets

Table 407: ERROROCTETS
Device 0x1F, Register 0x9004

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	ERROROCTETS	R/W	0x0	0x0	Bad frame octets

Table 408: JABBER
Device 0x1F, Register 0x9008

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	JABBER	R/W	0x0	0x0	Frame of size MTU and bad CRC

Table 409: FRAGMENT
Device 0x1F, Register 0x900C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	FRAGMENT	R/W	0x0	0x0	Frame 48B with bad CRC

Table 410: UNDERSIZE
Device 0x1F, Register 0x9010

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	UNDERSIZE	R/W	0x0	0x0	Frame 48B with good CRC

Table 411: OVERSIZE
Device 0x1F, Register 0x9014

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	OVERSIZE	R/W	0x0	0x0	Frame of size MTU and good CRC

Table 412: RXERROR
Device 0x1F, Register 0x9018

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RXERROR	R/W	0x0	0x0	Sequence, code, symbol errors

Table 413: CRCERR_TXUNDERRUN
Device 0x1F, Register 0x901C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	CRCERR_TXUNDER-RUN	R/W	0x0	0x0	CRC error

Table 414: RXOVERRUN_BADFC
Device 0x1F, Register 0x9020

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RXOVERRUN_ BADFC	R/W	0x0	0x0	Overrun or bad flow control packet

Table 415: GOODPKTS
Device 0x1F, Register 0x9024

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	GOODPKTS	R/W	0x0	0x0	Number of good packets

Table 416: FCPKT
Device 0x1F, Register 0x9028

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	FCPKT	R/W	0x0	0x0	Flow control packet

Table 417: BROADCAST
Device 0x1F, Register 0x902C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	BROADCAST	R/W	0x0	0x0	Number of broadcast packets

Table 418: MULTICAST
Device 0x1F, Register 0x9030

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	MULTICAST	R/W	0x0	0x0	Number of multicast packets

Table 419: INPASSEMBLYERR
Device 0x1F, Register 0x9034

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	INPASSEMBLYERR	R/W	0x0	0x0	See description in section 9 of IP doc rev1.3

Table 420: INPFRAMES
Device 0x1F, Register 0x9038

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	INPFRAMES	R/W	0x0	0x0	See description in section 9 of IP doc rev1.3

Table 421: INPFRAGS
Device 0x1F, Register 0x903C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	INPFRAGS	R/W	0x0	0x0	See description in section 9 of IP doc rev1.3

Table 422: INPBADFRAGS
Device 0x1F, Register 0x9040

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	INPBADFRAGS	R/W	0x0	0x0	See description in section 9 of IP doc rev1.3

Table 423: GOODOCTETS
Device 0x1F, Register 0x9080

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	GOODOCTETS	R/W	0x0	0x0	Good frame octets

Table 424: ERROROCTETS
Device 0x1F, Register 0x9084

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	ERROROCTETS	R/W	0x0	0x0	Bad frame octets

Table 425: JABBER
Device 0x1F, Register 0x9088

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	JABBER	R/W	0x0	0x0	Frame of size MTU and bad CRC

Table 426: FRAGMENT
Device 0x1F, Register 0x908C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	FRAGMENT	R/W	0x0	0x0	Frame 48B with bad CRC

Table 427: UNDERSIZE
Device 0x1F, Register 0x9090

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	UNDERSIZE	R/W	0x0	0x0	Frame 48B with good CRC

Table 428: OVERSIZE
Device 0x1F, Register 0x9094

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	OVERSIZE	R/W	0x0	0x0	Frame of size MTU and good CRC

Table 429: RXERROR
Device 0x1F, Register 0x9098

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RXERROR	R/W	0x0	0x0	Sequence, code, symbol errors

Table 430: CRCERR_TXUNDERRUN
Device 0x1F, Register 0x909C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	CRCERR_TXUNDER-RUN	R/W	0x0	0x0	CRC error

Table 431: RXOVERRUN_BADFC
Device 0x1F, Register 0x90A0

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RXOVERRUN_ BADFC	R/W	0x0	0x0	Overrun or bad flow control packet

Table 432: GOODPKTS
Device 0x1F, Register 0x90A4

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	GOODPKTS	R/W	0x0	0x0	Number of good packets

Table 433: FCPKT
Device 0x1F, Register 0x90A8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	FCPKT	R/W	0x0	0x0	Flow control packet

Table 434: BROADCAST
Device 0x1F, Register 0x90AC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	BROADCAST	R/W	0x0	0x0	Number of broadcast packets

Table 435: MULTICAST
Device 0x1F, Register 0x90B0

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	MULTICAST	R/W	0x0	0x0	Number of multicast packets

Table 436: OUTPFRAGS
Device 0x1F, Register 0x90B4

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	OUTPFRAGS	R/W	0x0	0x0	See description in section 9 of IP doc rev1.3

Table 437: OUTPFRAMES
Device 0x1F, Register 0x90B8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	OUTPFRAMES	R/W	0x0	0x0	See description in section 9 of IP doc rev1.3

Table 438: DROPPEDPKTS
Device 0x1F, Register 0x9184

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	DROPPEDPKTS	R/W	0x0	0x0	dropped packets

Table 439: OCTETS
Device 0x1F, Register 0x9188

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	OCTETS	R/W	0x0	0x0	All packets octets

Table 440: JABBER
Device 0x1F, Register 0x918C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	JABBER	R/W	0x0	0x0	Packet MTU and bad CRC

Table 441: FRAGMENT
Device 0x1F, Register 0x9190

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	FRAGMENT	R/W	0x0	0x0	Packet 64B and bad CRC

Table 442: UNDERSIZE
Device 0x1F, Register 0x9194

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	UNDERSIZE	R/W	0x0	0x0	Packet 64B and good CRC

Table 443: RXERROR
Device 0x1F, Register 0x9198

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RXERROR	R/W	0x0	0x0	Sequence, code, symbol errors

Table 444: CRCERROR
Device 0x1F, Register 0x919C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	CRCERROR	R/W	0x0	0x0	CRC error packet

Table 445: FCPKTS
Device 0x1F, Register 0x91A0

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	FCPKTS	R/W	0x0	0x0	flow control packet

Table 446: BROADCASTPKTS
Device 0x1F, Register 0x91A4

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	BROADCASTPKTS	R/W	0x0	0x0	number of broadcast packets

Table 447: MULTICASTPKTS
Device 0x1F, Register 0x91A8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	MULTICASTPKTS	R/W	0x0	0x0	number of multicast packets

Table 448: INPASSEMBLYERR
Device 0x1F, Register 0x91DC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	INPASSEMBLYERR	R/W	0x0	0x0	See description in section 9 of IP doc rev1.3.

Table 449: INPFRAMES
Device 0x1F, Register 0x91E0

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	INPFRAMES	R/W	0x0	0x0	See description in section 9 of IP doc rev1.3.

Table 450: INPFRAGS
Device 0x1F, Register 0x91E4

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	INPFRAGS	R/W	0x0	0x0	See description in section 9 of IP doc rev1.3.

Table 451: INPBADFRAGS
Device 0x1F, Register 0x91E8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	INPBADFRAGS	R/W	0x0	0x0	See description in section 9 of IP doc rev1.3.

Table 452: PKTS
Device 0x1F, Register 0x9380

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	PKTS	R/W	0x0	0x0	All packets

Table 453: DROPPEDPKTS
Device 0x1F, Register 0x9384

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	DROPPEDPKTS	R/W	0x0	0x0	dropped packets

Table 454: OCTETS
Device 0x1F, Register 0x9388

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	OCTETS	R/W	0x0	0x0	All packets octets

Table 455: JABBER
Device 0x1F, Register 0x938C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	JABBER	R/W	0x0	0x0	Packet MTU and bad CRC

Table 456: FRAGMENT
Device 0x1F, Register 0x9390

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	FRAGMENT	R/W	0x0	0x0	Packet 64B and bad CRC

Table 457: UNDERSIZE
Device 0x1F, Register 0x9394

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	UNDERSIZE	R/W	0x0	0x0	Packet 64B and good CRC

Table 458: RXERROR
Device 0x1F, Register 0x9398

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RXERROR	R/W	0x0	0x0	sequence, code, symbol errors

Table 459: CRCERROR
Device 0x1F, Register 0x939C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	CRCERROR	R/W	0x0	0x0	CRC error packet

Table 460: FCPKTS
Device 0x1F, Register 0x93A0

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	FCPKTS	R/W	0x0	0x0	flow control packet

Table 461: BROADCASTPKTS
Device 0x1F, Register 0x93A4

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	BROADCASTPKTS	R/W	0x0	0x0	Number of broadcast packets

Table 462: MULTICASTPKTS
Device 0x1F, Register 0x93A8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	MULTICASTPKTS	R/W	0x0	0x0	Number of multicast packets

Table 463: OUTPFRAGS
Device 0x1F, Register 0x93DC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	OUTPFRAGS	R/W	0x0	0x0	See description in section 9 of IP doc rev1.3.

Table 464: OUTPFRAMES
Device 0x1F, Register 0x93E0

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	OUTPFRAMES	R/W	0x0	0x0	See description in section 9 of IP doc rev1.3.

3.12 MACsec Registers

Table 465: MACsec Summary Register Map

Register Name	Register Description	Register Address	Table and Page
PORT_CONFIG_0	Configure MACsec Packet Header Parser	Device 0x1F, Register 0x0004	Table 466, p. 341
CHANNEL_CONFIG_0	Bypass MACsec for Express Packets-	Device 0x1F, Register 0x0006	Table 467, p. 342
CHANNEL_CONFIG_1	Bypass MACsec for Pre-emption Packets	Device 0x1F, Register 0x0008	Table 468, p. 342
Registers for Packet Assembly Block in the Ingress path (PAB_RX)			
DELAY_CFG_0	Configure MACsec for fixed latency	Device 0x1F, Register 0x0288	Table 469, p. 342
Registers for Packet Assembly Block in the Egress path (PAB_TX)			
DELAY_CFG_0	Configure MACsec for fixed latency	Device 0x1F, Register 0x0308	Table 469, p. 342
Registers for Header Parsing & Extraction Block in the Ingress path (PEX_RX)			
PEX_CONFIGURATION	Packet Parser and Extractor Configuration	Device 0x1F, Register 0x0388	Table 471, p. 343
CUSTOM_TAG_0	Custom Tag Configuration Register 0	Device 0x1F, Register 0x038A	Table 472, p. 344
CUSTOM_TAG_1	Custom Tag Configuration Register 1	Device 0x1F, Register 0x038C	Table 473, p. 344
CUSTOM_TAG_2	Custom Tag Configuration Register 2	Device 0x1F, Register 0x038E	Table 474, p. 344
CUSTOM_TAG_3	Custom Tag Configuration Register 3	Device 0x1F, Register 0x0390	Table 475, p. 345
CUSTOM_TAG_4	Custom Tag Configuration Register 4	Device 0x1F, Register 0x0392	Table 476, p. 345
CUSTOM_TAG_5	Custom Tag Configuration Register 5	Device 0x1F, Register 0x0394	Table 477, p. 346
CUSTOM_TAG_6	Custom Tag Configuration Register 6	Device 0x1F, Register 0x0396	Table 478, p. 346
CUSTOM_TAG_7	Custom Tag Configuration Register 7	Device 0x1F, Register 0x0398	Table 479, p. 347
MPLS_CFG_0	MPLS stack configuration 0	Device 0x1F, Register 0x039C	Table 480, p. 347
MPLS_CFG_1	MPLS stack configuration 1	Device 0x1F, Register 0x039E	Table 481, p. 347
MPLS_CFG_2	MPLS stack configuration 2	Device 0x1F, Register 0x03A0	Table 482, p. 348
MPLS_CFG_3	MPLS stack configuration 3	Device 0x1F, Register 0x03A2	Table 483, p. 348
SECTAG_CFG	Configuration for SecTAG tags	Device 0x1F, Register 0x03A4	Table 484, p. 348
RULE_ETYPE_CFG_0	Ether Type 0 for control packet matching	Device 0x1F, Register 0x03A8	Table 485, p. 348
RULE_ETYPE_CFG_1	Ether Type 1 for control packet matching	Device 0x1F, Register 0x03AA	Table 486, p. 348

Table 465: MACsec Summary Register Map (Continued)

Register Name	Register Description	Register Address	Table and Page
RULE_ETYPE_CFG_2	Ether Type 2 for control packet matching	Device 0x1F, Register 0x03AC	Table 487, p. 348
RULE_ETYPE_CFG_3	Ether Type 3 for control packet matching	Device 0x1F, Register 0x03AE	Table 488, p. 349
RULE_ETYPE_CFG_4	Ether Type 4 for control packet matching	Device 0x1F, Register 0x03B0	Table 489, p. 349
RULE_ETYPE_CFG_5	Ether Type 5 for control packet matching	Device 0x1F, Register 0x03B2	Table 490, p. 349
RULE_ETYPE_CFG_6	Ether Type 6 for control packet matching	Device 0x1F, Register 0x03B4	Table 491, p. 349
RULE_ETYPE_CFG_7	Ether Type 7 for control packet matching	Device 0x1F, Register 0x03B6	Table 492, p. 349
RULE_DA_0	DA address 0 for control packet matching	Device 0x1F, Register 0x03B8	Table 493, p. 349
RULE_DA_1	DA address 1 for control packet matching	Device 0x1F, Register 0x03BC	Table 494, p. 350
RULE_DA_2	DA address 2 for control packet matching	Device 0x1F, Register 0x03C0	Table 495, p. 350
RULE_DA_3	DA address 3 for control packet matching	Device 0x1F, Register 0x03C4	Table 496, p. 350
RULE_DA_4	DA address 4 for control packet matching	Device 0x1F, Register 0x03C8	Table 497, p. 350
RULE_DA_5	DA address 5 for control packet matching	Device 0x1F, Register 0x03CC	Table 498, p. 350
RULE_DA_6	DA address 6 for control packet matching	Device 0x1F, Register 0x03D0	Table 499, p. 351
RULE_DA_7	DA address 7 for control packet matching	Device 0x1F, Register 0x03D4	Table 500, p. 351
RULE_DA_RANGE_MIN_0	Minimum DA address range 0 for control packet matching	Device 0x1F, Register 0x03D8	Table 501, p. 351
RULE_DA_RANGE_MAX_0	Maximum DA address range 0 for control packet matching	Device 0x1F, Register 0x03DC	Table 502, p. 351
RULE_DA_RANGE_MIN_1	Minimum DA address range 1 for control packet matching	Device 0x1F, Register 0x03E8	Table 503, p. 351
RULE_DA_RANGE_MAX_1	Maximum DA address range 1 for control packet matching	Device 0x1F, Register 0x03EC	Table 504, p. 352
RULE_DA_RANGE_MIN_2	Minimum DA address range 2 for control packet matching	Device 0x1F, Register 0x03F8	Table 505, p. 352
RULE_DA_RANGE_MAX_2	Maximum DA address range 2 for control packet matching	Device 0x1F, Register 0x03FC	Table 506, p. 352

Table 465: MACsec Summary Register Map (Continued)

Register Name	Register Description	Register Address	Table and Page
RULE_DA_RANGE_MIN_3	Minimum DA address range 3 for control packet matching	Device 0x1F, Register 0x0408	Table 507, p. 352
RULE_DA_RANGE_MAX_3	Maximum DA address range 3 for control packet matching	Device 0x1F, Register 0x040C	Table 508, p. 353
RULE_COMBO_MIN_0	Min DA in DA + ET Combo Rule 0 for control packet matching	Device 0x1F, Register 0x0410	Table 509, p. 353
RULE_COMBO_MAX_0	Max DA in DA + ET Combo Rule 0 for control packet matching	Device 0x1F, Register 0x0414	Table 510, p. 353
RULE_COMBO_ET_0	Ether Type in DA + ET Combo Rule 0 for control packet matching	Device 0x1F, Register 0x0418	Table 511, p. 353
RULE_COMBO_MIN_1	Min DA in DA + ET Combo Rule 1 for control packet matching	Device 0x1F, Register 0x0424	Table 512, p. 354
RULE_COMBO_MAX_1	Max DA in DA + ET Combo Rule 1 for control packet matching	Device 0x1F, Register 0x0428	Table 513, p. 354
RULE_COMBO_ET_1	Ether Type in DA + ET Combo Rule 1 for control packet matching	Device 0x1F, Register 0x042C	Table 514, p. 354
RULE_COMBO_MIN_2	Min DA in DA + ET Combo Rule 2 for control packet matching	Device 0x1F, Register 0x0438	Table 515, p. 354
RULE_COMBO_MAX_2	Max DA in DA + ET Combo Rule 2 for control packet matching	Device 0x1F, Register 0x043C	Table 516, p. 354
RULE_COMBO_ET_2	Ether Type in DA + ET Combo Rule 2 for control packet matching	Device 0x1F, Register 0x0440Device 0x1F, Register 0x0440	Table 517, p. 355
RULE_COMBO_MIN_3	Min DA in DA + ET Combo Rule 3 for control packet matching	Device 0x1F, Register 0x044C	Table 518, p. 355
RULE_COMBO_MAX_3	Max DA in DA + ET Combo Rule 3 for control packet matching	Device 0x1F, Register 0x0450	Table 519, p. 355
RULE_COMBO_ET_3	Ether Type in DA + ET Combo Rule 3 for control packet matching	Device 0x1F, Register 0x0454	Table 520, p. 355
RULE_MAC	MAC address for MAC-specific protocol matching	Device 0x1F, Register 0x0458	Table 521, p. 356
RULE_ENABLE	Enable bits for rule based control packet matching	Device 0x1F, Register 0x045C	Table 522, p. 356
ETYPE_ENABLE	Enable bits for Ether Types matching	Device 0x1F, Register 0x045E	Table 523, p. 356

Table 465: MACsec Summary Register Map (Continued)

Register Name	Register Description	Register Address	Table and Page
Registers for Header Parsing & Extraction Block in the Ingress path (PEX_TX)			
PEX_CONFIGURATION	Packet Parser and Extractor Configuration	Device 0x1F, Register 0x0488	Table 524, p. 357
CUSTOM_TAG_0	Custom Tag Configuration Register 0	Device 0x1F, Register 0x048A	Table 525, p. 357
CUSTOM_TAG_1	Custom Tag Configuration Register 1	Device 0x1F, Register 0x048C	Table 526, p. 357
CUSTOM_TAG_2	Custom Tag Configuration Register 2	Device 0x1F, Register 0x048E	Table 527, p. 358
CUSTOM_TAG_3	Custom Tag Configuration Register 3	Device 0x1F, Register 0x0490	Table 528, p. 358
CUSTOM_TAG_4	Custom Tag Configuration Register 4	Device 0x1F, Register 0x0492	Table 529, p. 359
CUSTOM_TAG_5	Custom Tag Configuration Register 5	Device 0x1F, Register 0x0494	Table 530, p. 359
CUSTOM_TAG_6	Custom Tag Configuration Register 6	Device 0x1F, Register 0x0496	Table 531, p. 360
CUSTOM_TAG_7	Custom Tag Configuration Register 7	Device 0x1F, Register 0x0498	Table 532, p. 360
MPLS_CFG_0	MPLS stack configuration 0	Device 0x1F, Register 0x049C	Table 533, p. 360
MPLS_CFG_1	MPLS stack configuration 1	Device 0x1F, Register 0x049E	Table 534, p. 361
MPLS_CFG_2	MPLS stack configuration 2	Device 0x1F, Register 0x04A0	Table 535, p. 361
MPLS_CFG_3	MPLS stack configuration 3	Device 0x1F, Register 0x04A2	Table 536, p. 361
SECTAG_CFG	Configuration for SecTAG tags	Device 0x1F, Register 0x04A4	Table 537, p. 361
RULE_ETYPE_CFG_0	Ether Type 0 for control packet matching	Device 0x1F, Register 0x04A8	Table 538, p. 361
RULE_ETYPE_CFG_1	Ether Type 1 for control packet matching	Device 0x1F, Register 0x04AA	Table 539, p. 361
RULE_ETYPE_CFG_2	Ether Type 2 for control packet matching	Device 0x1F, Register 0x04AC	Table 540, p. 362
RULE_ETYPE_CFG_3	Ether Type 3 for control packet matching	Device 0x1F, Register 0x04AE	Table 541, p. 362
RULE_ETYPE_CFG_4	Ether Type 4 for control packet matching	Device 0x1F, Register 0x04B0	Table 542, p. 362
RULE_ETYPE_CFG_5	Ether Type 5 for control packet matching	Device 0x1F, Register 0x04B2	Table 543, p. 362
RULE_ETYPE_CFG_6	Ether Type 6 for control packet matching	Device 0x1F, Register 0x04B4	Table 544, p. 362
RULE_ETYPE_CFG_7	Ether Type 7 for control packet matching	Device 0x1F, Register 0x04B6	Table 545, p. 362
RULE_DA_0	DA address 0 for control packet matching	Device 0x1F, Register 0x04B8	Table 546, p. 363
RULE_DA_1	DA address 1 for control packet matching	Device 0x1F, Register 0x04BC	Table 547, p. 363

Table 465: MACsec Summary Register Map (Continued)

Register Name	Register Description	Register Address	Table and Page
RULE_DA_2	DA address 2 for control packet matching	Device 0x1F, Register 0x04C0	Table 548, p. 363
RULE_DA_3	DA address 3 for control packet matching	Device 0x1F, Register 0x04C4	Table 549, p. 363
RULE_DA_4	DA address 4 for control packet matching	Device 0x1F, Register 0x04C8	Table 550, p. 363
RULE_DA_5	DA address 5 for control packet matching	Device 0x1F, Register 0x04CC	Table 551, p. 364
RULE_DA_6	DA address 6 for control packet matching	Device 0x1F, Register 0x04D0	Table 552, p. 364
RULE_DA_7	DA address 7 for control packet matching	Device 0x1F, Register 0x04D4	Table 553, p. 364
RULE_DA_RANGE_MIN_0	Minimum DA address range 0 for control packet matching	Device 0x1F, Register 0x04D8	Table 554, p. 364
RULE_DA_RANGE_MAX_0	Maximum DA address range 0 for control packet matching	Device 0x1F, Register 0x04DC	Table 555, p. 364
RULE_DA_RANGE_MIN_1	Minimum DA address range 1 for control packet matching	Device 0x1F, Register 0x04E8	Table 556, p. 365
RULE_DA_RANGE_MAX_1	Maximum DA address range 1 for control packet matching	Device 0x1F, Register 0x04EC	Table 557, p. 365
RULE_DA_RANGE_MIN_2	Minimum DA address range 2 for control packet matching	Device 0x1F, Register 0x04F8	Table 558, p. 365
RULE_DA_RANGE_MAX_2	Maximum DA address range 2 for control packet matching	Device 0x1F, Register 0x04FC	Table 559, p. 365
RULE_DA_RANGE_MIN_3	Minimum DA address range 3 for control packet matching	Device 0x1F, Register 0x0508	Table 560, p. 366
RULE_DA_RANGE_MAX_3	Maximum DA address range 3 for control packet matching	Device 0x1F, Register 0x050C	Table 561, p. 366
RULE_COMBO_MIN_0	Min DA in DA + ET Combo Rule 0 for control packet matching	Device 0x1F, Register 0x0510	Table 562, p. 366
RULE_COMBO_MAX_0	Max DA in DA + ET Combo Rule 0 for control packet matching	Device 0x1F, Register 0x0514	Table 563, p. 366
RULE_COMBO_ET_0	Ether Type in DA + ET Combo Rule 0 for control packet matching	Device 0x1F, Register 0x0518	Table 564, p. 367
RULE_COMBO_MIN_1	Min DA in DA + ET Combo Rule 1 for control packet matching	Device 0x1F, Register 0x0524	Table 565, p. 367

Table 465: MACsec Summary Register Map (Continued)

Register Name	Register Description	Register Address	Table and Page
RULE_COMBO_MAX_1	Max DA in DA + ET Combo Rule 1 for control packet matching	Device 0x1F, Register 0x0528	Table 566, p. 367
RULE_COMBO_ET_1	Ether Type in DA + ET Combo Rule 1 for control packet matching	Device 0x1F, Register 0x052C	Table 567, p. 367
RULE_COMBO_MIN_2	Min DA in DA + ET Combo Rule 2 for control packet matching	Device 0x1F, Register 0x0538	Table 568, p. 367
RULE_COMBO_MAX_2	Max DA in DA + ET Combo Rule 2 for control packet matching	Device 0x1F, Register 0x053C	Table 569, p. 368
RULE_COMBO_ET_2	Ether Type in DA + ET Combo Rule 2 for control packet matching	Device 0x1F, Register 0x0540	Table 570, p. 368
RULE_COMBO_MIN_3	Min DA in DA + ET Combo Rule 3 for control packet matching	Device 0x1F, Register 0x054C	Table 571, p. 368
RULE_COMBO_MAX_3	Max DA in DA + ET Combo Rule 3 for control packet matching	Device 0x1F, Register 0x0550	Table 572, p. 368
RULE_COMBO_ET_3	Ether Type in DA + ET Combo Rule 3 for control packet matching	Device 0x1F, Register 0x0554	Table 573, p. 368
RULE_MAC	MAC address for MAC-specific protocol matching	Device 0x1F, Register 0x0558	Table 574, p. 369
RULE_ENABLE	Enable bits for rule based control packet matching	Device 0x1F, Register 0x055C	Table 575, p. 369
ETYPE_ENABLE	Enable bits for Ether Types matching	Device 0x1F, Register 0x055E	Table 576, p. 369
Registers for Header Parsing & Extraction Block in the Ingress path (PEX_TX)			
AUTO_REKEY_ENABLE_0	SC auto rekey Enable	Device 0x1F, Register 0x1998	Table 636, p. 393
TX_PORT_CFG_0	MACsec SecTAG Ether Type Configuration	Device 0x1F, Register 0x199A	Table 637, p. 394
XPN_THRESHOLD	64-bit XPN Threshold to trigger Interrupt when the transmitted packet's 64-bit XPN hits or exceeds this value	Device 0x1F, Register 0x199C	Table 638, p. 394
PN_THRESHOLD	32-bit PN Threshold to trigger Interrupt when the transmitted packet's 32-bit PN hits or exceeds this value	Device 0x1F, Register 0x19A0	Table 639, p. 394

Table 465: MACsec Summary Register Map (Continued)

Register Name	Register Description	Register Address	Table and Page
SECY_MAP_MEM0	SecY MAP Memory (aka Flow-ID policy/map) for Flow 0 The matching index obtained from the Flow-ID TCAM is used to obtain a corresponding Flow-ID policy from this memory. This table supports an N:1 mapping of Flow-IDs to SecY policies. The Flow-ID Map is also used to identify control packets per Flow-ID based on a more complicated set of lookups than is provided by the rules-based control packet classifier.	Device 0x1F, Register 0x19B0	Table 642, p. 395
SECY_MAP_MEM1	SecY MAP Memory for Flow 1	Device 0x1F, Register 0x19B8	Table 643, p. 395
SECY_MAP_MEM2	SecY MAP Memory for Flow 2	Device 0x1F, Register 0x19C0	Table 644, p. 395
SECY_MAP_MEM3	SecY MAP Memory for Flow 3	Device 0x1F, Register 0x19C8	Table 645, p. 396
SECY_PLCY_MEM0	SecY Policy Memory for Flow 0. The SecY Policy Table is indexed by the SecY obtained from the SecY Map table above.	Device 0x1F, Register 0x19F0	Table 646, p. 396
SECY_PLCY_MEM1	SecY Policy Memory for Flow 1	Device 0x1F, Register 0x19F4	Table 647, p. 397
SECY_PLCY_MEM2	SecY Policy Memory for Flow 2	Device 0x1F, Register 0x19F8	Table 648, p. 399
SECY_PLCY_MEM3	SecY Policy Memory for Flow 3	Device 0x1F, Register 0x19FC	Table 649, p. 400
TX_SA_ACTIVE_0	Active SA indicator for SC 0 to determine which of 2 possible SAs associated to the corresponding SC is currently the active SA. If set, then sa_index1 in SA_MAP_MEM is the currently active SA index. If cleared, the sa_index0 in SA_MAP_MEM is the currently active SA index.	Device 0x1F, Register 0x1A10	Table 650, p. 401
TX_SA_ACTIVE_1	Active SA indicator for SC 1	Device 0x1F, Register 0x1A12	Table 651, p. 401
TX_SA_ACTIVE_2	Active SA indicator for SC 2	Device 0x1F, Register 0x1A14	Table 652, p. 401
TX_SA_ACTIVE_3	Active SA indicator for SC 3	Device 0x1F, Register 0x1A16	Table 653, p. 401

Table 465: MACsec Summary Register Map (Continued)

Register Name	Register Description	Register Address	Table and Page
SA_INDEX0_VLD_0	SA index0 valid for SC 0. The valid in this register qualifies the corresponding SC's SA index0 in each SA_MAP_MEM entry. Although these bits can only be set by SW, each valid bit can be automatically cleared by HW when either 1) auto-rekey is enabled and the PN threshold for the SA index has been reached, meaning that current SA index0 is no longer valid or 2) when the PN rolls over to all-zeros or 3) the SC/SA timer was enabled and has expired. Note that these registers are programmed per SC just like the TX SA_MAP_MEM.	Device 0x1F, Register 0x1A20	Table 654, p. 402
SA_INDEX0_VLD_1	SA index0 valid for SC 1	Device 0x1F, Register 0x1A22	Table 655, p. 402
SA_INDEX0_VLD_2	SA index0 valid for SC 2	Device 0x1F, Register 0x1A24	Table 656, p. 402
SA_INDEX0_VLD_3	SA index0 valid for SC 3	Device 0x1F, Register 0x1A26	Table 657, p. 402
SA_INDEX1_VLD_0	SA index1 valid for SC 0	Device 0x1F, Register 0x1A30	Table 658, p. 402
SA_INDEX1_VLD_1	SA index1 valid for SC 1	Device 0x1F, Register 0x1A32	Table 659, p. 403
SA_INDEX1_VLD_2	SA index1 valid for SC 2	Device 0x1F, Register 0x1A34	Table 660, p. 403
SA_INDEX1_VLD_3	SA index1 valid for SC 3	Device 0x1F, Register 0x1A36	Table 661, p. 403
SA_MAP_MEM0	SA MAP Memory for SC 0. The SC index is used to address this memory to obtain 2 possible SA induces to use. The one to use is determined by tx_sa_active[SC]. Associated with each sa_index0 and sa_index1 is a corresponding sa_index0_vld (registers) and sa_index1_vld (registers).	Device 0x1F, Register 0x1A40	Table 662, p. 403
SA_MAP_MEM1	SA MAP Memory for SC 1.	Device 0x1F, Register 0x1A44	Table 663, p. 403
SA_MAP_MEM2	SA MAP Memory for SC 2.	Device 0x1F, Register 0x1A48	Table 664, p. 404
SA_MAP_MEM3	SA MAP Memory for SC 3.	Device 0x1F, Register 0x1A4C	Table 665, p. 404

Table 465: MACsec Summary Register Map (Continued)

Register Name	Register Description	Register Address	Table and Page
SA_PLCY_MEM0	SA Policy (SAK) Memory 0. The SA Policy (SAK) table provides the various Key and Salt values required to decrypt the packet. The table is indexed by the SA Index read from the SA Map.	Device 0x1F, Register 0x1A80	Table 666, p. 404
SA_PLCY_MEM1	SA Policy (SAK) Memory 1	Device 0x1F, Register 0x1AC0	Table 667, p. 404
SA_PLCY_MEM2	SA Policy (SAK) Memory 2	Device 0x1F, Register 0x1B00	Table 668, p. 405
SA_PLCY_MEM3	SA Policy (SAK) Memory 3	Device 0x1F, Register 0x1B40	Table 669, p. 405
SA_PLCY_MEM4	SA Policy (SAK) Memory 4	Device 0x1F, Register 0x1B80	Table 670, p. 406
SA_PLCY_MEM5	SA Policy (SAK) Memory 5	Device 0x1F, Register 0x1BC0	Table 671, p. 407
SA_PLCY_MEM6	SA Policy (SAK) Memory 6	Device 0x1F, Register 0x1C00	Table 672, p. 407
SA_PLCY_MEM7	SA Policy (SAK) Memory 7	Device 0x1F, Register 0x1C40	Table 673, p. 408
SA_PN_TABLE_MEM0	PN Table Memory 0 The Egress PN Table keeps track of the next PN value to insert into an outgoing packet on the corresponding SA. The next_PN must be configured by SW prior to it being used. However HW will update it as a packet is transmitted on that SA.	Device 0x1F, Register 0x1E80	Table 674, p. 408
SA_PN_TABLE_MEM1	PN Table Memory 1	Device 0x1F, Register 0x1E84	Table 675, p. 408
SA_PN_TABLE_MEM2	PN Table Memory 2	Device 0x1F, Register 0x1E88	Table 676, p. 408
SA_PN_TABLE_MEM3	PN Table Memory 3	Device 0x1F, Register 0x1E8C	Table 677, p. 409
SA_PN_TABLE_MEM4	PN Table Memory 4	Device 0x1F, Register 0x1E90	Table 678, p. 409
SA_PN_TABLE_MEM5	PN Table Memory 5	Device 0x1F, Register 0x1E94	Table 679, p. 409
SA_PN_TABLE_MEM6	PN Table Memory 6	Device 0x1F, Register 0x1E98	Table 680, p. 409
SA_PN_TABLE_MEM7	PN Table Memory 7	Device 0x1F, Register 0x1E9C	Table 681, p. 409
TX_FLOWID_TCAM_ENABLE_0	Flow ID TCAM enable For a TCAM entry to be considered in the search/compare function, the corresponding TCAM entry must be enabled (set to 1). When disabled, the corresponding TCAM entry is ignored in the search/compare.	Device 0x1F, Register 0x1EC0	Table 682, p. 410

Table 465: MACsec Summary Register Map (Continued)

Register Name	Register Description	Register Address	Table and Page
FLOWID_TCAM_DATA0	TCAM Entry for Flow 0 With standard MACsec, a SA can only be associated with a port. WAN based MACsec allows different flows on the same port to support different SecYs and SA greatly expanding upon its usefulness. The first step in the classification process involves performing a lookup in the Flow-ID TCAM based on the information extracted by the Packet Extractor block to determine the Flow-ID index. All packets including control packets trigger a lookup in this TCAM. Note that there is also 32 entries of per bit masks (flowid_tcam_mask). The lookup key consists of the following sub-fields.	Device 0x1F, Register 0x1ED0	Table 683, p. 410
FLOWID_TCAM_DATA1	TCAM Entry for Flow 1	Device 0x1F, Register 0x1EE0	Table 684, p. 411
FLOWID_TCAM_DATA2	TCAM Entry for Flow 2	Device 0x1F, Register 0x1EF0	Table 685, p. 412
FLOWID_TCAM_DATA3	TCAM Entry for Flow 3	Device 0x1F, Register 0x1F00	Table 686, p. 413
FLOWID_TCAM_MASK0	TCAM_MASK for Flow 0 Set mask bit to 1 to mask/exclude corresponding flowid_tcam_data bit from compare. For example, that bit will result in a match.	Device 0x1F, Register 0x1F50	Table 687, p. 414
FLOWID_TCAM_MASK1	TCAM_MASK for Flow 1	Device 0x1F, Register 0x1F60	Table 688, p. 415
FLOWID_TCAM_MASK2	TCAM_MASK for Flow 2	Device 0x1F, Register 0x1F70	Table 689, p. 416
FLOWID_TCAM_MASK3	TCAM_MASK for Flow 3	Device 0x1F, Register 0x1F80	Table 690, p. 417
MIB Statistic counters for the packets in the MACsec Ingress path (CSE_RX_MEM)			
IFINCTLOCTETS0	Total MSDU and MAC-DA/SA Octets permitted by the controlled port policies of SecY 0	Device 0x1F, Register 0x3300	Table 691, p. 418
IFINCTLOCTETS1	Total MSDU and MAC-DA/SA Octets permitted by the controlled port policies of SecY 1	Device 0x1F, Register 0x3304	Table 692, p. 418
IFINCTLOCTETS2	Total MSDU and MAC-DA/SA Octets permitted by the controlled port policies of SecY 2	Device 0x1F, Register 0x3308	Table 693, p. 418

Table 465: MACsec Summary Register Map (Continued)

Register Name	Register Description	Register Address	Table and Page
IFINCTLOCTETS3	Total MSDU and MAC-DA/SA Octets permitted by the controlled port policies of SecY 3	Device 0x1F, Register 0x330C	Table 694, p. 419
IFINCTLUCPKTS0	Unicast packets permitted by the controlled port policies of this SecY 0	Device 0x1F, Register 0x3310	Table 695, p. 419
IFINCTLUCPKTS1	Unicast packets permitted by the controlled port policies of this SecY 1	Device 0x1F, Register 0x3314	Table 696, p. 419
IFINCTLUCPKTS2	Unicast packets permitted by the controlled port policies of this SecY 2	Device 0x1F, Register 0x3318	Table 697, p. 419
IFINCTLUCPKTS3	Unicast packets permitted by the controlled port policies of this SecY 3	Device 0x1F, Register 0x331C	Table 698, p. 419
IFINCTLMCPKTS0	Multicast packets permitted by the controlled port policies of this SecY 0	Device 0x1F, Register 0x3320	Table 699, p. 420
IFINCTLMCPKTS1	Multicast packets permitted by the controlled port policies of this SecY 1	Device 0x1F, Register 0x3324	Table 700, p. 420
IFINCTLMCPKTS2	Multicast packets permitted by the controlled port policies of this SecY 2	Device 0x1F, Register 0x3328	Table 701, p. 420
IFINCTLMCPKTS3	Multicast packets permitted by the controlled port policies of this SecY 3	Device 0x1F, Register 0x332C	Table 702, p. 420
IFINCTLBCPKTS0	Broadcast packets permitted by the controlled port policies of this SecY 0	Device 0x1F, Register 0x3330	Table 703, p. 420
IFINCTLBCPKTS1	Broadcast packets permitted by the controlled port policies of this SecY 1	Device 0x1F, Register 0x3334	Table 704, p. 421
IFINCTLBCPKTS2	Broadcast packets permitted by the controlled port policies of this SecY 2	Device 0x1F, Register 0x3338	Table 705, p. 421
IFINCTLBCPKTS3	Broadcast packets permitted by the controlled port policies of this SecY 3	Device 0x1F, Register 0x333C	Table 706, p. 421
IFINUNCTLOCTETS0	Total MSDU and MAC-DA/SA Octets that are permitted by the uncontrolled port policies of SecY 0	Device 0x1F, Register 0x3340	Table 707, p. 421

Table 465: MACsec Summary Register Map (Continued)

Register Name	Register Description	Register Address	Table and Page
IFINUNCTLOCTETS1	Total MSDU and MAC-DA/SA Octets that are permitted by the uncontrolled port policies of SecY 1	Device 0x1F, Register 0x3344	Table 708, p. 421
IFINUNCTLOCTETS2	Total MSDU and MAC-DA/SA Octets that are permitted by the uncontrolled port policies of SecY 2	Device 0x1F, Register 0x3348	Table 709, p. 422
IFINUNCTLOCTETS3	Total MSDU and MAC-DA/SA Octets that are permitted by the uncontrolled port policies of SecY 3	Device 0x1F, Register 0x334C	Table 710, p. 422
IFINUNCTLUCPKTS0	Unicast packets permitted by the uncontrolled port policies of SecY 0	Device 0x1F, Register 0x3350	Table 711, p. 422
IFINUNCTLUCPKTS1	Unicast packets permitted by the uncontrolled port policies of SecY 1	Device 0x1F, Register 0x3354	Table 712, p. 422
IFINUNCTLUCPKTS2	Unicast packets permitted by the uncontrolled port policies of SecY 2	Device 0x1F, Register 0x3358	Table 713, p. 422
IFINUNCTLUCPKTS3	Unicast packets permitted by the uncontrolled port policies of SecY 3	Device 0x1F, Register 0x335C	Table 714, p. 423
IFINUNCTLMCPKTS0	Multicast packets permitted by the uncontrolled port policies of SecY 0	Device 0x1F, Register 0x3360	Table 715, p. 423
IFINUNCTLMCPKTS1	Multicast packets permitted by the uncontrolled port policies of SecY 1	Device 0x1F, Register 0x3364	Table 716, p. 423
IFINUNCTLMCPKTS2	Multicast packets permitted by the uncontrolled port policies of SecY 2	Device 0x1F, Register 0x3368	Table 717, p. 423
IFINUNCTLMCPKTS3	Multicast packets permitted by the uncontrolled port policies of SecY 3	Device 0x1F, Register 0x336C	Table 718, p. 423
IFINUNCTLBCPKTS0	Broadcast packets permitted by the uncontrolled port policies of SecY 0	Device 0x1F, Register 0x3370	Table 719, p. 424
IFINUNCTLBCPKTS1	Broadcast packets permitted by the uncontrolled port policies of SecY 1	Device 0x1F, Register 0x3374	Table 720, p. 424
IFINUNCTLBCPKTS2	Broadcast packets permitted by the uncontrolled port policies of SecY 2	Device 0x1F, Register 0x3378	Table 721, p. 424

Table 465: MACsec Summary Register Map (Continued)

Register Name	Register Description	Register Address	Table and Page
IFINUNCTLBCPKTS3	Broadcast packets permitted by the uncontrolled port policies of SecY 3	Device 0x1F, Register 0x337C	Table 722, p. 424
INPKTSCTRLPORTDISABLED0	The number of packets received which are dropped on disabled SecY 0	Device 0x1F, Register 0x3390	Table 727, p. 425
INPKTSCTRLPORTDISABLED1	The number of packets received which are dropped on disabled SecY 1	Device 0x1F, Register 0x3394	Table 728, p. 425
INPKTSCTRLPORTDISABLED2	The number of packets received which are dropped on disabled SecY 2	Device 0x1F, Register 0x3398	Table 729, p. 426
INPKTSCTRLPORTDISABLED3	The number of packets received which are dropped on disabled SecY 3	Device 0x1F, Register 0x339C	Table 730, p. 426
INPKTSSECYUNTAGGED0	The number of packets without a SecTag received while Validate_Frames in SecY 0 was not STRICT	Device 0x1F, Register 0x33A0	Table 731, p. 426
INPKTSSECYUNTAGGED1	The number of packets without a SecTag received while Validate_Frames in SecY 1 was not STRICT	Device 0x1F, Register 0x33A4	Table 732, p. 426
INPKTSSECYUNTAGGED2	The number of packets without a SecTag received while Validate_Frames in SecY 2 was not STRICT	Device 0x1F, Register 0x33A8	Table 733, p. 426
INPKTSSECYUNTAGGED3	The number of packets without a SecTag received while Validate_Frames in SecY 3 was not STRICT	Device 0x1F, Register 0x33AC	Table 734, p. 427
INPKTSSECYNOTAG0	The number of packets without a SecTag received while Validate_Frames in SecY 0 was STRICT	Device 0x1F, Register 0x33B0	Table 735, p. 427
INPKTSSECYNOTAG1	The number of packets without a SecTag received while Validate_Frames in SecY 1 was STRICT	Device 0x1F, Register 0x33B4	Table 736, p. 427
INPKTSSECYNOTAG2	The number of packets without a SecTag received while Validate_Frames in SecY 2 was STRICT	Device 0x1F, Register 0x33B8	Table 737, p. 427
INPKTSSECYNOTAG3	The number of packets without a SecTag received while Validate_Frames in SecY 3 was STRICT	Device 0x1F, Register 0x33BC	Table 738, p. 427

Table 465: MACsec Summary Register Map (Continued)

Register Name	Register Description	Register Address	Table and Page
INPKTSSECYBADTAG0	The number of received packets discarded with an invalid SecTag, zero value PN, or invalid ICV in SecY 0	Device 0x1F, Register 0x33C0	Table 739, p. 428
INPKTSSECYBADTAG1	The number of received packets discarded with an invalid SecTag, zero value PN, or invalid ICV in SecY 1	Device 0x1F, Register 0x33C4	Table 740, p. 428
INPKTSSECYBADTAG2	The number of received packets discarded with an invalid SecTag, zero value PN, or invalid ICV in SecY 2	Device 0x1F, Register 0x33C8	Table 741, p. 428
INPKTSSECYBADTAG3	The number of received packets discarded with an invalid SecTag, zero value PN, or invalid ICV in SecY 3	Device 0x1F, Register 0x33CC	Table 742, p. 428
INPKTSSECYNOSA0	The number of received packets with an unknown SA or an unused SA in SecY 0	Device 0x1F, Register 0x33D0	Table 743, p. 428
INPKTSSECYNOSA1	The number of received packets with an unknown SA or an unused SA in SecY 1	Device 0x1F, Register 0x33D4	Table 744, p. 429
INPKTSSECYNOSA2	The number of received packets with an unknown SA or an unused SA in SecY 2	Device 0x1F, Register 0x33D8	Table 745, p. 429
INPKTSSECYNOSA3	The number of received packets with an unknown SA or an unused SA in SecY 3	Device 0x1F, Register 0x33DC	Table 746, p. 429
INPKTSSECYNOSAERROR0	The number of received packets discarded because the received SCI is unknown or the SA is not in use in SecY 0	Device 0x1F, Register 0x33E0	Table 747, p. 429
INPKTSSECYNOSAERROR1	The number of received packets discarded because the received SCI is unknown or the SA is not in use in SecY 1	Device 0x1F, Register 0x33E4	Table 748, p. 429
INPKTSSECYNOSAERROR2	The number of received packets discarded because the received SCI is unknown or the SA is not in use in SecY 2	Device 0x1F, Register 0x33E8	Table 749, p. 430

Table 465: MACsec Summary Register Map (Continued)

Register Name	Register Description	Register Address	Table and Page
INPKTSSECYNOSAERROR3	The number of received packets discarded because the received SCI is unknown or the SA is not in use in SecY 3	Device 0x1F, Register 0x33EC	Table 750, p. 430
INOCTETSSECYVALIDATE0	The number of plaintext octets recovered from packets that were integrity protected but not encrypted in SecY 0	Device 0x1F, Register 0x33F0	Table 751, p. 430
INOCTETSSECYVALIDATE1	The number of plaintext octets recovered from packets that were integrity protected but not encrypted in SecY 1	Device 0x1F, Register 0x33F4	Table 752, p. 430
INOCTETSSECYVALIDATE2	The number of plaintext octets recovered from packets that were integrity protected but not encrypted in SecY 2	Device 0x1F, Register 0x33F8	Table 753, p. 430
INOCTETSSECYVALIDATE3	The number of plaintext octets recovered from packets that were integrity protected but not encrypted in SecY 3	Device 0x1F, Register 0x33FC	Table 754, p. 431
INOCTETSSECYDECRYPTED0	The number of plaintext octets recovered from packets that were integrity protected and encrypted in SecY 0	Device 0x1F, Register 0x3400	Table 755, p. 431
INOCTETSSECYDECRYPTED1	The number of plaintext octets recovered from packets that were integrity protected and encrypted in SecY 1	Device 0x1F, Register 0x3404	Table 756, p. 431
INOCTETSSECYDECRYPTED2	The number of plaintext octets recovered from packets that were integrity protected and encrypted in SecY 2	Device 0x1F, Register 0x3408	Table 757, p. 431
INOCTETSSECYDECRYPTED3	The number of plaintext octets recovered from packets that were integrity protected and encrypted in SecY 3	Device 0x1F, Register 0x340C	Table 758, p. 431
INPKTSSCLATE0	The number of packets discarded in SC0, because the received PN was lower than the lowest acceptable PN and with replay protect true.	Device 0x1F, Register 0x3420	Table 759, p. 432

Table 465: MACsec Summary Register Map (Continued)

Register Name	Register Description	Register Address	Table and Page
INPKTSSCLATE1	The number of packets discarded in SC1, because the received PN was lower than the lowest acceptable PN and with replay protect true.	Device 0x1F, Register 0x3424	Table 760, p. 432
INPKTSSCLATE2	The number of packets discarded in SC2, because the received PN was lower than the lowest acceptable PN and with replay protect true.	Device 0x1F, Register 0x3428	Table 761, p. 432
INPKTSSCLATE3	The number of packets discarded in SC3, because the received PN was lower than the lowest acceptable PN and with replay protect true.	Device 0x1F, Register 0x342C	Table 762, p. 432
INPKTSSCNOTVALID0	The number of packets discarded in SC0 because validation failed and Validate_Frames in SecY0 is 'STRICT' or the data was encrypted so the original frame could not be recovered.	Device 0x1F, Register 0x3430	Table 763, p. 432
INPKTSSCNOTVALID1	The number of packets discarded in SC1 because validation failed and Validate_Frames in SecY1 is 'STRICT' or the data was encrypted so the original frame could not be recovered.	Device 0x1F, Register 0x3434	Table 764, p. 433
INPKTSSCNOTVALID2	The number of packets discarded in SC2 because validation failed and Validate_Frames in SecY2 is 'STRICT' or the data was encrypted so the original frame could not be recovered.	Device 0x1F, Register 0x3438	Table 765, p. 433
INPKTSSCNOTVALID3	The number of packets discarded in SC3 because validation failed and Validate_Frames in SecY3 is 'STRICT' or the data was encrypted so the original frame could not be recovered.	Device 0x1F, Register 0x343C	Table 766, p. 433

Table 465: MACsec Summary Register Map (Continued)

Register Name	Register Description	Register Address	Table and Page
INPKTSSCINVALID0	The number of packets in SC0, that failed validation but could be received because Validate_Frames in SecY0 was 'CHECK' and the data was not encrypted so the original frame could be recovered.	Device 0x1F, Register 0x3440	Table 767, p. 433
INPKTSSCINVALID1	The number of packets in SC1, that failed validation but could be received because Validate_Frames in SecY1 was 'CHECK' and the data was not encrypted so the original frame could be recovered.	Device 0x1F, Register 0x3444	Table 768, p. 434
INPKTSSCINVALID2	The number of packets in SC2, that failed validation but could be received because Validate_Frames in SecY2 was 'CHECK' and the data was not encrypted so the original frame could be recovered.	Device 0x1F, Register 0x3448	Table 769, p. 434
INPKTSSCINVALID3	The number of packets in SC3, that failed validation but could be received because Validate_Frames in SecY3 was 'CHECK' and the data was not encrypted so the original frame could be recovered.	Device 0x1F, Register 0x344C	Table 770, p. 434
INPKTSSCDELAYED0	The number of received packets in SC0, with PN lower than the lowest acceptable PN and replay protect is false.	Device 0x1F, Register 0x3450	Table 771, p. 434
INPKTSSCDELAYED1	The number of received packets in SC1, with PN lower than the lowest acceptable PN and replay protect is false.	Device 0x1F, Register 0x3454	Table 772, p. 434
INPKTSSCDELAYED2	The number of received packets in SC2, with PN lower than the lowest acceptable PN and replay protect is false.	Device 0x1F, Register 0x3458	Table 773, p. 435
INPKTSSCDELAYED3	The number of received packets in SC3, with PN lower than the lowest acceptable PN and replay protect is false.	Device 0x1F, Register 0x345C	Table 774, p. 435

Table 465: MACsec Summary Register Map (Continued)

Register Name	Register Description	Register Address	Table and Page
INPKTSSCUNCHECKED0	The number of packets received in SC0, while Validate_Frames was disabled.	Device 0x1F, Register 0x3460	Table 775, p. 435
INPKTSSCUNCHECKED1	The number of packets received in SC1, while Validate_Frames was disabled.	Device 0x1F, Register 0x3464	Table 776, p. 435
INPKTSSCUNCHECKED2	The number of packets received in SC2, while Validate_Frames was disabled.	Device 0x1F, Register 0x3468	Table 777, p. 435
INPKTSSCUNCHECKED3	The number of packets received in SC3, while Validate_Frames was disabled.	Device 0x1F, Register 0x346C	Table 778, p. 436
INPKTSSCOK0	The number of packets received in SC0 successfully validated and within the replay window.	Device 0x1F, Register 0x3470	Table 779, p. 436
INPKTSSCOK1	The number of packets received in SC1 successfully validated and within the replay window.	Device 0x1F, Register 0x3474	Table 780, p. 436
INPKTSSCOK2	The number of packets received in SC2 successfully validated and within the replay window.	Device 0x1F, Register 0x3478	Table 781, p. 436
INPKTSSCOK3	The number of packets received in SC3 successfully validated and within the replay window.	Device 0x1F, Register 0x347C	Table 782, p. 436
INPKTSPARSEERR	The number of packets that have a parse error as indicated by PEX per port.	Device 0x1F, Register 0x3480	Table 783, p. 437
INPKTSFLOWIDTCAMMISS	The number of Flow ID TCAM misses per port.	Device 0x1F, Register 0x3484	Table 784, p. 437
INPKTSEARLYPREEMPTERR	The number of packets with Early Preemption violations detected per port.	Device 0x1F, Register 0x3488	Table 785, p. 437
INPKTSFLOWIDTCAMHIT0	The number of Packets which hit an entry in the Flow 0 TCAM. Only 1 counter increments per packet.	Device 0x1F, Register 0x348C	Table 786, p. 437
INPKTSFLOWIDTCAMHIT1	The number of Packets which hit an entry in the Flow 1 TCAM. Only 1 counter increments per packet.	Device 0x1F, Register 0x3490	Table 787, p. 437

Table 465: MACsec Summary Register Map (Continued)

Register Name	Register Description	Register Address	Table and Page
INPKTSFLOWIDTCAMHIT2	The number of Packets which hit an entry in the Flow 2 TCAM. Only 1 counter increments per packet.	Device 0x1F, Register 0x3494	Table 788, p. 438
INPKTSFLOWIDTCAMHIT3	The number of Packets which hit an entry in the Flow 3 TCAM. Only 1 counter increments per packet.	Device 0x1F, Register 0x3498	Table 789, p. 438
MIB Statistics counters for the packets in the MACsec Egress path (CSE_TX_MEM)			
IFOUTCTLOCTETS0	Total MSDU and MAC-DA/SA Octets that are permitted by the controlled port policies of SecY 0.	Device 0x1F, Register 0x34A0	Table 790, p. 438
IFOUTCTLOCTETS1	Total MSDU and MAC-DA/SA Octets that are permitted by the uncontrolled port policies of SecY 1	Device 0x1F, Register 0x34A4	Table 791, p. 438
IFOUTCTLOCTETS2	Total MSDU and MAC-DA/SA Octets that are permitted by the uncontrolled port policies of SecY 2	Device 0x1F, Register 0x34A8	Table 792, p. 438
IFOUTCTLOCTETS3	Total MSDU and MAC-DA/SA Octets that are permitted by the uncontrolled port policies of SecY 3	Device 0x1F, Register 0x34AC	Table 793, p. 439
IFOUTCTLUCPKTS0	Unicast packets permitted by the uncontrolled port policies of SecY 0	Device 0x1F, Register 0x34B0	Table 794, p. 439
IFOUTCTLUCPKTS1	Unicast packets permitted by the uncontrolled port policies of SecY 1	Device 0x1F, Register 0x34B4	Table 795, p. 439
IFOUTCTLUCPKTS2	Unicast packets permitted by the uncontrolled port policies of SecY 2	Device 0x1F, Register 0x34B8	Table 796, p. 439
IFOUTCTLUCPKTS3	Unicast packets permitted by the uncontrolled port policies of SecY 3	Device 0x1F, Register 0x34BC	Table 797, p. 439
IFOUTCTLMCPKTS0	Multicast packets permitted by the uncontrolled port policies of SecY 0	Device 0x1F, Register 0x34C0	Table 798, p. 440
IFOUTCTLMCPKTS1	Multicast packets permitted by the uncontrolled port policies of SecY 1	Device 0x1F, Register 0x34C4	Table 799, p. 440

Table 465: MACsec Summary Register Map (Continued)

Register Name	Register Description	Register Address	Table and Page
IFOUTCTLMCPKTS2	Multicast packets permitted by the uncontrolled port policies of SecY 2	Device 0x1F, Register 0x34C8	Table 800, p. 440
IFOUTCTLMCPKTS3	Multicast packets permitted by the uncontrolled port policies of SecY 3	Device 0x1F, Register 0x34CC	Table 801, p. 440
IFOUTCTLBCPKTS0	Broadcast packets permitted by the uncontrolled port policies of SecY 0	Device 0x1F, Register 0x34D0	Table 802, p. 440
IFOUTCTLBCPKTS1	Broadcast packets permitted by the uncontrolled port policies of SecY 1	Device 0x1F, Register 0x34D4	Table 803, p. 441
IFOUTCTLBCPKTS2	Broadcast packets permitted by the uncontrolled port policies of SecY 2	Device 0x1F, Register 0x34D8	Table 804, p. 441
IFOUTCTLBCPKTS3	Broadcast packets permitted by the uncontrolled port policies of SecY 3	Device 0x1F, Register 0x34DC	Table 805, p. 441
IFOUTUNCTLOCTETS0	Total MSDU and MAC-DA/SA Octets that are permitted by the uncontrolled port policies of SecY 0	Device 0x1F, Register 0x34E0	Table 806, p. 441
IFOUTUNCTLOCTETS1	Total MSDU and MAC-DA/SA Octets that are permitted by the uncontrolled port policies of SecY 1	Device 0x1F, Register 0x34E4	Table 807, p. 441
IFOUTUNCTLOCTETS2	Total MSDU and MAC-DA/SA Octets that are permitted by the uncontrolled port policies of SecY 2	Device 0x1F, Register 0x34E8	Table 808, p. 442
IFOUTUNCTLOCTETS3	Total MSDU and MAC-DA/SA Octets that are permitted by the uncontrolled port policies of SecY 3	Device 0x1F, Register 0x34EC	Table 809, p. 442
IFOUTUNCTLUCPKTS0	Unicast packets permitted by the uncontrolled port policies of SecY 0	Device 0x1F, Register 0x34F0	Table 810, p. 442
IFOUTUNCTLUCPKTS1	Unicast packets permitted by the uncontrolled port policies of SecY 1	Device 0x1F, Register 0x34F4	Table 811, p. 442
IFOUTUNCTLUCPKTS2	Unicast packets permitted by the uncontrolled port policies of SecY 2	Device 0x1F, Register 0x34F8	Table 812, p. 442

Table 465: MACsec Summary Register Map (Continued)

Register Name	Register Description	Register Address	Table and Page
IFOUTUNCTLUCPKTS3	Unicast packets permitted by the uncontrolled port policies of SecY 3	Device 0x1F, Register 0x34FC	Table 813, p. 443
IFOUTUNCTLMCPKTS0	Multicast packets permitted by the uncontrolled port policies of SecY 0	Device 0x1F, Register 0x3500	Table 814, p. 443
IFOUTUNCTLMCPKTS1	Multicast packets permitted by the uncontrolled port policies of SecY 1	Device 0x1F, Register 0x3504	Table 815, p. 443
IFOUTUNCTLMCPKTS2	Multicast packets permitted by the uncontrolled port policies of SecY 2	Device 0x1F, Register 0x3508	Table 816, p. 443
IFOUTUNCTLMCPKTS3	Multicast packets permitted by the uncontrolled port policies of SecY 3	Device 0x1F, Register 0x350C	Table 817, p. 443
IFOUTUNCTLBCPKTS0	Broadcast packets permitted by the uncontrolled port policies of SecY 0	Device 0x1F, Register 0x3510	Table 818, p. 444
IFOUTUNCTLBCPKTS1	Broadcast packets permitted by the uncontrolled port policies of SecY 1	Device 0x1F, Register 0x3514	Table 819, p. 444
IFOUTUNCTLBCPKTS2	Broadcast packets permitted by the uncontrolled port policies of SecY 2	Device 0x1F, Register 0x3518	Table 820, p. 444
IFOUTUNCTLBCPKTS3	Broadcast packets permitted by the uncontrolled port policies of SecY 3	Device 0x1F, Register 0x351C	Table 821, p. 444
OUTPKTSCTRLPORTDISABLED0	The number of packets received which are dropped on disabled SecY 0	Device 0x1F, Register 0x3520	Table 822, p. 444
OUTPKTSCTRLPORTDISABLED1	The number of packets received which are dropped on disabled SecY 1	Device 0x1F, Register 0x3524	Table 823, p. 445
OUTPKTSCTRLPORTDISABLED2	The number of packets received which are dropped on disabled SecY 2	Device 0x1F, Register 0x3528	Table 824, p. 445
OUTPKTSCTRLPORTDISABLED3	The number of packets received which are dropped on disabled SecY 3	Device 0x1F, Register 0x352C	Table 825, p. 445
OUTPKTSSECYUNTAGGED0	The number of packets without a SecTag received while Validate_Frames in SecY 0 was not STRICT.	Device 0x1F, Register 0x3530	Table 826, p. 445
OUTPKTSSECYUNTAGGED1	The number of packets without a SecTag received while Validate_Frames in SecY 1 was not STRICT.	Device 0x1F, Register 0x3534	Table 827, p. 445

Table 465: MACsec Summary Register Map (Continued)

Register Name	Register Description	Register Address	Table and Page
OUTPKTSSECYUNTAGGED2	The number of packets without a SecTag received while Validate_Frames in SecY 2 was not STRICT.	Device 0x1F, Register 0x3538	Table 828, p. 446
OUTPKTSSECYUNTAGGED3	The number of packets without a SecTag received while Validate_Frames in SecY 3 was not STRICT.	Device 0x1F, Register 0x353C	Table 829, p. 446
OUTPKTSSECYNOACTIVESA0	The number of data packets with SA value not matching any active SA value configured in SecY 0.	Device 0x1F, Register 0x3540	Table 830, p. 446
OUTPKTSSECYNOACTIVESA1	The number of data packets with SA value not matching any active SA value configured in SecY 1.	Device 0x1F, Register 0x3544	Table 831, p. 446
OUTPKTSSECYNOACTIVESA2	The number of data packets with SA value not matching any active SA value configured in SecY 2	Device 0x1F, Register 0x3548	Table 832, p. 446
OUTPKTSSECYNOACTIVESA3	The number of data packets with SA value not matching any active SA value configured in SecY 3.	Device 0x1F, Register 0x354C	Table 833, p. 447
OUTPKTSSECYTOOLONG0	The number of transmit packets discarded in SecY 0 because their length is greater than the configured MTU after SecTag/ICV insertion.	Device 0x1F, Register 0x3550	Table 834, p. 447
OUTPKTSSECYTOOLONG1	The number of transmit packets discarded in SecY 1 because their length is greater than the configured MTU after SecTag/ICV insertion.	Device 0x1F, Register 0x3554	Table 835, p. 447
OUTPKTSSECYTOOLONG2	The number of transmit packets discarded in SecY 2 because their length is greater than the configured MTU after SecTag/ICV insertion.	Device 0x1F, Register 0x3558	Table 836, p. 447
OUTPKTSSECYTOOLONG3	The number of transmit packets discarded in SecY 3 because their length is greater than the configured MTU after SecTag/ICV insertion.	Device 0x1F, Register 0x355C	Table 837, p. 447

Table 465: MACsec Summary Register Map (Continued)

Register Name	Register Description	Register Address	Table and Page
OUTOCTETSSECYPROTECTED0	The number of plain text octets in SecY 0 integrity protected but not encrypted in transmitted frames.	Device 0x1F, Register 0x3560	Table 838, p. 448
OUTOCTETSSECYPROTECTED1	The number of plain text octets in SecY 1 integrity protected but not encrypted in transmitted frames.	Device 0x1F, Register 0x3564	Table 839, p. 448
OUTOCTETSSECYPROTECTED2	The number of plain text octets in SecY 2 integrity protected but not encrypted in transmitted frames.	Device 0x1F, Register 0x3568	Table 840, p. 448
OUTOCTETSSECYPROTECTED3	The number of plain text octets in SecY 3 integrity protected but not encrypted in transmitted frames.	Device 0x1F, Register 0x356C	Table 841, p. 448
OUTOCTETSSECYENCRYPTED0	The number of plain text octets in SecY 0 integrity protected and encrypted in transmitted frames.	Device 0x1F, Register 0x3570	Table 842, p. 448
OUTOCTETSSECYENCRYPTED1	The number of plain text octets in SecY 1 integrity protected and encrypted in transmitted frames.	Device 0x1F, Register 0x3574	Table 843, p. 449
OUTOCTETSSECYENCRYPTED2	The number of plain text octets in SecY 2 integrity protected and encrypted in transmitted frames.	Device 0x1F, Register 0x3578	Table 844, p. 449
OUTOCTETSSECYENCRYPTED3	The number of plain text octets in SecY 3 integrity protected and encrypted in transmitted frames.	Device 0x1F, Register 0x357C	Table 845, p. 449
OUTPKTSSCPROTECTED0	The number of integrity protected but not encrypted packets transmitted SC 0	Device 0x1F, Register 0x3580	Table 846, p. 449
OUTPKTSSCPROTECTED1	The number of integrity protected but not encrypted packets transmitted SC 1	Device 0x1F, Register 0x3584	Table 847, p. 449
OUTPKTSSCPROTECTED2	The number of integrity protected but not encrypted packets transmitted SC 2	Device 0x1F, Register 0x3588	Table 848, p. 450
OUTPKTSSCPROTECTED3	The number of integrity protected but not encrypted packets transmitted SC 3	Device 0x1F, Register 0x358C	Table 849, p. 450
OUTPKTSSCENCRYPTED0	The number of integrity protected and encrypted packets transmitted in SC 0.	Device 0x1F, Register 0x3590	Table 850, p. 450

Table 465: MACsec Summary Register Map (Continued)

Register Name	Register Description	Register Address	Table and Page
OUTPKTSSCENCRYPTED1	The number of integrity protected and encrypted packets transmitted in SC 1.	Device 0x1F, Register 0x3594	Table 851, p. 450
OUTPKTSSCENCRYPTED2	The number of integrity protected and encrypted packets transmitted in SC 2.	Device 0x1F, Register 0x3598	Table 852, p. 450
OUTPKTSSCENCRYPTED3	The number of integrity protected and encrypted packets transmitted in SC 3.	Device 0x1F, Register 0x359C	Table 853, p. 451
OUTPKTSPARSEERR	The number of packets that have a parse error as indicated by PEX per port.	Device 0x1F, Register 0x35A0	Table 854, p. 451
OUTPKTSFLOWIDTCAMMISS	The number of Flow ID TCAM misses per port.	Device 0x1F, Register 0x35A4	Table 855, p. 451
OUTPKTSEARLYPREEMPTERR	The number of packets with Early Preemption violations detected per port.	Device 0x1F, Register 0x35A8	Table 856, p. 451
OUTPKTSFLOWIDTCAMHIT0	The number of Flow 0 TCAM hits per flow id entry.	Device 0x1F, Register 0x35AC	Table 857, p. 451
OUTPKTSFLOWIDTCAMHIT1	The number of Flow 1 TCAM hits per flow id entry.	Device 0x1F, Register 0x35B0	Table 858, p. 452
OUTPKTSFLOWIDTCAMHIT2	The number of Flow 2 TCAM hits per flow id entry.	Device 0x1F, Register 0x35B4	Table 859, p. 452
OUTPKTSFLOWIDTCAMHIT3	The number of Flow 3 TCAM hits per flow id entry.	Device 0x1F, Register 0x35B8	Table 860, p. 452
MPTP_CFG	Configuration during initialization	Device 0x1F, Register 0xA008	Table 861, p. 452
MPTP_RSTN	Reset during initialization	Device 0x1F, Register 0xA00A	Table 862, p. 453

Table 466: PORT_CONFIG_0
Device 0x1F, Register 0x0004

Bits	Field	Mode	HW Rst	SW Rst	Description
1:0	PARSE_DEPTH	R/W	0x1	0x1	Number of packet header bytes to parse, expressed in units of 16 bytes (for example, 1 means 16 bytes, 2 means 32 bytes, and so on) and counted from the first byte on SOP (which means that, if there is an 8B custom header, then the latter is part of the parse_depth). The value of zero specifies 64 bytes.

Table 467: CHANNEL_CONFIG_0
Device 0x1F, Register 0x0006

Bits	Field	Mode	HW Rst	SW Rst	Description
0	CH_BYPASS	R/W	0x1	0x1	Per channel bypass indication. When set, packets in the channel are not parsed and extracted.

Table 468: CHANNEL_CONFIG_1
Device 0x1F, Register 0x0008

Bits	Field	Mode	HW Rst	SW Rst	Description
0	CH_BYPASS	R/W	0x1	0x1	Per channel bypass indication. When set, packets in the channel are not parsed and extracted.

Table 469: DELAY_CFG_0
Device 0x1F, Register 0x0288

Bits	Field	Mode	HW Rst	SW Rst	Description
28	ENABLE_PREEMPT_FIXED_LATENCY	R/W	0x1	0x1	Express packets will always try to meet the fixed_latency setting. However Preempt packets can also be configured to try to meet the fixed_latency. Set this bit to 1 to have Preempt packets also have fixed latency.
17:0	FIXED_LATENCY	R/W	0x00000	0x00000	Fixed latency controls the latency that an express packet will undergo through the MACsec block. The latency is measured in clock cycles and is from SOP of the incoming packet to SOP of the corresponding outgoing packet. 0 - means that the fixed latency is disabled. Note that not all values of fixed latency will function. The following are the recommended values to use if fixed latency is desired. 1G (15.6 MHz) - set this field to 53. Note total latency through MACsec block will be 60 clock cycles (15.6 MHz). 1G (125 MHz) - set this field to 133. Note total latency through MACsec block will be 140 clock cycles (125 MHz). 100M (12.5 MHz) - set this field to 133. Note total latency through MACsec block will be 140 clock cycles (12.5 MHz).

Table 470: DELAY_CFG_0
Device 0x1F, Register 0x0308

Bits	Field	Mode	HW Rst	SW Rst	Description
28	ENABLE_PREEMPT_FIXED_LATENCY	R/W	0x1	0x1	Express packets will always try to meet the fixed_latency setting. However, Preempt packets can also be configured to try to meet the fixed_latency. Set this bit to 1 to have Preempt packets also have fixed latency.
17:0	FIXED_LATENCY	R/W	0x00000	0x00000	Fixed latency controls the latency that an express packet will undergo through the MACsec block. The latency is measured in clock cycles and is from SOP of the incoming packet to SOP of the corresponding outgoing packet. 0 - means that the fixed latency is disabled. Note that not all values of fixed latency will work. The following are the recommended values to use if fixed latency is desired. 1G (15.6 MHz) - set this field to 53. Note total latency through MACsec block will be 60 clock cycles (15.6 MHz). 1G (12 5MHz) - set this field to 133. Note total latency through MACsec block will be 140 clock cycles (125 MHz). 100M (12.5 MHz) - set this field to 133. Note total latency through MACsec block will be 140 clock cycles (12.5 MHz).

Table 471: PEX_CONFIGURATION
Device 0x1F, Register 0x0388

Bits	Field	Mode	HW Rst	SW Rst	Description
2	NON_DIX_ERR	R/W	0x0	0x0	Set to 1 to trigger a parse error when non-DIX frames are received
1	VLAN_AFTER_CUSTOM	R/W	0x0	0x0	Extract packets with VLAN tags located after custom tags
0	CUSTOM_HEADER	R/W	0x0	0x0	Per-port custom header enable. Port number packets are expected to have 8B custom header before DA/SA bit is set. This field only exists in RX slave and is RESERVED in TX slave.

Table 472: CUSTOM_TAG_0
Device 0x1F, Register 0x038A

Bits	Field	Mode	HW Rst	SW Rst	Description
24:22	CSTM_INDX	R/W	0x0	0x0	Custom tag index used to identify the VLAN etype when match is found (used to generate pex_cpm.outer_vlan_ type and pex_cpm.inner_vlan_type).
21	CSTM_BONUS	R/W	0x0	0x0	When set, extract the two bytes immediately following the tag label. If this bit is clear for all instances, then PEX will extract 2B after the first non-matching etype as bonus data.
20	CSTM_VLAN	R/W	0x0	0x0	Custom tag is VLAN tag.
19:16	CSTM_SIZE	R/W	0x0	0x0	Size of custom tag, including tag label. Valid values are 2,4,6,8,10,12,14,16. VLAN tag size must always be 4. For size 16, set field to zero.
15:0	CSTM_ETYPE	R/W	0x0000	0x0000	EthType/TPID; typical TPID for C-Tag is 0x8100, and S-Tag is 0x88a8.

Table 473: CUSTOM_TAG_1
Device 0x1F, Register 0x038C

Bits	Field	Mode	HW Rst	SW Rst	Description
24:22	CSTM_INDX	R/W	0x0	0x0	Custom tag index used to identify the VLAN etype when match is found (used to generate pex_cpm.outer_vlan_ type and pex_cpm.inner_vlan_type).
21	CSTM_BONUS	R/W	0x0	0x0	When set, extract the two bytes immediately following the tag label. If this bit is clear for all instances, then PEX will extract 2B after the first non-matching etype as bonus data.
20	CSTM_VLAN	R/W	0x0	0x0	Custom tag is VLAN tag.
19:16	CSTM_SIZE	R/W	0x0	0x0	Size of custom tag, including tag label. Valid values are 2,4,6,8,10,12,14,16. VLAN tag size must always be 4. For size 16, set field to zero.
15:0	CSTM_ETYPE	R/W	0x0000	0x0000	EthType/TPID; typical TPID for C-Tag is 0x8100, and S-Tag is 0x88a8.

Table 474: CUSTOM_TAG_2
Device 0x1F, Register 0x038E

Bits	Field	Mode	HW Rst	SW Rst	Description
24:22	CSTM_INDX	R/W	0x0	0x0	Custom tag index used to identify the VLAN etype when match is found (used to generate pex_cpm.outer_vlan_ type and pex_cpm.inner_vlan_type).

Table 474: CUSTOM_TAG_2
Device 0x1F, Register 0x038E

Bits	Field	Mode	HW Rst	SW Rst	Description
21	CSTM_BONUS	R/W	0x0	0x0	When set, extract the two bytes immediately following the tag label. If this bit is clear for all instances, then PEX will extract 2B after the first non-matching etype as bonus data.
20	CSTM_VLAN	R/W	0x0	0x0	Custom tag is VLAN tag.
19:16	CSTM_SIZE	R/W	0x0	0x0	Size of custom tag, including tag label. Valid values are 2,4,6,8,10,12,14,16. VLAN tag size must always be 4. For size 16, set field to zero.
15:0	CSTM_ETYPE	R/W	0x0000	0x0000	EthType/TPID; typical TPID for C-Tag is 0x8100 and S-Tag is 0x88a8.

Table 475: CUSTOM_TAG_3
Device 0x1F, Register 0x0390

Bits	Field	Mode	HW Rst	SW Rst	Description
24:22	CSTM_INDX	R/W	0x0	0x0	Custom tag index used to identify the VLAN etype when match is found (used to generate pex_cpm.outer_vlan_ type and pex_cpm.inner_vlan_type).
21	CSTM_BONUS	R/W	0x0	0x0	When set, extract the two bytes immediately following the tag label. If this bit is clear for all instances, then PEX will extract 2B after the first non-matching etype as bonus data.
20	CSTM_VLAN	R/W	0x0	0x0	Custom tag is VLAN tag.
19:16	CSTM_SIZE	R/W	0x0	0x0	Size of custom tag, including tag label. Valid values are 2,4,6,8,10,12,14,16. VLAN tag size must always be 4. For size 16, set field to zero.
15:0	CSTM_ETYPE	R/W	0x0000	0x0000	EthType/TPID; typical TPID for C-Tag is 0x8100, and S-Tag is 0x88a8.

Table 476: CUSTOM_TAG_4
Device 0x1F, Register 0x0392

Bits	Field	Mode	HW Rst	SW Rst	Description
24:22	CSTM_INDX	R/W	0x0	0x0	Custom tag index used to identify the VLAN etype when match is found (used to generate pex_cpm.outer_vlan_ type and pex_cpm.inner_vlan_type).
21	CSTM_BONUS	R/W	0x0	0x0	When set, extract the two bytes immediately following the tag label. If this bit is clear for all instances, then PEX will extract 2B after the first non-matching etype as bonus data.

Table 476: CUSTOM_TAG_4
Device 0x1F, Register 0x0392

Bits	Field	Mode	HW Rst	SW Rst	Description
20	CSTM_VLAN	R/W	0x0	0x0	Custom tag is VLAN tag.
19:16	CSTM_SIZE	R/W	0x0	0x0	Size of custom tag, including tag label. Valid values are 2,4,6,8,10,12,14,16. VLAN tag size must always be 4. For size 16, set field to zero.
15:0	CSTM_ETYPE	R/W	0x0000	0x0000	EthType/TPID; typical TPID for C-Tag is 0x8100, and S-Tag is 0x88a8.

Table 477: CUSTOM_TAG_5
Device 0x1F, Register 0x0394

Bits	Field	Mode	HW Rst	SW Rst	Description
24:22	CSTM_INDX	R/W	0x0	0x0	Custom tag index used to identify the VLAN etype when match is found (used to generate pex_cpm.outer_vlan_ type and pex_cpm.inner_vlan_type).
21	CSTM_BONUS	R/W	0x0	0x0	When set, extract the two bytes immediately following the tag label. If this bit is clear for all instances, then PEX will extract 2B after the first non-matching etype as bonus data.
20	CSTM_VLAN	R/W	0x0	0x0	Custom tag is VLAN tag.
19:16	CSTM_SIZE	R/W	0x0	0x0	Size of custom tag, including tag label. Valid values are 2,4,6,8,10,12,14,16. VLAN tag size must always be 4. For size 16, set field to zero.
15:0	CSTM_ETYPE	R/W	0x0000	0x0000	EthType/TPID; typical TPID for C-Tag is 0x8100, and S-Tag is 0x88a8.

Table 478: CUSTOM_TAG_6
Device 0x1F, Register 0x0396

Bits	Field	Mode	HW Rst	SW Rst	Description
24:22	CSTM_INDX	R/W	0x0	0x0	Custom tag index used to identify the VLAN etype when match is found (used to generate pex_cpm.outer_vlan_ type and pex_cpm.inner_vlan_type).
21	CSTM_BONUS	R/W	0x0	0x0	When set, extract the two bytes immediately following the tag label. If this bit is clear for all instances, then PEX will extract 2B after the first non-matching etype as bonus data.
20	CSTM_VLAN	R/W	0x0	0x0	Custom tag is VLAN tag.
19:16	CSTM_SIZE	R/W	0x0	0x0	Size of custom tag, including tag label. Valid values are 2,4,6,8,10,12,14,16. VLAN tag size must always be 4. For size 16, set field to zero.

Table 478: CUSTOM_TAG_6
Device 0x1F, Register 0x0396

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	CSTM_ETYPE	R/W	0x0000	0x0000	EthType/TPID; typical TPID for C-Tag is 0x8100, and S-Tag is 0x88a8.

Table 479: CUSTOM_TAG_7
Device 0x1F, Register 0x0398

Bits	Field	Mode	HW Rst	SW Rst	Description
24:22	CSTM_INDX	R/W	0x0	0x0	Custom tag index used to identify the VLAN etype when match is found (used to generate pex_cpm.outer_vlan_type and pex_cpm.inner_vlan_type).
21	CSTM_BONUS	R/W	0x0	0x0	When set, extract the two bytes immediately following the tag label. If this bit is clear for all instances, then PEX will extract 2B after the first non-matching etype as bonus data.
20	CSTM_VLAN	R/W	0x0	0x0	Custom tag is VLAN tag.
19:16	CSTM_SIZE	R/W	0x0	0x0	Size of custom tag, including tag label. Valid values are 2,4,6,8,10,12,14,16. VLAN tag size must always be 4. For size 16, set field to zero.
15:0	CSTM_ETYPE	R/W	0x0000	0x0000	EthType/TPID; typical TPID for C-Tag is 0x8100 and S-Tag is 0x88a8.

Table 480: MPLS_CFG_0
Device 0x1F, Register 0x039C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	MPLS_ETYPE	R/W	0x0000	0x0000	MPLS stack EthType

Table 481: MPLS_CFG_1
Device 0x1F, Register 0x039E

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	MPLS_ETYPE	R/W	0x0000	0x0000	MPLS stack EthType

Table 482: MPLS_CFG_2
Device 0x1F, Register 0x03A0

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	MPLS_ETYPE	R/W	0x0000	0x0000	MPLS stack EthType

Table 483: MPLS_CFG_3
Device 0x1F, Register 0x03A2

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	MPLS_ETYPE	R/W	0x0000	0x0000	MPLS stack EthType

Table 484: SECTAG_CFG
Device 0x1F, Register 0x03A4

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	SECTAG_ETYPE	R/W	0x0101	0x0101	SecTAG EthType

Table 485: RULE_ETYPE_CFG_0
Device 0x1F, Register 0x03A8

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RULE_ETYPE	R/W	0x0000	0x0000	EthType for control packet matching

Table 486: RULE_ETYPE_CFG_1
Device 0x1F, Register 0x03AA

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RULE_ETYPE	R/W	0x0000	0x0000	EthType for control packet matching

Table 487: RULE_ETYPE_CFG_2
Device 0x1F, Register 0x03AC

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RULE_ETYPE	R/W	0x0000	0x0000	EthType for control packet matching

Table 488: RULE_ETYPE_CFG_3
Device 0x1F, Register 0x03AE

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RULE_ETYPE	R/W	0x0000	0x0000	EthType for control packet matching

Table 489: RULE_ETYPE_CFG_4
Device 0x1F, Register 0x03B0

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RULE_ETYPE	R/W	0x0000	0x0000	EthType for control packet matching

Table 490: RULE_ETYPE_CFG_5
Device 0x1F, Register 0x03B2

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RULE_ETYPE	R/W	0x0000	0x0000	EthType for control packet matching

Table 491: RULE_ETYPE_CFG_6
Device 0x1F, Register 0x03B4

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RULE_ETYPE	R/W	0x0000	0x0000	EthType for control packet matching

Table 492: RULE_ETYPE_CFG_7
Device 0x1F, Register 0x03B6

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RULE_ETYPE	R/W	0x0000	0x0000	EthType for control packet matching

Table 493: RULE_DA_0
Device 0x1F, Register 0x03B8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_DA_MSB	R/W	0x0000	0x0000	MSB of DA address for control packet matching
31:0	RULE_DA_LSB	R/W	0x0	0x0	LSB of DA address for control packet matching

Table 494: RULE_DA_1
Device 0x1F, Register 0x03BC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_DA_MSB	R/W	0x0000	0x0000	MSB of DA address for control packet matching
31:0	RULE_DA_LSB	R/W	0x0	0x0	LSB of DA address for control packet matching

Table 495: RULE_DA_2
Device 0x1F, Register 0x03C0

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_DA_MSB	R/W	0x0000	0x0000	MSB of DA address for control packet matching
31:0	RULE_DA_LSB	R/W	0x0	0x0	LSB of DA address for control packet matching

Table 496: RULE_DA_3
Device 0x1F, Register 0x03C4

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_DA_MSB	R/W	0x0000	0x0000	MSB of DA address for control packet matching
31:0	RULE_DA_LSB	R/W	0x0	0x0	LSB of DA address for control packet matching

Table 497: RULE_DA_4
Device 0x1F, Register 0x03C8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_DA_MSB	R/W	0x0000	0x0000	MSB of DA address for control packet matching
31:0	RULE_DA_LSB	R/W	0x0	0x0	LSB of DA address for control packet matching

Table 498: RULE_DA_5
Device 0x1F, Register 0x03CC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_DA_MSB	R/W	0x0000	0x0000	MSB of DA address for control packet matching
31:0	RULE_DA_LSB	R/W	0x0	0x0	LSB of DA address for control packet matching

Table 499: RULE_DA_6
Device 0x1F, Register 0x03D0

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_DA_MSB	R/W	0x0000	0x0000	MSB of DA address for control packet matching
31:0	RULE_DA_LSB	R/W	0x0	0x0	LSB of DA address for control packet matching

Table 500: RULE_DA_7
Device 0x1F, Register 0x03D4

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_DA_MSB	R/W	0x0000	0x0000	MSB of DA address for control packet matching
31:0	RULE_DA_LSB	R/W	0x0	0x0	LSB of DA address for control packet matching

Table 501: RULE_DA_RANGE_MIN_0
Device 0x1F, Register 0x03D8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_RANGE_MIN_MSB	R/W	0x0000	0x0000	MSB of minimum DA address for DA range control packet matching
31:0	RULE_RANGE_MIN_LSB	R/W	0x0	0x0	LSB of minimum DA address for DA range control packet matching

Table 502: RULE_DA_RANGE_MAX_0
Device 0x1F, Register 0x03DC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_RANGE_MAX_MSB	R/W	0x0000	0x0000	MSB of maximum DA address for DA range control packet matching
31:0	RULE_RANGE_MAX_LSB	R/W	0x0	0x0	LSB of maximum DA address for DA range control packet matching

Table 503: RULE_DA_RANGE_MIN_1
Device 0x1F, Register 0x03E8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_RANGE_MIN_MSB	R/W	0x0000	0x0000	MSB of minimum DA address for DA range control packet matching

Table 503: RULE_DA_RANGE_MIN_1
Device 0x1F, Register 0x03E8

Bits	Field	Mode	HW Rst	SW Rst	Description
31:0	RULE_RANGE_MIN_LSB	R/W	0x0	0x0	LSB of minimum DA address for DA range control packet matching

Table 504: RULE_DA_RANGE_MAX_1
Device 0x1F, Register 0x03EC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_RANGE_MAX_MSB	R/W	0x0000	0x0000	MSB of maximum DA address for DA range control packet matching
31:0	RULE_RANGE_MAX_LSB	R/W	0x0	0x0	LSB of maximum DA address for DA range control packet matching

Table 505: RULE_DA_RANGE_MIN_2
Device 0x1F, Register 0x03F8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_RANGE_MIN_MSB	R/W	0x0000	0x0000	MSB of minimum DA address for DA range control packet matching
31:0	RULE_RANGE_MIN_LSB	R/W	0x0	0x0	LSB of minimum DA address for DA range control packet matching

Table 506: RULE_DA_RANGE_MAX_2
Device 0x1F, Register 0x03FC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_RANGE_MAX_MSB	R/W	0x0000	0x0000	MSB of maximum DA address for DA range control packet matching
31:0	RULE_RANGE_MAX_LSB	R/W	0x0	0x0	LSB of maximum DA address for DA range control packet matching

Table 507: RULE_DA_RANGE_MIN_3
Device 0x1F, Register 0x0408

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_RANGE_MIN_MSB	R/W	0x0000	0x0000	MSB of minimum DA address for DA range control packet matching

Table 507: RULE_DA_RANGE_MIN_3
Device 0x1F, Register 0x0408

Bits	Field	Mode	HW Rst	SW Rst	Description
31:0	RULE_RANGE_MIN_LSB	R/W	0x0	0x0	LSB of minimum DA address for DA range control packet matching

Table 508: RULE_DA_RANGE_MAX_3
Device 0x1F, Register 0x040C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_RANGE_MAX_MSB	R/W	0x0000	0x0000	MSB of maximum DA address for DA range control packet matching
31:0	RULE_RANGE_MAX_LSB	R/W	0x0	0x0	LSB of maximum DA address for DA range control packet matching

Table 509: RULE_COMBO_MIN_0
Device 0x1F, Register 0x0410

Bits	Field	Mode	HW Rst	SW Rst	Description
63:32	RULE_COMBO_MIN_MSB	R/W	0x0	0x0	MSB of minimum DA address for control packet matching
31:0	RULE_COMBO_MIN_LSB	R/W	0x0	0x0	LSB of minimum DA address for control packet matching

Table 510: RULE_COMBO_MAX_0
Device 0x1F, Register 0x0414

Bits	Field	Mode	HW Rst	SW Rst	Description
63:32	RULE_COMBO_MAX_MSB	R/W	0x0	0x0	MSB of minimum DA address for control packet matching
31:0	RULE_COMBO_MAX_LSB	R/W	0x0	0x0	LSB of maximum DA address for control packet matching

Table 511: RULE_COMBO_ET_0
Device 0x1F, Register 0x0418

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RULE_COMBO_ET	R/W	0x0000	0x0000	EthType for combo control packet matching

Table 512: RULE_COMBO_MIN_1
Device 0x1F, Register 0x0424

Bits	Field	Mode	HW Rst	SW Rst	Description
63:32	RULE_COMBO_MIN_MSB	R/W	0x0	0x0	MSB of minimum DA address for control packet matching
31:0	RULE_COMBO_MIN_LSB	R/W	0x0	0x0	LSB of minimum DA address for control packet matching

Table 513: RULE_COMBO_MAX_1
Device 0x1F, Register 0x0428

Bits	Field	Mode	HW Rst	SW Rst	Description
63:32	RULE_COMBO_MAX_MSB	R/W	0x0	0x0	MSB of minimum DA address for control packet matching
31:0	RULE_COMBO_MAX_LSB	R/W	0x0	0x0	LSB of maximum DA address for control packet matching

Table 514: RULE_COMBO_ET_1
Device 0x1F, Register 0x042C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RULE_COMBO_ET	R/W	0x0000	0x0000	EthType for combo control packet matching

Table 515: RULE_COMBO_MIN_2
Device 0x1F, Register 0x0438

Bits	Field	Mode	HW Rst	SW Rst	Description
63:32	RULE_COMBO_MIN_MSB	R/W	0x0	0x0	MSB of minimum DA address for control packet matching
31:0	RULE_COMBO_MIN_LSB	R/W	0x0	0x0	LSB of minimum DA address for control packet matching

Table 516: RULE_COMBO_MAX_2
Device 0x1F, Register 0x043C

Bits	Field	Mode	HW Rst	SW Rst	Description
63:32	RULE_COMBO_MAX_MSB	R/W	0x0	0x0	MSB of minimum DA address for control packet matching

Table 516: RULE_COMBO_MAX_2
Device 0x1F, Register 0x043C

Bits	Field	Mode	HW Rst	SW Rst	Description
31:0	RULE_COMBO_MAX_LSB	R/W	0x0	0x0	LSB of maximum DA address for control packet matching

Table 517: RULE_COMBO_ET_2
Device 0x1F, Register 0x0440

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RULE_COMBO_ET	R/W	0x0000	0x0000	EthType for combo control packet matching

Table 518: RULE_COMBO_MIN_3
Device 0x1F, Register 0x044C

Bits	Field	Mode	HW Rst	SW Rst	Description
63:32	RULE_COMBO_MIN_MSB	R/W	0x0	0x0	MSB of minimum DA address for control packet matching
31:0	RULE_COMBO_MIN_LSB	R/W	0x0	0x0	LSB of minimum DA address for control packet matching

Table 519: RULE_COMBO_MAX_3
Device 0x1F, Register 0x0450

Bits	Field	Mode	HW Rst	SW Rst	Description
63:32	RULE_COMBO_MAX_MSB	R/W	0x0	0x0	MSB of minimum DA address for control packet matching
31:0	RULE_COMBO_MAX_LSB	R/W	0x0	0x0	LSB of maximum DA address for control packet matching

Table 520: RULE_COMBO_ET_3
Device 0x1F, Register 0x0454

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RULE_COMBO_ET	R/W	0x0000	0x0000	EthType for combo control packet matching

Table 521: RULE_MAC
Device 0x1F, Register 0x0458

Bits	Field	Mode	HW Rst	SW Rst	Description
43:32	RULE_MAC_MSB	R/W	0x000	0x000	MSB of MAC address
31:0	RULE_MAC_LSB	R/W	0x0	0x0	LSB of MAC address

Table 522: RULE_ENABLE
Device 0x1F, Register 0x045C

Bits	Field	Mode	HW Rst	SW Rst	Description
24	RULE_MAC_EN	R/W	0x0	0x0	Enable MAC addresses for control packet matching
23:20	RULE_COMBO_EN	R/W	0x0	0x0	Enable combos for control packet matching
19:16	RULE_RANGE_EN	R/W	0x0	0x0	Enable DA range for control packet matching
15:8	RULE_AD_EN	R/W	0x00	0x00	Enable DAs for control packet matching
7:0	RULE_ETYP_EN	R/W	0x00	0x00	Enable EthTypes for control packet matching

Table 523: ETYPE_ENABLE
Device 0x1F, Register 0x045E

Bits	Field	Mode	HW Rst	SW Rst	Description
14	TXMCS_ETYPE_EN	R/W	0x0	0x0	Enable EthType stored in the field tx_mcs_header in the opt_header_cfg register. Set to 1 to enable the EthTypes, or 0 to disable.
13	RXMCS_ETYPE_EN	R/W	0x0	0x0	Enable EthType stored in the field rx_mcs_header in the opt_header_cfg register. Set to 1 to enable the EthType, or 0 to disable.
12	ST_ETYPE_EN	R/W	0x1	0x1	Enable EthType stored in the sectag_cfg registers. Set to 1 to enable the EthType, or 0 to disable.
11:8	MPLS_ETYPE_EN	R/W	0x0	0x0	Enable EthTypes stored in the 4 mpls_cfg registers, where bit 8-11 enable registers 0-3, respectively. Set to 1 to enable the EthTypes, or 0 to disable.
7:0	CSTM_ETYPE_EN	R/W	0x00	0x00	Enable EthTypes/TPID stored in the 8 custom_tag (including VLAN tags) registers, where bit 0-7 enable registers 0-7, respectively. Set to 1 to enable the EthTypes, or 0 to disable.

Table 524: PEX_CONFIGURATION
Device 0x1F, Register 0x0488

Bits	Field	Mode	HW Rst	SW Rst	Description
2	NON_DIX_ERR	R/W	0x0	0x0	Set to 1 to trigger a parse error when non-DIX frames are received
1	VLAN_AFTER_CUS-TOM	R/W	0x0	0x0	Extract packets with VLAN tags located after custom tags
0	CUSTOM_HEADER	R/W	0x0	0x0	Per-port custom header enable. Port number packets are expected to have8B custom header before DA/SA bit is set. This field only exists in RX slave and is RESERVED in TX slave.

Table 525: CUSTOM_TAG_0
Device 0x1F, Register 0x048A

Bits	Field	Mode	HW Rst	SW Rst	Description
24:22	CSTM_INDX	R/W	0x0	0x0	Custom tag index used to identify the VLAN etype when match is found (used to generate pex_cpm.outer_vlan_ type and pex_cpm.inner_vlan_type).
21	CSTM_BONUS	R/W	0x0	0x0	When set, extract the two bytes immediately following the tag label. If this bit is clear for all instances, then PEX will extract 2B after the first non-matching etype as bonus data.
20	CSTM_VLAN	R/W	0x0	0x0	Custom tag is VLAN tag.
19:16	CSTM_SIZE	R/W	0x0	0x0	Size of custom tag, including tag label. Valid values are 2,4,6,8,10,12,14,16. VLAN tag size must always be 4. For size 16, set field to zero.
15:0	CSTM_ETYPE	R/W	0x0000	0x0000	EthType/TPID; typical TPID for C-Tag is 0x8100, and S-Tag is 0x88a8.

Table 526: CUSTOM_TAG_1
Device 0x1F, Register 0x048C

Bits	Field	Mode	HW Rst	SW Rst	Description
24:22	CSTM_INDX	R/W	0x0	0x0	Custom tag index used to identify the VLAN etype when match is found (used to generate pex_cpm.outer_vlan_ type and pex_cpm.inner_vlan_type).
21	CSTM_BONUS	R/W	0x0	0x0	When set, extract the two bytes immediately following the tag label. If this bit is clear for all instances, then PEX will extract 2B after the first non-matching etype as bonus data.

Table 526: CUSTOM_TAG_1
Device 0x1F, Register 0x048C

Bits	Field	Mode	HW Rst	SW Rst	Description
20	CSTM_VLAN	R/W	0x0	0x0	Custom tag is VLAN tag.
19:16	CSTM_SIZE	R/W	0x0	0x0	Size of custom tag, including tag label. Valid values are 2,4,6,8,10,12,14,16. VLAN tag size must always be 4. For size 16, set field to zero.
15:0	CSTM_ETYPE	R/W	0x0000	0x0000	EthType/TPID; typical TPID for C-Tag is 0x8100, and S-Tag is 0x88a8.

Table 527: CUSTOM_TAG_2
Device 0x1F, Register 0x048E

Bits	Field	Mode	HW Rst	SW Rst	Description
24:22	CSTM_INDX	R/W	0x0	0x0	Custom tag index used to identify the VLAN etype when match is found (used to generate pex_cpm.outer_vlan_ type and pex_cpm.inner_vlan_type).
21	CSTM_BONUS	R/W	0x0	0x0	When set, extract the two bytes immediately following the tag label. If this bit is clear for all instances, then PEX will extract 2B after the first non-matching etype as bonus data.
20	CSTM_VLAN	R/W	0x0	0x0	Custom tag is VLAN tag.
19:16	CSTM_SIZE	R/W	0x0	0x0	Size of custom tag, including tag label. Valid values are 2,4,6,8,10,12,14,16. VLAN tag size must always be 4. For size 16, set field to zero.
15:0	CSTM_ETYPE	R/W	0x0000	0x0000	EthType/TPID; typical TPID for C-Tag is 0x8100, and S-Tag is 0x88a8.

Table 528: CUSTOM_TAG_3
Device 0x1F, Register 0x0490

Bits	Field	Mode	HW Rst	SW Rst	Description
24:22	CSTM_INDX	R/W	0x0	0x0	Custom tag index used to identify the VLAN etype when match is found (used to generate pex_cpm.outer_vlan_ type and pex_cpm.inner_vlan_type).
21	CSTM_BONUS	R/W	0x0	0x0	When set, extract the two bytes immediately following the tag label. If this bit is clear for all instances, then PEX will extract 2B after the first non-matching etype as bonus data.
20	CSTM_VLAN	R/W	0x0	0x0	Custom tag is VLAN tag.
19:16	CSTM_SIZE	R/W	0x0	0x0	Size of custom tag, including tag label. Valid values are 2,4,6,8,10,12,14,16. VLAN tag size must always be 4. For size 16, set field to zero.

Table 528: CUSTOM_TAG_3
Device 0x1F, Register 0x0490

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	CSTM_ETYPE	R/W	0x0000	0x0000	EthType/TPID; typical TPID for C-Tag is 0x8100, and S-Tag is 0x88a8.

Table 529: CUSTOM_TAG_4
Device 0x1F, Register 0x0492

Bits	Field	Mode	HW Rst	SW Rst	Description
24:22	CSTM_INDX	R/W	0x0	0x0	Custom tag index used to identify the VLAN etype when match is found (used to generate pex_cpm.outer_vlan_type and pex_cpm.inner_vlan_type).
21	CSTM_BONUS	R/W	0x0	0x0	When set, extract the two bytes immediately following the tag label. If this bit is clear for all instances, then PEX will extract 2B after the first non-matching etype as bonus data.
20	CSTM_VLAN	R/W	0x0	0x0	Custom tag is VLAN tag.
19:16	CSTM_SIZE	R/W	0x0	0x0	Size of custom tag, including tag label. Valid values are 2,4,6,8,10,12,14,16. VLAN tag size must always be 4. For size 16, set field to zero.
15:0	CSTM_ETYPE	R/W	0x0000	0x0000	EthType/TPID; typical TPID for C-Tag is 0x8100, and S-Tag is 0x88a8.

Table 530: CUSTOM_TAG_5
Device 0x1F, Register 0x0494

Bits	Field	Mode	HW Rst	SW Rst	Description
24:22	CSTM_INDX	R/W	0x0	0x0	Custom tag index used to identify the VLAN etype when match is found (used to generate pex_cpm.outer_vlan_type and pex_cpm.inner_vlan_type).
21	CSTM_BONUS	R/W	0x0	0x0	When set, extract the two bytes immediately following the tag label. If this bit is clear for all instances, then PEX will extract 2B after the first non-matching etype as bonus data.
20	CSTM_VLAN	R/W	0x0	0x0	Custom tag is VLAN tag.
19:16	CSTM_SIZE	R/W	0x0	0x0	Size of custom tag, including tag label. Valid values are 2,4,6,8,10,12,14,16. VLAN tag size must always be 4. For size 16, set field to zero.
15:0	CSTM_ETYPE	R/W	0x0000	0x0000	EthType/TPID; typical TPID for C-Tag is 0x8100, and S-Tag is 0x88a8.

Table 531: CUSTOM_TAG_6
Device 0x1F, Register 0x0496

Bits	Field	Mode	HW Rst	SW Rst	Description
24:22	CSTM_INDX	R/W	0x0	0x0	Custom tag index used to identify the VLAN etype when match is found (used to generate pex_cpm.outer_vlan_ type and pex_cpm.inner_vlan_type).
21	CSTM_BONUS	R/W	0x0	0x0	When set, extract the two bytes immediately following the tag label. If this bit is clear for all instances, then PEX will extract 2B after the first non-matching etype as bonus data.
20	CSTM_VLAN	R/W	0x0	0x0	Custom tag is VLAN tag.
19:16	CSTM_SIZE	R/W	0x0	0x0	Size of custom tag, including tag label. Valid values are 2,4,6,8,10,12,14,16. VLAN tag size must always be 4. For size 16, set field to zero.
15:0	CSTM_ETYPE	R/W	0x0000	0x0000	EthType/TPID; typical TPID for C-Tag is 0x8100, and S-Tag is 0x88a8.

Table 532: CUSTOM_TAG_7
Device 0x1F, Register 0x0498

Bits	Field	Mode	HW Rst	SW Rst	Description
24:22	CSTM_INDX	R/W	0x0	0x0	Custom tag index used to identify the VLAN etype when match is found (used to generate pex_cpm.outer_vlan_ type and pex_cpm.inner_vlan_type).
21	CSTM_BONUS	R/W	0x0	0x0	When set, extract the two bytes immediately following the tag label. If this bit is clear for all instances, then PEX will extract 2B after the first non-matching etype as bonus data.
20	CSTM_VLAN	R/W	0x0	0x0	Custom tag is VLAN tag.
19:16	CSTM_SIZE	R/W	0x0	0x0	Size of custom tag, including tag label. Valid values are 2,4,6,8,10,12,14,16. VLAN tag size must always be 4. For size 16, set field to zero.
15:0	CSTM_ETYPE	R/W	0x0000	0x0000	EthType/TPID; typical TPID for C-Tag is 0x8100, and S-Tag is 0x88a8.

Table 533: MPLS_CFG_0
Device 0x1F, Register 0x049C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	MPLS_ETYPE	R/W	0x0000	0x0000	MPLS stack EthType

Table 534: MPLS_CFG_1
Device 0x1F, Register 0x049E

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	MPLS_ETYPE	R/W	0x0000	0x0000	MPLS stack EthType

Table 535: MPLS_CFG_2
Device 0x1F, Register 0x04A0

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	MPLS_ETYPE	R/W	0x0000	0x0000	MPLS stack EthType

Table 536: MPLS_CFG_3
Device 0x1F, Register 0x04A2

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	MPLS_ETYPE	R/W	0x0000	0x0000	MPLS stack EthType

Table 537: SECTAG_CFG
Device 0x1F, Register 0x04A4

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	SECTAG_ETYPE	R/W	0x0101	0x0101	SecTAG EthType

Table 538: RULE_ETYPE_CFG_0
Device 0x1F, Register 0x04A8

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RULE_ETYPE	R/W	0x0000	0x0000	EthType for control packet matching

Table 539: RULE_ETYPE_CFG_1
Device 0x1F, Register 0x04AA

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RULE_ETYPE	R/W	0x0000	0x0000	EthType for control packet matching

Table 540: RULE_ETYPE_CFG_2
Device 0x1F, Register 0x04AC

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RULE_ETYPE	R/W	0x0000	0x0000	EthType for control packet matching

Table 541: RULE_ETYPE_CFG_3
Device 0x1F, Register 0x04AE

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RULE_ETYPE	R/W	0x0000	0x0000	EthType for control packet matching

Table 542: RULE_ETYPE_CFG_4
Device 0x1F, Register 0x04B0

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RULE_ETYPE	R/W	0x0000	0x0000	EthType for control packet matching

Table 543: RULE_ETYPE_CFG_5
Device 0x1F, Register 0x04B2

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RULE_ETYPE	R/W	0x0000	0x0000	EthType for control packet matching

Table 544: RULE_ETYPE_CFG_6
Device 0x1F, Register 0x04B4

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RULE_ETYPE	R/W	0x0000	0x0000	EthType for control packet matching

Table 545: RULE_ETYPE_CFG_7
Device 0x1F, Register 0x04B6

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RULE_ETYPE	R/W	0x0000	0x0000	EthType for control packet matching

Table 546: RULE_DA_0
Device 0x1F, Register 0x04B8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_DA_MSB	R/W	0x0000	0x0000	MSB of DA address for control packet matching
31:0	RULE_DA_LSB	R/W	0x0	0x0	LSB of DA address for control packet matching

Table 547: RULE_DA_1
Device 0x1F, Register 0x04BC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_DA_MSB	R/W	0x0000	0x0000	MSB of DA address for control packet matching
31:0	RULE_DA_LSB	R/W	0x0	0x0	LSB of DA address for control packet matching

Table 548: RULE_DA_2
Device 0x1F, Register 0x04C0

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_DA_MSB	R/W	0x0000	0x0000	MSB of DA address for control packet matching
31:0	RULE_DA_LSB	R/W	0x0	0x0	LSB of DA address for control packet matching

Table 549: RULE_DA_3
Device 0x1F, Register 0x04C4

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_DA_MSB	R/W	0x0000	0x0000	MSB of DA address for control packet matching
31:0	RULE_DA_LSB	R/W	0x0	0x0	LSB of DA address for control packet matching

Table 550: RULE_DA_4
Device 0x1F, Register 0x04C8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_DA_MSB	R/W	0x0000	0x0000	MSB of DA address for control packet matching
31:0	RULE_DA_LSB	R/W	0x0	0x0	LSB of DA address for control packet matching

Table 551: RULE_DA_5
Device 0x1F, Register 0x04CC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_DA_MSB	R/W	0x0000	0x0000	MSB of DA address for control packet matching
31:0	RULE_DA_LSB	R/W	0x0	0x0	LSB of DA address for control packet matching

Table 552: RULE_DA_6
Device 0x1F, Register 0x04D0

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_DA_MSB	R/W	0x0000	0x0000	MSB of DA address for control packet matching
31:0	RULE_DA_LSB	R/W	0x0	0x0	LSB of DA address for control packet matching

Table 553: RULE_DA_7
Device 0x1F, Register 0x04D4

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_DA_MSB	R/W	0x0000	0x0000	MSB of DA address for control packet matching
31:0	RULE_DA_LSB	R/W	0x0	0x0	LSB of DA address for control packet matching

Table 554: RULE_DA_RANGE_MIN_0
Device 0x1F, Register 0x04D8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_RANGE_MIN_MSB	R/W	0x0000	0x0000	MSB of minimum DA address for DA range control packet matching
31:0	RULE_RANGE_MIN_LSB	R/W	0x0	0x0	LSB of minimum DA address for DA range control packet matching

Table 555: RULE_DA_RANGE_MAX_0
Device 0x1F, Register 0x04DC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_RANGE_MAX_MSB	R/W	0x0000	0x0000	MSB of maximum DA address for DA range control packet matching
31:0	RULE_RANGE_MAX_LSB	R/W	0x0	0x0	LSB of maximum DA address for DA range control packet matching

Table 556: RULE_DA_RANGE_MIN_1
Device 0x1F, Register 0x04E8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_RANGE_MIN_MSB	R/W	0x0000	0x0000	MSB of minimum DA address for DA range control packet matching
31:0	RULE_RANGE_MIN_LSB	R/W	0x0	0x0	LSB of minimum DA address for DA range control packet matching

Table 557: RULE_DA_RANGE_MAX_1
Device 0x1F, Register 0x04EC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_RANGE_MAX_MSB	R/W	0x0000	0x0000	MSB of maximum DA address for DA range control packet matching
31:0	RULE_RANGE_MAX_LSB	R/W	0x0	0x0	LSB of maximum DA address for DA range control packet matching

Table 558: RULE_DA_RANGE_MIN_2
Device 0x1F, Register 0x04F8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_RANGE_MIN_MSB	R/W	0x0000	0x0000	MSB of minimum DA address for DA range control packet matching
31:0	RULE_RANGE_MIN_LSB	R/W	0x0	0x0	LSB of minimum DA address for DA range control packet matching

Table 559: RULE_DA_RANGE_MAX_2
Device 0x1F, Register 0x04FC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_RANGE_MAX_MSB	R/W	0x0000	0x0000	MSB of maximum DA address for DA range control packet matching
31:0	RULE_RANGE_MAX_LSB	R/W	0x0	0x0	LSB of maximum DA address for DA range control packet matching

Table 560: RULE_DA_RANGE_MIN_3
Device 0x1F, Register 0x0508

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_RANGE_MIN_MSB	R/W	0x0000	0x0000	MSB of minimum DA address for DA range control packet matching
31:0	RULE_RANGE_MIN_LSB	R/W	0x0	0x0	LSB of minimum DA address for DA range control packet matching

Table 561: RULE_DA_RANGE_MAX_3
Device 0x1F, Register 0x050C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:32	RULE_RANGE_MAX_MSB	R/W	0x0000	0x0000	MSB of maximum DA address for DA range control packet matching
31:0	RULE_RANGE_MAX_LSB	R/W	0x0	0x0	LSB of maximum DA address for DA range control packet matching

Table 562: RULE_COMBO_MIN_0
Device 0x1F, Register 0x0510

Bits	Field	Mode	HW Rst	SW Rst	Description
63:32	RULE_COMBO_MIN_MSB	R/W	0x0	0x0	MSB of minimum DA address for control packet matching
31:0	RULE_COMBO_MIN_LSB	R/W	0x0	0x0	LSB of minimum DA address for control packet matching

Table 563: RULE_COMBO_MAX_0
Device 0x1F, Register 0x0514

Bits	Field	Mode	HW Rst	SW Rst	Description
63:32	RULE_COMBO_MAX_MSB	R/W	0x0	0x0	MSB of minimum DA address for control packet matching
31:0	RULE_COMBO_MAX_LSB	R/W	0x0	0x0	LSB of maximum DA address for control packet matching

Table 564: RULE_COMBO_ET_0
Device 0x1F, Register 0x0518

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RULE_COMBO_ET	R/W	0x0000	0x0000	EthType for combo control packet matching

Table 565: RULE_COMBO_MIN_1
Device 0x1F, Register 0x0524

Bits	Field	Mode	HW Rst	SW Rst	Description
63:32	RULE_COMBO_MIN_MSB	R/W	0x0	0x0	MSB of minimum DA address for control packet matching
31:0	RULE_COMBO_MIN_LSB	R/W	0x0	0x0	LSB of minimum DA address for control packet matching

Table 566: RULE_COMBO_MAX_1
Device 0x1F, Register 0x0528

Bits	Field	Mode	HW Rst	SW Rst	Description
63:32	RULE_COMBO_MAX_MSB	R/W	0x0	0x0	MSB of minimum DA address for control packet matching
31:0	RULE_COMBO_MAX_LSB	R/W	0x0	0x0	LSB of maximum DA address for control packet matching

Table 567: RULE_COMBO_ET_1
Device 0x1F, Register 0x052C

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RULE_COMBO_ET	R/W	0x0000	0x0000	EthType for combo control packet matching

Table 568: RULE_COMBO_MIN_2
Device 0x1F, Register 0x0538

Bits	Field	Mode	HW Rst	SW Rst	Description
63:32	RULE_COMBO_MIN_MSB	R/W	0x0	0x0	MSB of minimum DA address for control packet matching
31:0	RULE_COMBO_MIN_LSB	R/W	0x0	0x0	LSB of minimum DA address for control packet matching

Table 569: RULE_COMBO_MAX_2
Device 0x1F, Register 0x053C

Bits	Field	Mode	HW Rst	SW Rst	Description
63:32	RULE_COMBO_MAX_MSB	R/W	0x0	0x0	MSB of minimum DA address for control packet matching
31:0	RULE_COMBO_MAX_LSB	R/W	0x0	0x0	LSB of maximum DA address for control packet matching

Table 570: RULE_COMBO_ET_2
Device 0x1F, Register 0x0540

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RULE_COMBO_ET	R/W	0x0000	0x0000	EthType for combo control packet matching

Table 571: RULE_COMBO_MIN_3
Device 0x1F, Register 0x054C

Bits	Field	Mode	HW Rst	SW Rst	Description
63:32	RULE_COMBO_MIN_MSB	R/W	0x0	0x0	MSB of minimum DA address for control packet matching
31:0	RULE_COMBO_MIN_LSB	R/W	0x0	0x0	LSB of minimum DA address for control packet matching

Table 572: RULE_COMBO_MAX_3
Device 0x1F, Register 0x0550

Bits	Field	Mode	HW Rst	SW Rst	Description
63:32	RULE_COMBO_MAX_MSB	R/W	0x0	0x0	MSB of minimum DA address for control packet matching
31:0	RULE_COMBO_MAX_LSB	R/W	0x0	0x0	LSB of maximum DA address for control packet matching

Table 573: RULE_COMBO_ET_3
Device 0x1F, Register 0x0554

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	RULE_COMBO_ET	R/W	0x0000	0x0000	EthType for combo control packet matching

Table 574: RULE_MAC
Device 0x1F, Register 0x0558

Bits	Field	Mode	HW Rst	SW Rst	Description
43:32	RULE_MAC_MSB	R/W	0x000	0x000	MSB of MAC address
31:0	RULE_MAC_LSB	R/W	0x0	0x0	LSB of MAC address

Table 575: RULE_ENABLE
Device 0x1F, Register 0x055C

Bits	Field	Mode	HW Rst	SW Rst	Description
24	RULE_MAC_EN	R/W	0x0	0x0	Enable MAC addresses for control packet matching.
23:20	RULE_COMBO_EN	R/W	0x0	0x0	Enable combos for control packet matching.
19:16	RULE_RANGE_EN	R/W	0x0	0x0	Enable DA range for control packet matching.
15:8	RULE_AD_EN	R/W	0x00	0x00	Enable DAs for control packet matching.
7:0	RULE_ETYP_EN	R/W	0x00	0x00	Enable EthTypes for control packet matching.

Table 576: ETYPE_ENABLE
Device 0x1F, Register 0x055E

Bits	Field	Mode	HW Rst	SW Rst	Description
14	TXMCS_ETYPE_EN	R/W	0x0	0x0	Enable EthType stored in the field tx_mcs_header in the opt_header_cfg register. Set to 1 to enable the EthTypes, or 0 to disable.
13	RXMCS_ETYPE_EN	R/W	0x0	0x0	Enable EthType stored in the field rx_mcs_header in the opt_header_cfg register. Set to 1 to enable the EthType, or 0 to disable.
12	ST_ETYPE_EN	R/W	0x1	0x1	Enable EthType stored in the sectag_cfg registers. Set to 1 to enable the EthType, or 0 to disable.
11:8	MPLS_ETYPE_EN	R/W	0x0	0x0	Enable EthTypes stored in the 4 mpls_cfg registers, where bit 8-11 enable registers 0-3 respectively. Set to 1 to enable the EthTypes, or 0 to disable.
7:0	CSTM_ETYPE_EN	R/W	0x00	0x00	Enable EthTypes/TPID stored in the 8 custom_tag (including VLAN tags) registers, where bit 0-7 enable registers 0-7 respectively. Set to 1 to enable the EthTypes, or 0 to disable.

Table 577: CTRL
Device 0x1F, Register 0x0588

Bits	Field	Mode	HW Rst	SW Rst	Description
0	CPU_CSE_CLR_ON_RD	R/W	0x0	0x0	When set to 1, counter memory will be cleared when it is read.

Table 578: CTRL
Device 0x1F, Register 0x05A0

Bits	Field	Mode	HW Rst	SW Rst	Description
0	CPU_CSE_CLR_ON_RD	R/W	0x0	0x0	When set to 1, counter memory will be cleared when it is read.

Table 579: RX_DEFAULT_SCI
Device 0x1F, Register 0x0624

Bits	Field	Mode	HW Rst	SW Rst	Description
63:32	RX_DEFAULT_SCI_MSB	R/W	0x1111 1111111 1111111 1111111 1111111	0x1111 1111111 1111111 1111111 1111111	Default SCI[63:32].
31:0	RX_DEFAULT_SCI_LSB	R/W	0x1111 1111111 1111111 1111111 1111111	0x1111 1111111 1111111 1111111 1111111	Default SCI[31:0].

Table 580: XPN_THRESHOLD
Device 0x1F, Register 0x0628

Bits	Field	Mode	HW Rst	SW Rst	Description
63:32	XPN_THRESH-OLD_MSB	R/W	0x1100 000000 000000 000000 0000	0x1100 000000 000000 000000 0000	32 MSB of the 64b xpn_threshold.
31:0	XPN_THRESH-OLD_LSB	R/W	0x0	0x0	32 LSB of the 64b xpn_threshold.

Table 581: PN_THRESHOLD
Device 0x1F, Register 0x062C

Bits	Field	Mode	HW Rst	SW Rst	Description
31:0	PN_THRESHOLD	R/W	0x1100 0000 0000 0000 0000 0000 0000	0x1100 0000 0000 0000 0000 0000 0000	32b pn_threshold

Table 582: SECY_MAP_MEM0
Device 0x1F, Register 0x063C

Bits	Field	Mode	HW Rst	SW Rst	Description
2	CTRL_PKT	R/W	0x0	0x0	Identifies all packets matching the associated Flow-ID lookup as control packets.
1:0	SECY	R/W	0x0	0x0	Identifies the SecY for this Flow.

Table 583: SECY_MAP_MEM1
Device 0x1F, Register 0x063D

Bits	Field	Mode	HW Rst	SW Rst	Description
2	CTRL_PKT	R/W	0x0	0x0	Identifies all packets matching the associated Flow-ID lookup as control packets.
1:0	SECY	R/W	0x0	0x0	Identifies the SecY for this Flow.

Table 584: SECY_MAP_MEM2
Device 0x1F, Register 0x063E

Bits	Field	Mode	HW Rst	SW Rst	Description
2	CTRL_PKT	R/W	0x0	0x0	Identifies all packets matching the associated Flow-ID lookup as control packets.
1:0	SECY	R/W	0x0	0x0	Identifies the SecY for this Flow.

Table 585: SECY_MAP_MEM3
Device 0x1F, Register 0x063F

Bits	Field	Mode	HW Rst	SW Rst	Description
2	CTRL_PKT	R/W	0x0	0x0	Identifies all packets matching the associated Flow-ID lookup as control packets.
1:0	SECY	R/W	0x0	0x0	Identifies the SecY for this Flow.

Table 586: SECY_PLCY_MEM0
Device 0x1F, Register 0x065C

Bits	Field	Mode	HW Rst	SW Rst	Description
63:32	REPLAY_WIN-DOW	R/W	0x0	0x0	Unsigned value indicating the size of the anti-replay window. The incoming packet PN must be greater than or equal to the associated next_pn (sa_pn_ table_mem) minus this value or the packet must be dropped.
30	REPLAY_PRO-TECT	R/W	0x0	0x0	Enables Anti-Replay protection
28	ICV_INCLUDES_ DA_SA	R/W	0x0	0x0	When set, the outer DA/SA bytes are included in the authentication GHASH calculation. Both standard MACsec and WAN based MACsec with VLAN tags in the clear require the DA+SA to be included in the authentication. WAN based MPLS MACsec would typically have the DA+SA excluded from authentica-tion since these fields can be modified by the NextHop lookup in MPLS routers.
26:20	CONFIDENTIALI-TY_OFFSET	R/W	0x0	0x0	Defines the number of bytes that are unencrypted following the SecTag.
15:12	CIPHER	R/W	0x0	0x0	Defines the cipher suite to use for this SecY This is an enum with the following supported options: 0 = GCM-AES-128 1 = GCM-AES-256 2 = GCM-AES-XPN-128 3 = GCM-AES-XPN-256
9:8	STRIP_SECTAG_ ICV	R/W	0x0	0x0	2'b00 = Strip both SecTag and ICV from packet 2'b01 = Reserved 2'b10 = Preserve SecTag, Strip ICV. 2'b11 = Preserve both SecTag and ICV.
5:4	VALIDATE_ FRAMES	R/W	0x0	0x0	Defines the permit policy for frames as defined in IEEE 802.1ae. Encoded as follows: 0 = DISABLED: Disable validation. 1 = CHECK: Enable validation, do not discard invalid frames. 2 = STRICT: Enable validation and discard invalid frames. 3 = NULL: No processing or accounting.
0	CONTROLLED_ PORT_ENABLED	R/W	0x0	0x0	Enable (or disable) operation of the Controlled port associated with this SecY. This can be used to dis-able the Controlled port and drop all data packets until the secure connectivity has been fully estab-lished.

Table 587: SECY_PLCY_MEM1
Device 0x1F, Register 0x0660

Bits	Field	Mode	HW Rst	SW Rst	Description
63:32	REPLAY_WIN-DOW	R/W	0x0	0x0	Unsigned value indicating the size of the anti-replay window. The incoming packet PN must be greater than or equal to the associated next_pn (sa_pn_ table_mem) minus this value or the packet must be dropped.
30	REPLAY_PRO-TECT	R/W	0x0	0x0	Enables Anti-Replay protection
28	ICV_INCLUDES_ DA_SA	R/W	0x0	0x0	When set, the outer DA/SA bytes are included in the authentication GHASH calculation. Both standard MACsec and WAN based MACsec with VLAN tags in the clear require the DA+SA to be included in the authentication. WAN based MPLS MACsec would typically have the DA+SA excluded from authentica-tion since these fields can be modified by the NextHop lookup in MPLS routers.
26:20	CONFIDENTIALI-TY_OFFSET	R/W	0x0	0x0	Defines the number of bytes that are unencrypted following the SecTag.
15:12	CIPHER	R/W	0x0	0x0	Defines the cipher suite to use for this SecY This is an enum with the following supported options: 0 = GCM-AES-128 1 = GCM-AES-256 2 = GCM-AES-XPN-128 3 = GCM-AES-XPN-256
9:8	STRIP_SECTAG_ ICV	R/W	0x0	0x0	2'b00 = Strip both SecTag and ICV from packet 2'b01 = Reserved. 2'b10 = Preserve SecTag, Strip ICV. 2'b11 = Preserve both SecTag and ICV.
5:4	VALIDATE_ FRAMES	R/W	0x0	0x0	Defines the permit policy for frames as defined in IEEE 802.1ae. Encoded as follows: 0 = DISABLED: Disable validation. 1 = CHECK: Enable validation, do not discard invalid frames. 2 = STRICT: Enable validation and discard invalid frames. 3 = NULL: No processing or accounting.
0	CONTROLLED_ PORT_ENABLED	R/W	0x0	0x0	Enable (or disable) operation of the Controlled port associated with this SecY. This can be used to dis-able the Controlled port and drop all data packets until the secure connectivity has been fully estab-lished.

Table 588: SECY_PLCY_MEM2
Device 0x1F, Register 0x0664

Bits	Field	Mode	HW Rst	SW Rst	Description
63:32	REPLAY_WIN-DOW	R/W	0x0	0x0	Unsigned value indicating the size of the anti-replay window. The incoming packet PN must be greater than or equal to the associated next_pn (sa_pn_ table_mem) minus this value or the packet must be dropped.
30	REPLAY_PRO-TECT	R/W	0x0	0x0	Enables Anti-Replay protection
28	ICV_INCLUDES_ DA_SA	R/W	0x0	0x0	When set, the outer DA/SA bytes are included in the authentication GHASH calculation. Both standard MACsec- and WAN-based MACsec with VLAN tags in the clear require the DA+SA to be included in the authentication. WAN-based MPLS MACsec would typically have the DA+SA excluded from authentica-tion since these fields can be modified by the NextHop lookup in MPLS routers.
26:20	CONFIDENTIALI-TY_OFFSET	R/W	0x0	0x0	Defines the number of bytes that are unencrypted following the SecTag.
15:12	CIPHER	R/W	0x0	0x0	Defines the cipher suite to use for this SecY. This is an enum with the following supported options: 0 = GCM-AES-128 1 = GCM-AES-256 2 = GCM-AES-XPN-128 3 = GCM-AES-XPN-256
9:8	STRIP_SECTAG_ ICV	R/W	0x0	0x0	2'b00 = Strip both SecTag and ICV from packet 2'b01 = Reserved. 2'b10 = Preserve SecTag, Strip ICV. 2'b11 = Preserve both SecTag and ICV.
5:4	VALIDATE_ FRAMES	R/W	0x0	0x0	Defines the permit policy for frames as defined in IEEE 802.1ae. Encoded as follows: 0 = DISABLED: Disable validation. 1 = CHECK: Enable validation, do not discard invalid frames. 2 = STRICT: Enable validation and discard invalid frames. 3 = NULL: No processing or accounting.
0	CONTROLLED_ PORT_ENABLED	R/W	0x0	0x0	Enable (or disable) operation of the Controlled port associated with this SecY. This can be used to dis-able the Controlled port and drop all data packets until the secure connectivity has been fully estab-lished.

Table 589: SECY_PLCY_MEM3
Device 0x1F, Register 0x0668

Bits	Field	Mode	HW Rst	SW Rst	Description
63:32	REPLAY_WIN-DOW	R/W	0x0	0x0	Unsigned value indicating the size of the anti-replay window. The incoming packet PN must be greater than or equal to the associated next_pn (sa_pn_ table_mem) minus this value or the packet must be dropped.
30	REPLAY_PRO-TECT	R/W	0x0	0x0	Enables Anti-Replay protection
28	ICV_INCLUDES_ DA_SA	R/W	0x0	0x0	When set, the outer DA/SA bytes are included in the authentication GHASH calculation. Both standard MACsec and WAN based MACsec with VLAN tags in the clear require the DA+SA to be included in the authentication. WAN based MPLS MACsec would typically have the DA+SA excluded from authentica-tion since these fields can be modified by the NextHop lookup in MPLS routers.
26:20	CONFIDENTIALI-TY_OFFSET	R/W	0x0	0x0	Defines the number of bytes that are unencrypted following the SecTag.
15:12	CIPHER	R/W	0x0	0x0	Defines the cipher suite to use for this SecY This is an enum with the following supported options: 0 = GCM-AES-128 1 = GCM-AES-256 2 = GCM-AES-XPN-128 3 = GCM-AES-XPN-256
9:8	STRIP_SECTAG_ ICV	R/W	0x0	0x0	2'b00 = Strip both SecTag and ICV from packet 2'b01 = Reserved. 2'b10 = Preserve SecTag, Strip ICV. 2'b11 = Preserve both SecTag and ICV.
5:4	VALIDATE_ FRAMES	R/W	0x0	0x0	Defines the permit policy for frames as defined in 802.1ae. Encoded as follows: 0 = DISABLED: Disable validation. 1 = CHECK: Enable validation, do not discard invalid frames. 2 = STRICT: Enable validation and discard invalid frames. 3 = NULL: No processing or accounting.
0	CONTROLLED_ PORT_ENABLED	R/W	0x0	0x0	Enable (or disable) operation of the Controlled port associated with this SecY. This can be used to dis-able the Controlled port and drop all data packets until the secure connectivity has been fully estab-lished.

Table 590: SA_MAP_MEM0
Device 0x1F, Register 0x067C

Bits	Field	Mode	HW Rst	SW Rst	Description
3	SA_IN_USE	R/W	0x0	0x0	Specifies whether this SA is in use. If a packet matches on an SA which is not in use, a policy violation is triggered and the packet is either permitted or denied based on the SecY Policy table.
2:0	SA_INDEX	R/W	0x0	0x0	Defines the SA to use for this packet

Table 591: SA_MAP_MEM1
Device 0x1F, Register 0x0680

Bits	Field	Mode	HW Rst	SW Rst	Description
3	SA_IN_USE	R/W	0x0	0x0	Specifies whether this SA is in use. If a packet matches on an SA which is not in use, a policy violation is triggered and the packet is either permitted or denied based on the SecY Policy table.
2:0	SA_INDEX	R/W	0x0	0x0	Defines the SA to use for this packet

Table 592: SA_MAP_MEM2
Device 0x1F, Register 0x0684

Bits	Field	Mode	HW Rst	SW Rst	Description
3	SA_IN_USE	R/W	0x0	0x0	Specifies whether this SA is in use or not. If a packet matches on an SA which is not in use, a policy violation is triggered and the packet is either permitted or denied based on the SecY Policy table.
2:0	SA_INDEX	R/W	0x0	0x0	Defines the SA to use for this packet

Table 593: SA_MAP_MEM3
Device 0x1F, Register 0x0688

Bits	Field	Mode	HW Rst	SW Rst	Description
3	SA_IN_USE	R/W	0x0	0x0	Specifies whether this SA is in use or not. If a packet matches on an SA which is not in use, a policy violation is triggered and the packet is either permitted or denied based on the SecY Policy table.
2:0	SA_INDEX	R/W	0x0	0x0	Defines the SA to use for this packet

Table 594: SA_MAP_MEM4
Device 0x1F, Register 0x068C

Bits	Field	Mode	HW Rst	SW Rst	Description
3	SA_IN_USE	R/W	0x0	0x0	Specifies whether this SA is in use or not. If a packet matches on an SA which is not in use, a policy violation is triggered and the packet is either permitted or denied based on the SecY Policy table.
2:0	SA_INDEX	R/W	0x0	0x0	Defines the SA to use for this packet

Table 595: SA_MAP_MEM5
Device 0x1F, Register 0x0690

Bits	Field	Mode	HW Rst	SW Rst	Description
3	SA_IN_USE	R/W	0x0	0x0	Specifies whether this SA is in use or not. If a packet matches on an SA which is not in use, a policy violation is triggered and the packet is either permitted or denied based on the SecY Policy table.
2:0	SA_INDEX	R/W	0x0	0x0	Defines the SA to use for this packet

Table 596: SA_MAP_MEM6
Device 0x1F, Register 0x0694

Bits	Field	Mode	HW Rst	SW Rst	Description
3	SA_IN_USE	R/W	0x0	0x0	Specifies whether this SA is in use or not. If a packet matches on an SA which is not in use, a policy violation is triggered and the packet is either permitted or denied based on the SecY Policy table.
2:0	SA_INDEX	R/W	0x0	0x0	Defines the SA to use for this packet

Table 597: SA_MAP_MEM7
Device 0x1F, Register 0x0698

Bits	Field	Mode	HW Rst	SW Rst	Description
3	SA_IN_USE	R/W	0x0	0x0	Specifies whether this SA is in use or not. If a packet matches on an SA which is not in use, a policy violation is triggered and the packet is either permitted or denied based on the SecY Policy table.
2:0	SA_INDEX	R/W	0x0	0x0	Defines the SA to use for this packet

Table 598: SA_MAP_MEM8
Device 0x1F, Register 0x069C

Bits	Field	Mode	HW Rst	SW Rst	Description
3	SA_IN_USE	R/W	0x0	0x0	Specifies whether this SA is in use or not. If a packet matches on an SA which is not in use, a policy violation is triggered and the packet is either permitted or denied based on the SecY Policy table.
2:0	SA_INDEX	R/W	0x0	0x0	Defines the SA to use for this packet

Table 599: SA_MAP_MEM9
Device 0x1F, Register 0x06A0

Bits	Field	Mode	HW Rst	SW Rst	Description
3	SA_IN_USE	R/W	0x0	0x0	Specifies whether this SA is in use or not. If a packet matches on an SA which is not in use, a policy violation is triggered and the packet is either permitted or denied based on the SecY Policy table.
2:0	SA_INDEX	R/W	0x0	0x0	Defines the SA to use for this packet

Table 600: SA_MAP_MEM10
Device 0x1F, Register 0x06A4

Bits	Field	Mode	HW Rst	SW Rst	Description
3	SA_IN_USE	R/W	0x0	0x0	Specifies whether this SA is in use or not. If a packet matches on an SA which is not in use, a policy violation is triggered and the packet is either permitted or denied based on the SecY Policy table.
2:0	SA_INDEX	R/W	0x0	0x0	Defines the SA to use for this packet

Table 601: SA_MAP_MEM11
Device 0x1F, Register 0x06A8

Bits	Field	Mode	HW Rst	SW Rst	Description
3	SA_IN_USE	R/W	0x0	0x0	Specifies whether this SA is in use or not. If a packet matches on an SA which is not in use, a policy violation is triggered and the packet is either permitted or denied based on the SecY Policy table.
2:0	SA_INDEX	R/W	0x0	0x0	Defines the SA to use for this packet

Table 602: SA_MAP_MEM12
Device 0x1F, Register 0x06AC

Bits	Field	Mode	HW Rst	SW Rst	Description
3	SA_IN_USE	R/W	0x0	0x0	Specifies whether this SA is in use or not. If a packet matches on an SA which is not in use, a policy violation is triggered and the packet is either permitted or denied based on the SecY Policy table.
2:0	SA_INDEX	R/W	0x0	0x0	Defines the SA to use for this packet

Table 603: SA_MAP_MEM13
Device 0x1F, Register 0x06B0

Bits	Field	Mode	HW Rst	SW Rst	Description
3	SA_IN_USE	R/W	0x0	0x0	Specifies whether this SA is in use or not. If a packet matches on an SA which is not in use, a policy violation is triggered and the packet is either permitted or denied based on the SecY Policy table.
2:0	SA_INDEX	R/W	0x0	0x0	Defines the SA to use for this packet

Table 604: SA_MAP_MEM14
Device 0x1F, Register 0x06B4

Bits	Field	Mode	HW Rst	SW Rst	Description
3	SA_IN_USE	R/W	0x0	0x0	Specifies whether this SA is in use or not. If a packet matches on an SA which is not in use, a policy violation is triggered and the packet is either permitted or denied based on the SecY Policy table.
2:0	SA_INDEX	R/W	0x0	0x0	Defines the SA to use for this packet

Table 605: SA_MAP_MEM15
Device 0x1F, Register 0x06B8

Bits	Field	Mode	HW Rst	SW Rst	Description
3	SA_IN_USE	R/W	0x0	0x0	Specifies whether this SA is in use or not. If a packet matches on an SA which is not in use, a policy violation is triggered and the packet is either permitted or denied based on the SecY Policy table.
2:0	SA_INDEX	R/W	0x0	0x0	Defines the SA to use for this packet

Table 606: SA_PLCY_MEM0
Device 0x1F, Register 0x0700

Bits	Field	Mode	HW Rst	SW Rst	Description
511:480	SSCI	R/W	0x0	0x0	32b SSCI value: Short Secure Channel Identifier, used in XPN ciphers.
479:384	SALT	R/W	0x0	0x0	96b Salt value: Salt value used in XPN ciphers.
383:256	HASHKEY	R/W	0x0	0x0	128b Hash Key: Key used for authentication. This is derived by performing a 128/256 bit AES-ECB block encryption of an all 0s block with the SAK;E(SAK, 128'h0). The cipher text result of this operation is the H Key software must configure in this entry.
255:0	SAK	R/W	0x0	0x0	256b SAK: Defines the encryption key to be used to decrypt this packet. The lower 128 bits are used for 128-bit ciphers.

Table 607: SA_PLCY_MEM1
Device 0x1F, Register 0x0720

Bits	Field	Mode	HW Rst	SW Rst	Description
511:480	SSCI	R/W	0x0	0x0	32b SSCI value: Short Secure Channel Identifier, used in XPN ciphers.
479:384	SALT	R/W	0x0	0x0	96b Salt value: Salt value used in XPN ciphers.
383:256	HASHKEY	R/W	0x0	0x0	128b Hash Key: Key used for authentication. This is derived by performing a 128/256 bit AES-ECB block encryption of an all 0s block with the SAK;E(SAK, 128'h0). The cipher text result of this operation is the H Key software needs to configure in this entry.
255:0	SAK	R/W	0x0	0x0	256b SAK: Defines the encryption key to be used to decrypt this packet. The lower 128 bits are used for 128-bit ciphers.

Table 608: SA_PLCY_MEM2
Device 0x1F, Register 0x0740

Bits	Field	Mode	HW Rst	SW Rst	Description
511:480	SSCI	R/W	0x0	0x0	32b SSCI value: Short Secure Channel Identifier, used in XPN ciphers.
479:384	SALT	R/W	0x0	0x0	96b Salt value: Salt value used in XPN ciphers.

Table 608: SA_PLCY_MEM2 (Continued)
Device 0x1F, Register 0x0740

Bits	Field	Mode	HW Rst	SW Rst	Description
383:256	HASHKEY	R/W	0x0	0x0	128b Hash Key: Key used for authentication. This is derived by performing a 128/256 bit AES-ECB block encryption of an all 0s block with the SAK;E(SAK, 128'h0). The cipher text result of this operation is the H Key software needs to configure in this entry.
255:0	SAK	R/W	0x0	0x0	256b SAK: Defines the encryption key to be used to decrypt this packet. The lower 128 bits are used for 128-bit ciphers.

Table 609: SA_PLCY_MEM3
Device 0x1F, Register 0x0760

Bits	Field	Mode	HW Rst	SW Rst	Description
511:480	SSCI	R/W	0x0	0x0	32b SSCI value: Short Secure Channel Identifier, used in XPN ciphers.
479:384	SALT	R/W	0x0	0x0	96b Salt value: Salt value used in XPN ciphers.
001f0760.383:256	HASHKEY	R/W	0x0	0x0	128b Hash Key: Key used for authentication. This is derived by performing a 128/256-bit AES-ECB block encryption of an all 0s block with the SAK;E(SAK, 128'h0). The cipher text result of this operation is the H Key software must configure in this entry.
001f0760.255:0	SAK	R/W	0x0	0x0	256b SAK: Defines the encryption key to be used to decrypt this packet. The lower 128 bits are used for 128-bit ciphers.

Table 610: SA_PLCY_MEM4
Device 0x1F, Register 0x0780

Bits	Field	Mode	HW Rst	SW Rst	Description
511:480	SSCI	R/W	0x0	0x0	32b SSCI value: Short Secure Channel Identifier, used in XPN ciphers.
479:384	SALT	R/W	0x0	0x0	96b Salt value: Salt value used in XPN ciphers.
383:256	HASHKEY	R/W	0x0	0x0	128b Hash Key: Key used for authentication. This is derived by performing a 128/256-bit AES-ECB block encryption of an all 0s block with the SAK;E(SAK, 128'h0). The cipher text result of this operation is the H Key software must configure in this entry.
255:0	SAK	R/W	0x0	0x0	256b SAK: Defines the encryption key to be used to decrypt this packet. The lower 128 bits are used for 128-bit ciphers.

Table 611: SA_PLCY_MEM5
Device 0x1F, Register 0x07A0

Bits	Field	Mode	HW Rst	SW Rst	Description
511:480	SSCI	R/W	0x0	0x0	32b SSCI value: Short Secure Channel Identifier, used in XPN ciphers.
479:384	SALT	R/W	0x0	0x0	96b Salt value: Salt value used in XPN ciphers.
383:256	HASHKEY	R/W	0x0	0x0	128b Hash Key: Key used for authentication. This is derived by performing a 128/256-bit AES-ECB block encryption of an all 0s block with the SAK;E(SAK, 128'h0). The cipher text result of this operation is the H Key software must configure in this entry.
255:0	SAK	R/W	0x0	0x0	256b SAK: Defines the encryption key to be used to decrypt this packet. The lower 128 bits are used for 128-bit ciphers.

Table 612: SA_PLCY_MEM6
Device 0x1F, Register 0x07C0

Bits	Field	Mode	HW Rst	SW Rst	Description
511:480	SSCI	R/W	0x0	0x0	32b SSCI value: Short Secure Channel Identifier, used in XPN ciphers.
479:384	SALT	R/W	0x0	0x0	96b Salt value: Salt value used in XPN ciphers.
383:256	HASHKEY	R/W	0x0	0x0	128b Hash Key: Key used for authentication. This is derived by performing a 128/256-bit AES-ECB block encryption of an all 0s block with the SAK;E(SAK, 128'h0). The cipher text result of this operation is the H Key software must configure in this entry.
255:0	SAK	R/W	0x0	0x0	256b SAK: Defines the encryption key to be used to decrypt this packet. The lower 128 bits are used for 128-bit ciphers.

Table 613: SA_PLCY_MEM7
Device 0x1F, Register 0x07E0

Bits	Field	Mode	HW Rst	SW Rst	Description
511:480	SSCI	R/W	0x0	0x0	32b SSCI value: Short Secure Channel Identifier, used in XPN ciphers.
479:384	SALT	R/W	0x0	0x0	96b Salt value: Salt value used in XPN ciphers.

Table 613: SA_PLCY_MEM7 (Continued)
Device 0x1F, Register 0x07E0

Bits	Field	Mode	HW Rst	SW Rst	Description
383:256	HASHKEY	R/W	0x0	0x0	128b Hash Key: Key used for authentication. This is derived by performing a 128/256-bit AES-ECB block encryption of an all 0s block with the SAK;E(SAK, 128'h0). The cipher text result of this operation is the H Key software must configure in this entry.
255:0	SAK	R/W	0x0	0x0	256b SAK: Defines the encryption key to be used to decrypt this packet. The lower 128 bits are used for 128-bit ciphers.

Table 614: SA_PN_TABLE_MEM0
Device 0x1F, Register 0x0900

Bits	Field	Mode	HW Rst	SW Rst	Description
63:0	NEXT_PN	R/W	0x0	0x0	64b next_pn value: Next packet number expected.

Table 615: SA_PN_TABLE_MEM1
Device 0x1F, Register 0x0904

Bits	Field	Mode	HW Rst	SW Rst	Description
63:0	NEXT_PN	R/W	0x0	0x0	64b next_pn value: Next packet number expected.

Table 616: SA_PN_TABLE_MEM2
Device 0x1F, Register 0x0908

Bits	Field	Mode	HW Rst	SW Rst	Description
001f0908.63:0	NEXT_PN	R/W	0x0	0x0	64b next_pn value: Next packet number expected.

Table 617: SA_PN_TABLE_MEM3
Device 0x1F, Register 0x090C

Bits	Field	Mode	HW Rst	SW Rst	Description
001f090c.63:0	NEXT_PN	R/W	0x0	0x0	64b next_pn value: Next packet number expected.

Table 618: SA_PN_TABLE_MEM4
Device 0x1F, Register 0x0910

Bits	Field	Mode	HW Rst	SW Rst	Description
001f0910.63:0	NEXT_PN	R/W	0x0	0x0	64b next_pn value: Next packet number expected.

Table 619: SA_PN_TABLE_MEM5
Device 0x1F, Register 0x0914

Bits	Field	Mode	HW Rst	SW Rst	Description
001f0914.63:0	NEXT_PN	R/W	0x0	0x0	64b next_pn value: Next packet number expected.

Table 620: SA_PN_TABLE_MEM6
Device 0x1F, Register 0x0918

Bits	Field	Mode	HW Rst	SW Rst	Description
001f0918.63:0	NEXT_PN	R/W	0x0	0x0	64b next_pn value: Next packet number expected.

Table 621: SA_PN_TABLE_MEM7
Device 0x1F, Register 0x091C

Bits	Field	Mode	HW Rst	SW Rst	Description
001f091c.63:0	NEXT_PN	R/W	0x0	0x0	64b next_pn value: Next packet number expected.

Table 622: RX_FLOWID_TCAM_ENABLE_0
Device 0x1F, Register 0x0940

Bits	Field	Mode	HW Rst	SW Rst	Description
001f.3:0	ENABLE	R/W	0x0	0x0	Set to 1 to enable the corresponding TCAM entry to be part of the TCAM search/compare.

Table 623: FLOWID_TCAM_DATA0
Device 0x1F, Register 0x0950

Bits	Field	Mode	HW Rst	SW Rst	Description
202	PORT	R/W	0x0	0x0	Port number, 0-3
001f0950.201	EXPRESS	R/W	0x0	0x0	Express packet.

Table 623: FLOWID_TCAM_DATA0 (Continued)
Device 0x1F, Register 0x0950

Bits	Field	Mode	HW Rst	SW Rst	Description
001f0950.200:194	NUM_TAGS	R/W	0x0	0x0	Number of VLAN tags, CUSTOM tags, or MPLS labels before the SecTAG, excluding the Rx/Tx-MCS header tags. Bit 0: No tags/labels before SecTAG Bit 1: 1 tag/label before SecTAG Bit 2: 2 tags/labels before SecTAG. . Bit 6: 6 or more tags/labels before SecTAG.
001f0950.193:191	INNER_VLAN_TYPE	R/W	0x0	0x0	Encoded value indicating which VLAN TPID value matched for the second outermost VLAN Tag.
001f0950.190:188	OUTER_VLAN_TYPE	R/W	0x0	0x0	Encoded value indicating which VLAN TPID value matched for the outermost VLAN Tag.
001f0950.187:184	PACKET_TYPE	R/W	0x0	0x0	Encoded Packet Type from the parser: 0: No VLAN or MPLS 1: Single VLAN 2: Dual VLAN 3: MPLS4: Single VLAN followed by MPLS 5: Dual VLAN followed by MPLS 6: Unsupported type (2 VLAN or 4 MPLS) 7-14: Reserved for future use 15: Invalid (any parsing error)
001f0950.183:176	TAG_MATCH_BITMAP	R/W	0x0	0x0	Maps 1 to 1 with the set of configurable Etype CSRs and set when the associated E-Type (or TPID) was found in the first 6 tags of the packet.
001f0950.175:160	BONUS_DATA	R/W	0x0	0x0	2 bytes of additional bonus data extracted from one of the custom tags.
001f0950.159:156	SECOND_OUTER_PRIORITY	R/W	0x0	0x0	2nd Outermost VLAN {PCP/P bits, DE/CFI} or {1'b0, EXP} for MPLS.
001f0950.155:136	SECOND_OUTER_TAG_ID	R/W	0x0	0x0	2nd Outermost VLAN ID {8'd0, VLAN_ID[11:0]} or 20-bit MPLS label.
001f0950.135:132	OUTER_PRIORITY	R/W	0x0	0x0	Outermost VLAN {PCP/P bits, DE/CFI} or {1'b0, EXP} for MPLS.
001f0950.131:112	OUTER_TAG_ID	R/W	0x0	0x0	Outermost VLAN ID {8'd0, VLAN_ID[11:0]}, or 20-bit MPLS label.
001f0950.111:96	ETHER_TYPE	R/W	0x0	0x0	First E-Type found in the packet that does not match one of the preconfigured Custom, VLAN, or MPLS values.

Table 623: FLOWID_TCAM_DATA0 (Continued)
Device 0x1F, Register 0x0950

Bits	Field	Mode	HW Rst	SW Rst	Description
001f095 0.95:48	MAC_SA	R/W	0x0	0x0	MAC SA field extracted from the packet
001f095 0.47:0	MAC_DA	R/W	0x0	0x0	MAC DA field extracted from the packet

Table 624: FLOWID_TCAM_DATA1
Device 0x1F, Register 0x0960

Bits	Field	Mode	HW Rst	SW Rst	Description
202	PORT	R/W	0x0	0x0	Port number, 0-3
201	EXPRESS	R/W	0x0	0x0	Express packet.
200:194	NUM_TAGS	R/W	0x0	0x0	Number of VLAN tags, CUSTOM tags, or MPLS labels before the SecTAG, excluding the Rx/Tx-MCS header tags. Bit 0: No tags/labels before SecTAG Bit 1: 1 tag/label before SecTAG Bit 2: 2 tags/labels before SecTAG ... Bit 6: 6 or more tags/labels before SecTAG.
193:191	INNER_VLAN_ TYPE	R/W	0x0	0x0	Encoded value indicating which VLAN TPID value matched for the second outermost VLAN Tag.
190:188	OUTER_VLAN_ TYPE	R/W	0x0	0x0	Encoded value indicating which VLAN TPID value matched for the outermost VLAN Tag.
187:184	PACKET_TYPE	R/W	0x0	0x0	Encoded Packet Type from the parser: 0: No VLAN or MPLS 1: Single VLAN 2: Dual VLAN 3: MPLS 4: Single VLAN followed by MPLS 5: Dual VLAN followed by MPLS 6: Unsupported type (2 VLAN or 4 MPLS) 7-14: Reserved for future use 15: Invalid (any parsing error)
183:176	TAG_MATCH_ BITMAP	R/W	0x0	0x0	Maps 1 to 1 with the set of configurable Etype CSRs and set when the associated E-Type (or TPID) was found in the first 6 tags of the packet.
175:160	BONUS_DATA	R/W	0x0	0x0	2 bytes of additional bonus data extracted from one of the custom tags.
159:156	SECOND_OUT- ER_PRIORITY	R/W	0x0	0x0	2nd Outermost VLAN {PCP/P bits, DE/CFI} or {1'b0, EXP} for MPLS.
155:136	SECOND_OUT- ER_TAG_ID	R/W	0x0	0x0	2nd Outermost VLAN ID {8'd0, VLAN_ID[11:0]} or 20-bit MPLS label.
135:132	OUTER_PRIOR- ITY	R/W	0x0	0x0	Outermost VLAN {PCP/P bits, DE/CFI} or {1'b0, EXP} for MPLS.

Table 624: FLOWID_TCAM_DATA1 (Continued)
Device 0x1F, Register 0x0960

Bits	Field	Mode	HW Rst	SW Rst	Description
131:112	OUTER_TAG_ID	R/W	0x0	0x0	Outermost VLAN ID {8'd0, VLAN_ID[11:0]} or 20-bit MPLS label.
111:96	ETHER_TYPE	R/W	0x0	0x0	First E-Type found in the packet that does not match one of the preconfigured Custom, VLAN, or MPLS values.
95:48	MAC_SA	R/W	0x0	0x0	MAC SA field extracted from the packet
47:0	MAC_DA	R/W	0x0	0x0	MAC DA field extracted from the packet

Table 625: FLOWID_TCAM_DATA2
Device 0x1F, Register 0x0970

Bits	Field	Mode	HW Rst	SW Rst	Description
202	PORT	R/W	0x0	0x0	Port number, 0-3
201	EXPRESS	R/W	0x0	0x0	Express packet.
200:194	NUM_TAGS	R/W	0x0	0x0	Number of VLAN tags, CUSTOM tags, or MPLS labels before the SecTAG, excluding the Rx/Tx-MCS header tags. Bit 0: no tags/labels before SecTAG Bit 1: 1 tag/label before SecTAG Bit 2: 2 tags/labels before SecTAG. .. Bit 6: 6 or more tags/labels before SecTAG.
193:191	INNER_VLAN_ TYPE	R/W	0x0	0x0	Encoded value indicating which VLAN TPID value matched for the second outermost VLAN Tag.
190:188	OUTER_VLAN_ TYPE	R/W	0x0	0x0	Encoded value indicating which VLAN TPID value matched for the outermost VLAN Tag.
187:184	PACKET_TYPE	R/W	0x0	0x0	Encoded Packet Type from the parser: 0: No VLAN or MPLS 1: Single VLAN 2: Dual VLAN 3: MPLS 4: Single VLAN followed by MPLS 5: Dual VLAN followed by MPLS 6: Unsupported type (2 VLAN or 4 MPLS) 7-14: Reserved for future use 15: Invalid (any parsing error)
183:176	TAG_MATCH_ BITMAP	R/W	0x0	0x0	Maps 1 to 1 with the set of configurable Etype CSRs and set when the associated E-Type (or TPID) was found in the first 6 tags of the packet.
175:160	BONUS_DATA	R/W	0x0	0x0	2 bytes of additional bonus data extracted from one of the custom tags.
159:156	SECOND_OUT- ER_PRIORITY	R/W	0x0	0x0	2nd Outermost VLAN {PCP/P bits, DE/CFI} or {1'b0, EXP} for MPLS.

Table 625: FLOWID_TCAM_DATA2 (Continued)
Device 0x1F, Register 0x0970

Bits	Field	Mode	HW Rst	SW Rst	Description
155:136	SECOND_OUTER_TAG_ID	R/W	0x0	0x0	2nd Outermost VLAN ID {8'd0, VLAN_ID[11:0]} or 20-bit MPLS label.
135:132	OUTER_PRIORITY	R/W	0x0	0x0	Outermost VLAN {PCP/P bits, DE/CFI} or {1'b0, EXP} for MPLS.
131:112	OUTER_TAG_ID	R/W	0x0	0x0	Outermost VLAN ID {8'd0, VLAN_ID[11:0]} or 20-bit MPLS label.
111:96	ETHER_TYPE	R/W	0x0	0x0	First E-Type found in the packet that does not match one of the preconfigured Custom, VLAN, or MPLS values.
95:48	MAC_SA	R/W	0x0	0x0	MAC SA field extracted from the packet
47:0	MAC_DA	R/W	0x0	0x0	MAC DA field extracted from the packet

Table 626: FLOWID_TCAM_DATA3
Device 0x1F, Register 0x0980

Bits	Field	Mode	HW Rst	SW Rst	Description
202	PORT	R/W	0x0	0x0	Port number, 0-3
201	EXPRESS	R/W	0x0	0x0	Express packet.
200:194	NUM_TAGS	R/W	0x0	0x0	Number of VLAN tags, CUSTOM tags, or MPLS labels before the SecTAG, excluding the Rx/Tx-MCS header tags. Bit 0: no tags/labels before SecTAG Bit 1: 1 tag/label before SecTAG Bit 2: 2 tags/labels before SecTAG ... Bit 6: 6 or more tags/labels before SecTAG.
193:191	INNER_VLAN_TYPE	R/W	0x0	0x0	Encoded value indicating which VLAN TPID value matched for the second outermost VLAN Tag.
190:188	OUTER_VLAN_TYPE	R/W	0x0	0x0	Encoded value indicating which VLAN TPID value matched for the outermost VLAN Tag.
187:184	PACKET_TYPE	R/W	0x0	0x0	Encoded Packet Type from the parser: 0: No VLAN or MPLS 1: Single VLAN 2: Dual VLAN 3: MPLS 4: Single VLAN followed by MPLS 5: Dual VLAN followed by MPLS 6: Unsupported type (2 VLAN or 4 MPLS) 7-14: Reserved for future use 15: Invalid (any parsing error)
183:176	TAG_MATCH_BITMAP	R/W	0x0	0x0	Maps 1 to 1 with the set of configurable Etype CSRs and set when the associated E-Type (or TPID) was found in the first 6 tags of the packet.

Table 626: FLOWID_TCAM_DATA3 (Continued)
Device 0x1F, Register 0x0980

Bits	Field	Mode	HW Rst	SW Rst	Description
175:160	BONUS_DATA	R/W	0x0	0x0	2 bytes of additional bonus data extracted from one of the custom tags.
159:156	SECOND_OUTER_PRIORITY	R/W	0x0	0x0	2nd Outermost VLAN {PCP/P bits, DE/CFI} or {1'b0, EXP} for MPLS.
155:136	SECOND_OUTER_TAG_ID	R/W	0x0	0x0	2nd Outermost VLAN ID {8'd0, VLAN_ID[11:0]}, or 20-bit MPLS label.
135:132	OUTER_PRIORITY	R/W	0x0	0x0	Outermost VLAN {PCP/P bits, DE/CFI} or {1'b0, EXP} for MPLS.
131:112	OUTER_TAG_ID	R/W	0x0	0x0	Outermost VLAN ID {8'd0, VLAN_ID[11:0]}, or 20-bit MPLS label.
111:96	ETHER_TYPE	R/W	0x0	0x0	First E-Type found in the packet that does not match one of the preconfigured Custom, VLAN, or MPLS values.
95:48	MAC_SA	R/W	0x0	0x0	MAC SA field extracted from the packet
47:0	MAC_DA	R/W	0x0	0x0	MAC DA field extracted from the packet

Table 627: FLOWID_TCAM_MASK0
Device 0x1F, Register 0x090D

Bits	Field	Mode	HW Rst	SW Rst	Description
202	MASK_PORT	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
201	MASK_EXPRESS	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
200:194	MASK_NUM_TAGS	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
193:191	MASK_INNER_VLAN_TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
190:188	MASK_OUTER_VLAN_TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
187:184	MASK_PACKET_TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
183:176	MASK_TAG_MATCH_BITMAP	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
175:160	MASK_BONUS_DATA	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
159:156	MASK_SECOND_OUTER_PRIORITY	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
155:136	MASK_SECOND_OUTER_TAG_ID	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.

Table 627: FLOWID_TCAM_MASK0 (Continued)
Device 0x1F, Register 0x090D

Bits	Field	Mode	HW Rst	SW Rst	Description
135:132	MASK_OUTER_PRIORITY	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
131:112	MASK_OUTER_TAG_ID	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
111:96	MASK_ETHER_TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
95:48	MASK_MAC_SA	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
47:0	MASK_MAC_DA	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.

Table 628: FLOWID_TCAM_MASK1
Device 0x1F, Register 0x09E0

Bits	Field	Mode	HW Rst	SW Rst	Description
202	MASK_PORT	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
201	MASK_EXPRESS	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
200:194	MASK_NUM_TAGS	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
193:191	MASK_INNER_VLAN_TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
190:188	MASK_OUTER_VLAN_TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
187:184	MASK_PACKET_TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
183:176	MASK_TAG_MATCH_BITMAP	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
175:160	MASK_BONUS_DATA	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
159:156	MASK_SECOND_OUTER_PRIOR-ITY	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
155:136	MASK_SECOND_OUTER_TAG_ID	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
135:132	MASK_OUTER_PRIORITY	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
131:112	MASK_OUTER_TAG_ID	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
111:96	MASK_ETHER_TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.

Table 628: FLOWID_TCAM_MASK1 (Continued)
Device 0x1F, Register 0x09E0

Bits	Field	Mode	HW Rst	SW Rst	Description
95:48	MASK_MAC_SA	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
47:0	MASK_MAC_DA	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.

Table 629: FLOWID_TCAM_MASK2
Device 0x1F, Register 0x09F0

Bits	Field	Mode	HW Rst	SW Rst	Description
202	MASK_PORT	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
201	MASK_EXPRESS	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
200:194	MASK_NUM_ TAGS	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
193:191	MASK_INNER_ VLAN_TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
190:188	MASK_OUTER_ VLAN_TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
187:184	MASK_PACKET_ TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
183:176	MASK_TAG_ MATCH_BITMAP	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
175:160	MASK_BONUS_ DATA	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
159:156	MASK_SECOND_ OUTER_PRIOR- ITY	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
155:136	MASK_SECOND_ OUTER_TAG_ID	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
135:132	MASK_OUTER_ PRIORITY	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
131:112	MASK_OUTER_ TAG_ID	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
111:96	MASK_ETHER_ TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
95:48	MASK_MAC_SA	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
47:0	MASK_MAC_DA	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.

Table 630: FLOWID_TCAM_MASK3
Device 0x1F, Register 0x0A00

Bits	Field	Mode	HW Rst	SW Rst	Description
202	MASK_PORT	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
201	MASK_EXPRESS	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
200:194	MASK_NUM_ TAGS	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
193:191	MASK_INNER_ VLAN_TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
190:188	MASK_OUTER_ VLAN_TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude flowid_tcam_data bit from compare.
187:184	MASK_PACKET_ TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.corresponding
183:176	MASK_TAG_ MATCH_BITMAP	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
175:160	MASK_BONUS_ DATA	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
159:156	MASK_SECOND_ OUTER_PRIOR- ITY	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
155:136	MASK_SECOND_ OUTER_TAG_ID	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
135:132	MASK_OUTER_ PRIORITY	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
131:112	MASK_OUTER_ TAG_ID	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
111:96	MASK_ETHER_ TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
95:48	MASK_MAC_SA	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.
47:0	MASK_MAC_DA	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_ tcam_data bit from compare.

Table 631: SC_CAM_ENABLE_0
Device 0x1F, Register 0x0A50

Bits	Field	Mode	HW Rst	SW Rst	Description
3:0	ENABLE	R/W	0x0	0x0	Set to 1 to enable the corresponding CAM entry to be part of the CAM search/compare.

Table 632: SC_CAM0
Device 0x1F, Register 0x0x0A58

Bits	Field	Mode	HW Rst	SW Rst	Description
65:64	SECY	R/W	0x0	0x0	SecY associated with this packet.
63:0	SCI	R/W	0x0	0x0	The Secure Channel Identifier associated with this packet.

Table 633: SC_CAM1
Device 0x1F, Register 0x0A60

Bits	Field	Mode	HW Rst	SW Rst	Description
65:64	SECY	R/W	0x0	0x0	SecY associated with this packet.
63:0	SCI	R/W	0x0	0x0	The Secure Channel Identifier associated with this packet.

Table 634: SC_CAM2
Device 0x1F, Register 0x0A68

Bits	Field	Mode	HW Rst	SW Rst	Description
65:64	SECY	R/W	0x0	0x0	SecY associated with this packet.
63:0	SCI	R/W	0x0	0x0	The Secure Channel Identifier associated with this packet.

Table 635: SC_CAM3
Device 0x1F, Register 0x0A70

Bits	Field	Mode	HW Rst	SW Rst	Description
65:64	SECY	R/W	0x0	0x0	SecY associated with this packet.
63:0	SCI	R/W	0x0	0x0	The Secure Channel Identifier associated with this packet.

Table 636: AUTO_REKEY_ENABLE_0
Device 0x1F, Register 0x1998

Bits	Field	Mode	HW Rst	SW Rst	Description
3:0	AUTO_REKEY_ENABLE	R/W	0x0	0x0	Per SC auto rekey enable. 1b1 means enabled.

Table 637: TX_PORT_CFG_0
Device 0x1F, Register 0x199A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:0	SECTAG_ETYPE	R/W	0x0101	0x0101	MACsec SecTag ETYPE for insertion on corresponding port.

Table 638: XPN_THRESHOLD
Device 0x1F, Register 0x199C

Bits	Field	Mode	HW Rst	SW Rst	Description
63:32	XPN_THRESHOLD_MSB	R/W	0x0	0x0	32 MSB of the 64b xpn_threshold.
31:0	XPN_THRESHOLD_LSB	R/W	0x0	0x0	32 LSB of the 64b xpn_threshold.

Table 639: PN_THRESHOLD
Device 0x1F, Register 0x19A0

Bits	Field	Mode	HW Rst	SW Rst	Description
31:0	PN_THRESHOLD	R/W	0x0	0x0	32b pn_threshold.

Table 640: SA_KEY_LOCKOUT_0
Device 0x1F, Register 0x19A4

Bits	Field	Mode	HW Rst	SW Rst	Description
7:0	SA	R/W	0x00	0x00	SAK/Hash Key Lockout: When set, makes the corresponding SA Policy memory entries SAK/Hash Key values unreadable by SW. ASW read to that SAK/Hash Key entry will return 0s. Only after the SAK/Hash Key is written while this corresponding bit is low, will the entry's SAK/Hash Key that was written, become readable for as long as the corresponding lockout bit remains low. This ensures that the SAK/Hash Key inits entirety remain confidential once the lockout bit is set. As soon as the lockout bit goes high for an entry, all slices of the SAK/Hash Key will return 0s on SW read. Note that unlocking one entry has no impact on any other entry.

Table 641: FIXED_OFFSET_ADJUST
Device 0x1F, Register 0x19A8

Bits	Field	Mode	HW Rst	SW Rst	Description
4:0	FIXED_OFFSET_ADJUST	R/W	0x00	0x00	SecTag Fixed Offset Mode adjustment to compensate for Tx-MCS header size.

Table 642: SECY_MAP_MEM0
Device 0x1F, Register 0x19B0

Bits	Field	Mode	HW Rst	SW Rst	Description
69	AUXILIARY_PLCY	R/W	0x0	0x0	Auxiliary policy bits. MCS outputs the auxiliary bits to downstream for external functions such as Non-Disruptive Loopback (NDL).
68:67	SC	R/W	0x0	0x0	Identifies the SC for this Flow.
66	CTRL_PKT	R/W	0x0	0x0	Identifies all packets matching the associated Flow-ID lookup as control packets.
65:64	SECY	R/W	0x0	0x0	Identifies the SecY for this Flow.
63:0	SECTAG_SCI	R/W	0x00000	0x00000	Identifies the SecTAG SCI for this Flow.

Table 643: SECY_MAP_MEM1
Device 0x1F, Register 0x19B8

Bits	Field	Mode	HW Rst	SW Rst	Description
69	AUXILIARY_PLCY	R/W	0x0	0x0	Auxiliary policy bits. MCS outputs the auxiliary bits to downstream for external functions such as Non-Disruptive Loopback (NDL).
68:67	SC	R/W	0x0	0x0	Identifies the SC for this Flow.
66	CTRL_PKT	R/W	0x0	0x0	Identifies all packets matching the associated Flow-ID lookup as control packets.
65:64	SECY	R/W	0x0	0x0	Identifies the SecY for this Flow.
63:0	SECTAG_SCI	R/W	0x00000	0x00000	Identifies the SecTAG SCI for this Flow.

Table 644: SECY_MAP_MEM2
Device 0x1F, Register 0x19C0

Bits	Field	Mode	HW Rst	SW Rst	Description
69	AUXILIARY_PLCY	R/W	0x0	0x0	Auxiliary policy bits. MCS outputs the auxiliary bits to downstream for external functions such as Non-Disruptive Loopback (NDL).

Table 644: SECY_MAP_MEM2
Device 0x1F, Register 0x19C0

Bits	Field	Mode	HW Rst	SW Rst	Description
68:67	SC	R/W	0x0	0x0	Identifies the SC for this Flow.
66	CTRL_PKT	R/W	0x0	0x0	Identifies all packets matching the associated Flow-ID lookup as control packets.
65:64	SECY	R/W	0x0	0x0	Identifies the SecY for this Flow.
63:0	SECTAG_SCI	R/W	0x00000	0x00000	Identifies the SecTAG SCI for this Flow.

Table 645: SECY_MAP_MEM3
Device 0x1F, Register 0x19C8

Bits	Field	Mode	HW Rst	SW Rst	Description
69	AUXILIARY_PLCY	R/W	0x0	0x0	Auxiliary policy bits. MCS outputs the auxiliary bits to downstream for external functions such as Non-Disruptive Loopback (NDL).
68:67	SC	R/W	0x0	0x0	Identifies the SC for this Flow.
66	CTRL_PKT	R/W	0x0	0x0	Identifies all packets matching the associated Flow-ID lookup as control packets.
65:64	SECY	R/W	0x0	0x0	Identifies the SecY for this Flow.
63:0	SECTAG_SCI	R/W	0x00000	0x00000	Identifies the SecTAG SCI for this Flow.

Table 646: SECY_PLCY_MEM0
Device 0x1F, Register 0x19F0

Bits	Field	Mode	HW Rst	SW Rst	Description
63:48	MTU	R/W	0x0000	0x0000	Specifies the outgoing maximum transmission unit (MTU) in bytes for this SecY. The MTU must be checked on egress to ensure compliance with the configured MTU due to the expansion that occurs because of inserting the SecTag and ICV into the frame. MTU violation causes CRC corruption in the outgoing frame. The MTU is checked on EOP by comparing this value against the actual computed packet length. Violation causes the packet to be truncated and EOP-errored. Note that the maximum legal value is (2^14)-1
45:40	SECTAG_TCI	R/W	0x00	0x00	Tag Control Information excluding the AN field which originates from the SA Policy table. This field is inserted into the SecTag of the outgoing packet.
38:32	SECTAG_OFFSET	R/W	0x00	0x00	Defines the offset in bytes from either the start of the packet or a matching Etype depending on SecTag_Insertion_Mode.SecTag can only be inserted into the first 128B of the frame.

Table 646: SECY_PLCY_MEM0
Device 0x1F, Register 0x19F0

Bits	Field	Mode	HW Rst	SW Rst	Description
30	SECTAG_INSERT_MODE	R/W	0x0	0x0	Defines how to handle SecTag insertion on egress. 0 = SecTag is inserted at SecTag_Offset bytes following an E-Type matching a special E-Type value (Relative Offset Mode). 1 = SecTag is inserted at SecTag_Offset bytes from the first byte of the outer DA (Fixed Offset Mode).
28	ICV_INCLUDES_DA_SA	R/W	0x0	0x0	When set, the outer DA/SA bytes are included in the authentication GHASH calculation. Both standard MACsec and WAN based MACsec with VLAN tags in the clear require the DA+SA to be included in the authentication. WAN based MPLS MACsec would typically have the DA+SA excluded from authentication since these fields can be modified by the NextHop lookup in MPLS routers.
26:20	CONFIDENTIALITY_OFFSET	R/W	0x00	0x00	Defines the number of bytes that are unencrypted following the SecTag.
15:12	CIPHER	R/W	0x0	0x0	Defines the cipher suite to use for this SecY. This is an enum with the following supported options: 0 = GCM-AES-128 1 = GCM-AES-256 2 = GCM-AES-XPN-128 3 = GCM-AES-XPN-256
4	PROTECT_FRAMES	R/W	0x0	0x0	0 = Do not encrypt or authenticate this packet. 1 = Always Authenticate frame and if SecTag.TCI. E = 1 encrypt the packet as well.
0	CONTROLLED_PORT_ENABLED	R/W	0x0	0x0	Enable (or disable) operation of the Controlled port associated with this SecY. This can be used to disable the Controlled port and drop all data packets until the secure connectivity has been fully established.

Table 647: SECY_PLCY_MEM1
Device 0x1F, Register 0x19F4

Bits	Field	Mode	HW Rst	SW Rst	Description
63:48	MTU	R/W	0x0000	0x0000	Specifies the outgoing maximum transmission unit (MTU) in bytes for this SecY. The MTU must be checked on egress to ensure compliance with the configured MTU due to the expansion that occurs because of inserting the SecTag and ICV into the frame. MTU violation causes CRC corruption in the outgoing frame. The MTU is checked on EOP by comparing this value against the actual computed packet length. Violation causes the packet to be truncated and EOP-errored. Note that the maximum legal value is (2^14)-1

Table 647: SECY_PLCY_MEM1
Device 0x1F, Register 0x19F4

Bits	Field	Mode	HW Rst	SW Rst	Description
45:40	SECTAG_TCI	R/W	0x00	0x00	Tag Control Information excluding the AN field which originates from the SA Policy table. This field is inserted into the SecTag of the outgoing packet.
38:32	SECTAG_OFFSET	R/W	0x00	0x00	Defines the offset in bytes from either the start of the packet or a matching Etype depending on SecTag_Insertion_Mode.SecTag can only be inserted into the first 128B of the frame.
30	SECTAG_INSERT_MODE	R/W	0x0	0x0	Defines how to handle SecTag insertion on egress. 0 = SecTag is inserted at SecTag_Offset bytes following an E-Type matching a special E-Type value (Relative Offset Mode). 1 = SecTag is inserted at SecTag_Offset bytes from the first byte of the outer DA (Fixed Offset Mode).
28	ICV_INCLUDES_DA_SA	R/W	0x0	0x0	When set, the outer DA/SA bytes are included in the authentication GHASH calculation. Both standard MACsec and WAN based MACsec with VLAN tags in the clear require the DA+SA to be included in the authentication. WAN based MPLS MACsec would typically have the DA+SA excluded from authentication since these fields can be modified by the NextHop lookup in MPLS routers.
26:20	CONFIDENTIALITY_OFFSET	R/W	0x00	0x00	Defines the number of bytes that are unencrypted following the SecTag.
15:12	CIPHER	R/W	0x0	0x0	Defines the cipher suite to use for this SecY This is an enum with the following supported options: 0 = GCM-AES-128 1 = GCM-AES-256 2 = GCM-AES-XPN-128 3 = GCM-AES-XPN-256
4	PROTECT_FRAMES	R/W	0x0	0x0	0 = Do not encrypt or authenticate this packet. 1 = Always Authenticate frame and if SecTag.TCI. E = 1 encrypt the packet as well.
0	CONTROLLED_PORT_ENABLED	R/W	0x0	0x0	Enable (or disable) operation of the Controlled port associated with this SecY. This can be used to disable the Controlled port and drop all data packets until the secure connectivity has been fully established.

Table 648: SECY_PLCY_MEM2
Device 0x1F, Register 0x19F8

Bits	Field	Mode	HW Rst	SW Rst	Description
63:48	MTU	R/W	0x0000	0x0000	Specifies the outgoing maximum transmission unit (MTU) in bytes for this SecY. The MTU must be checked on egress to ensure compliance with the configured MTU due to the expansion that occurs because of inserting the SecTag and ICV into the frame. MTU violation causes CRC corruption in the outgoing frame. The MTU is checked on EOP by comparing this value against the actual computed packet length. Violation causes the packet to be truncated and EOP-errored. Note that the maximum legal value is (2^14)-1
45:40	SECTAG_TCI	R/W	0x00	0x00	Tag Control Information excluding the AN field which originates from the SA Policy table. This field is inserted into the SecTag of the outgoing packet.
38:32	SECTAG_OFFSET	R/W	0x00	0x00	Defines the offset in bytes from either the start of the packet or a matching Etype depending on SecTag_Insertion_Mode.SecTag can only be inserted into the first 128B of the frame.
30	SECTAG_INSERT_MODE	R/W	0x0	0x0	Defines how to handle SecTag insertion on egress. 0 = SecTag is inserted at SecTag_Offset bytes following an E-Type matching a special E-Type value (Relative Offset Mode). 1 = SecTag is inserted at SecTag_Offset bytes from the first byte of the outer DA (Fixed Offset Mode).
28	ICV_INCLUDES_DA_SA	R/W	0x0	0x0	When set, the outer DA/SA bytes are included in the authentication GHASH calculation. Both standard MACsec and WAN-based MACsec with VLAN tags in the clear require the DA+SA to be included in the authentication. WAN based MPLS MACsec would typically have the DA+SA excluded from authentication since these fields can be modified by the NextHop lookup in MPLS routers.
26:20	CONFIDENTIALITY_OFFSET	R/W	0x00	0x00	Defines the number of bytes that are unencrypted following the SecTag.
15:12	CIPHER	R/W	0x0	0x0	Defines the cipher suite to use for this SecY This is an enum with the following supported options: 0 = GCM-AES-128 1 = GCM-AES-256 2 = GCM-AES-XPN-128 3 = GCM-AES-XPN-256
4	PROTECT_FRAMES	R/W	0x0	0x0	0 = Do not encrypt or authenticate this packet. 1 = Always Authenticate frame and if SecTag.TCI. E = 1 encrypt the packet as well.
0	CONTROLLED_PORT_ENABLED	R/W	0x0	0x0	Enable (or disable) operation of the Controlled port associated with this SecY. This can be used to disable the Controlled port and drop all data packets until the secure connectivity has been fully established.

Table 649: SECY_PLCY_MEM3
Device 0x1F, Register 0x19FC

Bits	Field	Mode	HW Rst	SW Rst	Description
63:48	MTU	R/W	0x0000	0x0000	Specifies the outgoing maximum transmission unit (MTU) in bytes for this SecY. The MTU must be checked on egress to ensure compliance with the configured MTU due to the expansion that occurs because of inserting the SecTag and ICV into the frame. MTU violation causes CRC corruption in the outgoing frame. The MTU is checked on EOP by comparing this value against the actual computed packet length. Violation causes the packet to be truncated and EOP-errored. Note that the maximum legal value is (2^14)-1
45:40	SECTAG_TCI	R/W	0x00	0x00	Tag Control Information excluding the AN field which originates from the SA Policy table. This field is inserted into the SecTag of the outgoing packet.
38:32	SECTAG_OFFSET	R/W	0x00	0x00	Defines the offset in bytes from either the start of the packet or a matching Etype depending on SecTag_Insertion_Mode.SecTag can only be inserted into the first 128B of the frame.
30	SECTAG_INSERT_MODE	R/W	0x0	0x0	Defines how to handle SecTag insertion on egress. 0 = SecTag is inserted at SecTag_Offset bytes following an E-Type matching a special E-Type value (Relative Offset Mode). 1 = SecTag is inserted at SecTag_Offset bytes from the first byte of the outer DA (Fixed Offset Mode).
28	ICV_INCLUDES_DA_SA	R/W	0x0	0x0	When set, the outer DA/SA bytes are included in the authentication GHASH calculation. Both standard MACsec and WAN based MACsec with VLAN tags in the clear require the DA+SA to be included in the authentication. WAN based MPLS MACsec would typically have the DA+SA excluded from authentication since these fields can be modified by the NextHop lookup in MPLS routers.
26:20	CONFIDENTIALITY_OFFSET	R/W	0x00	0x00	Defines the number of bytes that are unencrypted following the SecTag.
15:12	CIPHER	R/W	0x0	0x0	Defines the cipher suite to use for this SecY This is an enum with the following supported options: 0 = GCM-AES-128 1 = GCM-AES-256 2 = GCM-AES-XPN-128 3 = GCM-AES-XPN-256
4	PROTECT_FRAMES	R/W	0x0	0x0	0 = Do not encrypt or authenticate this packet. 1 = Always Authenticate frame and if SecTag.TCI. E = 1 encrypt the packet as well.
0	CONTROLLED_PORT_ENABLED	R/W	0x0	0x0	Enable (or disable) operation of the Controlled port associated with this SecY. This can be used to disable the Controlled port and drop all data packets until the secure connectivity has been fully established.

Table 650: TX_SA_ACTIVE_0
Device 0x1F, Register 0x1A10

Bits	Field	Mode	HW Rst	SW Rst	Description
0	TX_SA_ACTIVE	R/W	0x0	0x0	Per SC, SA Active indicator determines which of 2 possible SAs associated to the corresponding SC is currently the active SA. If set, then sa_index1 (SA MAP memory) is the currently active SA index. If cleared, the sa_index0 (SA MAP memory) is the currently active SA index).

Table 651: TX_SA_ACTIVE_1
Device 0x1F, Register 0x1A12

Bits	Field	Mode	HW Rst	SW Rst	Description
0	TX_SA_ACTIVE	R/W	0x0	0x0	Per SC, SA Active indicator determines which of 2 possible SAs associated to the corresponding SC is currently the active SA. If set, then sa_index1 (SA MAP memory) is the currently active SA index. If cleared, the sa_index0 (SA MAP memory) is the currently active SA index).

Table 652: TX_SA_ACTIVE_2
Device 0x1F, Register 0x1A14

Bits	Field	Mode	HW Rst	SW Rst	Description
0	TX_SA_ACTIVE	R/W	0x0	0x0	Per SC, SA Active indicator determines which of 2 possible SAs associated to the corresponding SC is currently the active SA. If set, then sa_index1 (SA MAP memory) is the currently active SA index. If cleared, the sa_index0 (SA MAP memory) is the currently active SA index).

Table 653: TX_SA_ACTIVE_3
Device 0x1F, Register 0x1A16

Bits	Field	Mode	HW Rst	SW Rst	Description
0	TX_SA_ACTIVE	R/W	0x0	0x0	Per SC, SA Active indicator determines which of 2 possible SAs associated to the corresponding SC is currently the active SA. If set, then sa_index1 (SA MAP memory) is the currently active SA index. If cleared, the sa_index0 (SA MAP memory) is the currently active SA index).

Table 654: SA_INDEX0_VLD_0
Device 0x1F, Register 0x1A20

Bits	Field	Mode	HW Rst	SW Rst	Description
0	SA_INDEX0_VLD	R/W	0x0	0x0	When set, indicates that the corresponding SCsSAindex0(SAMAPmemory) is valid.

Table 655: SA_INDEX0_VLD_1
Device 0x1F, Register 0x1A22

Bits	Field	Mode	HW Rst	SW Rst	Description
0	SA_INDEX0_VLD	R/W	0x0	0x0	When set, indicates that the corresponding SCsSAindex0(SAMAPmemory) is valid.

Table 656: SA_INDEX0_VLD_2
Device 0x1F, Register 0x1A24

Bits	Field	Mode	HW Rst	SW Rst	Description
0	SA_INDEX0_VLD	R/W	0x0	0x0	When set, indicates that the corresponding SCsSAindex0(SAMAPmemory) is valid.

Table 657: SA_INDEX0_VLD_3
Device 0x1F, Register 0x1A26

Bits	Field	Mode	HW Rst	SW Rst	Description
0	SA_INDEX0_VLD	R/W	0x0	0x0	When set, indicates that the corresponding SCsSAindex0 (SAMAPmemory) is valid.

Table 658: SA_INDEX1_VLD_0
Device 0x1F, Register 0x1A30

Bits	Field	Mode	HW Rst	SW Rst	Description
0	SA_INDEX1_VLD	R/W	0x0	0x0	When set, indicates that the corresponding SCsSAindex1 (SAMAPmemory) is valid.

Table 659: SA_INDEX1_VLD_1
Device 0x1F, Register 0x1A32

Bits	Field	Mode	HW Rst	SW Rst	Description
0	SA_INDEX1_VLD	R/W	0x0	0x0	When set, indicates that the corresponding SCs SA index1 (SAMAP memory) is valid.

Table 660: SA_INDEX1_VLD_2
Device 0x1F, Register 0x1A34

Bits	Field	Mode	HW Rst	SW Rst	Description
0	SA_INDEX1_VLD	R/W	0x0	0x0	When set, indicates that the corresponding SCs SA index1 (SAMAP memory) is valid.

Table 661: SA_INDEX1_VLD_3
Device 0x1F, Register 0x1A36

Bits	Field	Mode	HW Rst	SW Rst	Description
0	SA_INDEX1_VLD	R/W	0x0	0x0	When set, indicates that the corresponding SCs SA index1 (SAMAP memory) is valid.

Table 662: SA_MAP_MEM0
Device 0x1F, Register 0x1A40

Bits	Field	Mode	HW Rst	SW Rst	Description
5:3	SA_INDEX1	R/W	0x0	0x0	SA index1 to use for this packet
2:0	SA_INDEX0	R/W	0x0	0x0	SA index0 to use for this packet

Table 663: SA_MAP_MEM1
Device 0x1F, Register 0x1A44

Bits	Field	Mode	HW Rst	SW Rst	Description
5:3	SA_INDEX1	R/W	0x0	0x0	SA index1 to use for this packet
2:0	SA_INDEX0	R/W	0x0	0x0	SA index0 to use for this packet

Table 664: SA_MAP_MEM2
Device 0x1F, Register 0x1A48

Bits	Field	Mode	HW Rst	SW Rst	Description
5:3	SA_INDEX1	R/W	0x0	0x0	SA index1 to use for this packet
2:0	SA_INDEX0	R/W	0x0	0x0	SA index0 to use for this packet

Table 665: SA_MAP_MEM3
Device 0x1F, Register 0x1A4C

Bits	Field	Mode	HW Rst	SW Rst	Description
5:3	SA_INDEX1	R/W	0x0	0x0	SA index1 to use for this packet
2:0	SA_INDEX0	R/W	0x0	0x0	SA index0 to use for this packet

Table 666: SA_PLCY_MEM0
Device 0x1F, Register 0x1A80

Bits	Field	Mode	HW Rst	SW Rst	Description
513:512	SECTAG_AN	R/W	0x0	0x0	2b SecTag Association Number (AN):
511:480	SSCI	R/W	0x0	0x0	32b SSCI value: Short Secure Channel Identifier, used in XPN ciphers.
479:384	SALT	R/W	0x00	0x00	96b Salt value: Salt value used in XPN ciphers.
383:256	HASHKEY	R/W	0x000	0x000	128b Hash Key: Key used for authentication. This is derived by performing a 128/256-bit AES-ECB block encryption of an all 0s block with the SAK;E(SAK, 128h0). The cipher text result of this operation is the HKey software must configure in this entry.
255:0	SAK	R/W	0x00000000000000000000000000000000	0x00000000000000000000000000000000	256b SAK: Defines the encryption key to be used to decrypt this packet. The lower 128 bits are used for 128-bit ciphers.

Table 667: SA_PLCY_MEM1
Device 0x1F, Register 0x1AC0

Bits	Field	Mode	HW Rst	SW Rst	Description
513:512	SECTAG_AN	R/W	0x0	0x0	2b SecTag Association Number (AN):

Table 667: SA_PLCY_MEM1
Device 0x1F, Register 0x1AC0

Bits	Field	Mode	HW Rst	SW Rst	Description
511:480	SSCI	R/W	0x0	0x0	32b SSCI value: Short Secure Channel Identifier, used in XPN ciphers.
479:384	SALT	R/W	0x00	0x00	96b Salt value: Salt value used in XPN ciphers.
383:256	HASHKEY	R/W	0x000	0x000	128b Hash Key: Key used for authentication. This is derived by performing a 128/256-bit AES-ECB block encryption of an all 0s block with the SAK;E(SAK, 128h0). The cipher text result of this operation is the HKey software must configure in this entry.
255:0	SAK	R/W	0x00000000000000000000000000000000	0x00000000000000000000000000000000	256b SAK: Defines the encryption key to be used to decrypt this packet. The lower 128 bits are used for 128-bit ciphers.

Table 668: SA_PLCY_MEM2
Device 0x1F, Register 0x1B00

Bits	Field	Mode	HW Rst	SW Rst	Description
513:512	SECTAG_AN	R/W	0x0	0x0	2b SecTag Association Number (AN):
511:480	SSCI	R/W	0x0	0x0	32b SSCI value: Short Secure Channel Identifier, used in XPN ciphers.
479:384	SALT	R/W	0x00	0x00	96b Salt value: Salt value used in XPN ciphers.
383:256	HASHKEY	R/W	0x000	0x000	128b Hash Key: Key used for authentication. This is derived by performing a 128/256-bit AES-ECB block encryption of an all 0s block with the SAK;E(SAK, 128h0). The cipher text result of this operation is the HKey software must configure in this entry.
255:0	SAK	R/W	0x00000000000000000000000000000000	0x00000000000000000000000000000000	256b SAK: Defines the encryption key to be used to decrypt this packet. The lower 128 bits are used for 128-bit ciphers.

Table 669: SA_PLCY_MEM3
Device 0x1F, Register 0x1B40

Bits	Field	Mode	HW Rst	SW Rst	Description
513:512	SECTAG_AN	R/W	0x0	0x0	2b SecTag Association Number (AN):

Table 669: SA_PLCY_MEM3
Device 0x1F, Register 0x1B40

Bits	Field	Mode	HW Rst	SW Rst	Description
511:480	SSCI	R/W	0x0	0x0	32b SSCI value: Short Secure Channel Identifier, used in XPN ciphers.
479:384	SALT	R/W	0x000000	0x000000	96b Salt value: Salt value used in XPN ciphers.
383:256	HASHKEY	R/W	0x0000000000000000	0x0000000000000000	128b Hash Key: Key used for authentication. This is derived by performing a 128/256-bit AES-ECB block encryption of an all 0s block with the SAK;E(SAK, 128h0). The cipher text result of this operation is the HKey software must configure in this entry.'
255:0	SAK	R/W	0x0000000000000000000000000000000000000000000000	0x0000000000000000000000000000000000000000000000	256b SAK: Defines the encryption key to be used to decrypt this packet. The lower 128 bits are used for 128-bit ciphers.

Table 670: SA_PLCY_MEM4
Device 0x1F, Register 0x1B80

Bits	Field	Mode	HW Rst	SW Rst	Description
513:512	SECTAG_AN	R/W	0x0	0x0	2b SecTag Association Number (AN):
511:480	SSCI	R/W	0x0	0x0	32b SSCI value: Short Secure Channel Identifier, used in XPN ciphers.
479:384	SALT	R/W	0x000000	0x000000	96b Salt value: Salt value used in XPN ciphers.
383:256	HASHKEY	R/W	0x0000000000000000	0x0000000000000000	128b Hash Key: Key used for authentication. This is derived by performing a 128/256-bit AES-ECB block encryption of an all 0s block with the SAK;E(SAK, 128h0). The cipher text result of this operation is the HKey software must configure in this entry.'
255:0	SAK	R/W	0x0000000000000000000000000000000000000000000000	0x0000000000000000000000000000000000000000000000	256b SAK: Defines the encryption key to be used to decrypt this packet. The lower 128 bits are used for 128-bit ciphers.

Table 671: SA_PLCY_MEM5
Device 0x1F, Register 0x1BC0

Bits	Field	Mode	HW Rst	SW Rst	Description
513:512	SECTAG_AN	R/W	0x0	0x0	2b SecTag Association Number (AN):
511:480	SSCI	R/W	0x0	0x0	32b SSCI value: Short Secure Channel Identifier, used in XPN ciphers.
479:384	SALT	R/W	0x000000	0x000000	96b Salt value: Salt value used in XPN ciphers.
383:256	HASHKEY	R/W	0x0000000000000000	0x0000000000000000	128b Hash Key: Key used for authentication. This is derived by performing a 128/256-bit AES-ECB block encryption of an all 0s block with the SAK;E(SAK, 128h0). The cipher text result of this operation is the HKey software must configure in this entry.
255:0	SAK	R/W	0x0000000000000000000000000000000000000000000000	0x0000000000000000000000000000000000000000000000	256b SAK: Defines the encryption key to be used to decrypt this packet. The lower 128 bits are used for 128-bit ciphers.

Table 672: SA_PLCY_MEM6
Device 0x1F, Register 0x1C00

Bits	Field	Mode	HW Rst	SW Rst	Description
513:512	SECTAG_AN	R/W	0x0	0x0	2b SecTag Association Number (AN):
511:480	SSCI	R/W	0x0	0x0	32b SSCI value: Short Secure Channel Identifier, used in XPN ciphers.
479:384	SALT	R/W	0x000000	0x000000	96b Salt value: Salt value used in XPN ciphers.
383:256	HASHKEY	R/W	0x0000000000000000	0x0000000000000000	128b Hash Key: Key used for authentication. This is derived by performing a 128/256-bit AES-ECB block encryption of an all 0s block with the SAK;E(SAK, 128h0). The cipher text result of this operation is the HKey software must configure n this entry.
255:0	SAK	R/W	0x0000000000000000000000000000000000000000000000	0x0000000000000000000000000000000000000000000000	256b SAK: Defines the encryption key to be used to decrypt this packet. The lower 128 bits are used for 128-bit ciphers.

Table 673: SA_PLCY_MEM7
Device 0x1F, Register 0x1C40

Bits	Field	Mode	HW Rst	SW Rst	Description
513:512	SECTAG_AN	R/W	0x0	0x0	2b SecTag Association Number (AN):
511:480	SSCI	R/W	0x0	0x0	32b SSCI value: Short Secure Channel Identifier, used in XPN ciphers.
479:384	SALT	R/W	0x0	0x0	96b Salt value: Salt value used in XPN ciphers.
383:256	HASHKEY	R/W	0x0	0x0	128b Hash Key: Key used for authentication. This is derived by performing a 128/256 bit AES-ECB block encryption of an all 0s block with the SAK;E(SAK, 128h0). The cipher text result of this operation is the HKey software must configure in this entry.
255:0	SAK	R/W	0x0	0x0	256b SAK: Defines the encryption key to be used to decrypt this packet. The lower 128 bits are used for 128-bit ciphers.

Table 674: SA_PN_TABLE_MEM0
Device 0x1F, Register 0x1E80

Bits	Field	Mode	HW Rst	SW Rst	Description
63:0	NEXT_PN	R/W	0x00000	0x00000	64b next_pn value: Next packet number to insert into outgoing packet on a particular SA.

Table 675: SA_PN_TABLE_MEM1
Device 0x1F, Register 0x1E84

Bits	Field	Mode	HW Rst	SW Rst	Description
63:0	NEXT_PN	R/W	0x00000	0x00000	64b next_pn value: Next packet number to insert into outgoing packet on a particular SA.

Table 676: SA_PN_TABLE_MEM2
Device 0x1F, Register 0x1E88

Bits	Field	Mode	HW Rst	SW Rst	Description
63:0	NEXT_PN	R/W	0x00000	0x00000	64b next_pn value: Next packet number to insert into outgoing packet on a particular SA.

Table 677: SA_PN_TABLE_MEM3
Device 0x1F, Register 0x1E8C

Bits	Field	Mode	HW Rst	SW Rst	Description
63:0	NEXT_PN	R/W	0x00000	0x00000	64b next_pn value: Next packet number to insert into outgoing packet on a particular SA.

Table 678: SA_PN_TABLE_MEM4
Device 0x1F, Register 0x1E90

Bits	Field	Mode	HW Rst	SW Rst	Description
63:0	NEXT_PN	R/W	0x00000	0x00000	64b next_pn value: Next packet number to insert into outgoing packet on a particular SA.

Table 679: SA_PN_TABLE_MEM5
Device 0x1F, Register 0x1E94

Bits	Field	Mode	HW Rst	SW Rst	Description
63:0	NEXT_PN	R/W	0x00000	0x00000	64b next_pn value: Next packet number to insert into outgoing packet on a particular SA.

Table 680: SA_PN_TABLE_MEM6
Device 0x1F, Register 0x1E98

Bits	Field	Mode	HW Rst	SW Rst	Description
63:0	NEXT_PN	R/W	0x00000	0x00000	64b next_pn value: Next packet number to insert into outgoing packet on a particular SA.

Table 681: SA_PN_TABLE_MEM7
Device 0x1F, Register 0x1E9C

Bits	Field	Mode	HW Rst	SW Rst	Description
63:0	NEXT_PN	R/W	0x00000	0x00000	64b next_pn value: Next packet number to insert into outgoing packet on a particular SA.

Table 682: TX_FLOWID_TCAM_ENABLE_0
Device 0x1F, Register 0x1EC0

Bits	Field	Mode	HW Rst	SW Rst	Description
3:0	ENABLE	R/W	0x0	0x0	Set to 1 to enable the corresponding TCAM entry to be part of the TCAM search/compare.

Table 683: FLOWID_TCAM_DATA0
Device 0x1F, Register 0x1ED0

Bits	Field	Mode	HW Rst	SW Rst	Description
202	PORT	R/W	0x0	0x0	Port number, 0-3.
201	EXPRESS	R/W	0x0	0x0	Express packet.
200:194	NUM_TAGS	R/W	0x00	0x00	Number of VLAN tags, CUSTOM tags, or MPLS labels before the SecTAG, excluding the Rx/Tx-MCS header tags. Bit 0: no tags/labels before SecTAG Bit 1: 1 tag/label before SecTAG Bit 2: 2 tags/labels before SecTAG ... Bit 6: 6 or more tags/labels before SecTAG.
193:191	INNER_VLAN_TYPE	R/W	0x0	0x0	Encoded value indicating which VLAN TPID value matched for the second outermost VLAN Tag.
190:188	OUTER_VLAN_TYPE	R/W	0x0	0x0	Encoded value indicating which VLAN TPID value matched for the outermost VLAN Tag.
187:184	PACKET_TYPE	R/W	0x0	0x0	Encoded Packet Type from the parser: 0: No VLAN or MPLS 1: Single VLAN 2: Dual VLAN 3: MPLS4: Single VLAN followed by MPLS 5: Dual VLAN followed by MPLS 6: Unsupported type (2 VLAN or 4 MPLS) 7-14: Reserved for future use 15: Invalid (any parsing error)
183:176	TAG_MATCH_BIT-MAP	R/W	0x00	0x00	Maps 1 to 1 with the set of configurable Etype CSRs and set when the associated E-Type (or TPID) was found in the first 6 tags of the packet.
175:160	BONUS_DATA	R/W	0x0000	0x0000	2 bytes of additional bonus data extracted from one of the custom tags.
159:156	SECOND_OUTER_ PRIORITY	R/W	0x0	0x0	2nd Outermost VLAN {PCP/P bits, DE/CFI} or {1b0,EXP}forMPLS.
155:136	SECOND_OUTER_ TAG_ID	R/W	0x00000	0x00000	2nd Outermost VLAN ID {8d0,VLAN_ID[11:0]},or 20-bit MPLS label.
135:132	OUTER_PRIORITY	R/W	0x0	0x0	Outermost VLAN {PCP/P bits, DE/CFI} or {1b0,EXP} for MPLS.

Table 683: FLOWID_TCAM_DATA0 (Continued)
Device 0x1F, Register 0x1ED0

Bits	Field	Mode	HW Rst	SW Rst	Description
131:112	OUTER_TAG_ID	R/W	0x00000	0x00000	Outermost VLAN ID {8d0,VLAN_ID[11:0]},or 20-bit MPLS label.
111:96	ETHER_TYPE	R/W	0x0000	0x0000	First E-Type found in the packet that does not match one of the preconfigured Custom, VLAN, or MPLS values.
95:48	MAC_SA	R/W	0x0	0x0	MAC SA field extracted from the packet
47:0	MAC_DA	R/W	0x0	0x0	MAC DA field extracted from the packet

Table 684: FLOWID_TCAM_DATA1
Device 0x1F, Register 0x1EE0

Bits	Field	Mode	HW Rst	SW Rst	Description
202	PORT	R/W	0x0	0x0	Port number, 0-3.
201	EXPRESS	R/W	0x0	0x0	Express packet.
200:194	NUM_TAGS	R/W	0x00	0x00	Number of VLAN tags, CUSTOM tags, or MPLS labels before the SecTAG, excluding the Rx/Tx-MCS header tags. Bit 0: No tags/labels before SecTAG Bit 1: 1 tag/label before SecTAG Bit 2: 2 tags/labels before SecTAG ... Bit 6: 6 or more tags/labels before SecTAG.
193:191	INNER_VLAN_TYPE	R/W	0x0	0x0	Encoded value indicating which VLAN TPID value matched for the second outermost VLAN Tag.
190:188	OUTER_VLAN_TYPE	R/W	0x0	0x0	Encoded value indicating which VLAN TPID value matched for the outermost VLAN Tag.
187:184	PACKET_TYPE	R/W	0x0	0x0	Encoded Packet Type from the parser: 0: No VLAN or MPLS 1: Single VLAN 2: Dual VLAN 3: MPLS 4: Single VLAN followed by MPLS 5: Dual VLAN followed by MPLS 6: Unsupported type (2 VLAN or 4 MPLS) 7-14: Reserved for future use 15: Invalid (any parsing error)
183:176	TAG_MATCH_BIT-MAP	R/W	0x00	0x00	Maps 1 to 1 with the set of configurable Etype CSRs and set when the associated E-Type (or TPID) was found in the first 6 tags of the packet.
175:160	BONUS_DATA	R/W	0x0000	0x0000	2 bytes of additional bonus data extracted from one of the custom tags.
159:156	SECOND_OUTER_ PRIORITY	R/W	0x0	0x0	2nd Outermost VLAN {PCP/P bits, DE/CFI} or {1b0,EXP} for MPLS.

Table 684: FLOWID_TCAM_DATA1 (Continued)
Device 0x1F, Register 0x1EE0

Bits	Field	Mode	HW Rst	SW Rst	Description
155:136	SECOND_OUTER_TAG_ID	R/W	0x00000	0x00000	2nd Outermost VLAN ID {8d0,VLAN_ID[11:0]},or 20-bit MPLS label.
135:132	OUTER_PRIORITY	R/W	0x0	0x0	Outermost VLAN {PCP/P bits, DE/CFI} or {1b0,EXP} for MPLS.
131:112	OUTER_TAG_ID	R/W	0x00000	0x00000	Outermost VLAN ID {8d0,VLAN_ID[11:0]},or 20-bit MPLS label.
111:96	ETHER_TYPE	R/W	0x0000	0x0000	First E-Type found in the packet that does not match one of the preconfigured Custom, VLAN, or MPLS values.
95:48	MAC_SA	R/W	0x0	0x0	MAC SA field extracted from the packet
47:0	MAC_DA	R/W	0x0	0x0	MAC DA field extracted from the packet

Table 685: FLOWID_TCAM_DATA2
Device 0x1F, Register 0x1EF0

Bits	Field	Mode	HW Rst	SW Rst	Description
202	PORT	R/W	0x0	0x0	Port number, 0-3.
201	EXPRESS	R/W	0x0	0x0	Express packet.
200:194	NUM_TAGS	R/W	0x00	0x00	Number of VLAN tags, CUSTOM tags, or MPLS labels before the SecTAG, excluding the Rx/Tx-MCS header tags. Bit 0: no tags/labels before SecTAG Bit 1: 1 tag/label before SecTAG Bit 2: 2 tags/labels before SecTAG ... Bit 6: 6 or more tags/labels before SecTAG.
193:191	INNER_VLAN_TYPE	R/W	0x0	0x0	Encoded value indicating which VLAN TPID value matched for the second outermost VLAN Tag.
190:188	OUTER_VLAN_TYPE	R/W	0x0	0x0	Encoded value indicating which VLAN TPID value matched for the outermost VLAN Tag.
187:184	PACKET_TYPE	R/W	0x0	0x0	Encoded Packet Type from the parser: 0: No VLAN or MPLS 1: Single VLAN 2: Dual VLAN 3: MPLS 4: Single VLAN followed by MPLS 5: Dual VLAN followed by MPLS 6: Unsupported type (2 VLAN or 4 MPLS) 7-14: Reserved for future use 15: Invalid (any parsing error)
183:176	TAG_MATCH_BIT-MAP	R/W	0x00	0x00	Maps 1 to 1 with the set of configurable Etype CSRs and set when the associated E-Type (or TPID) was found in the first 6 tags of the packet.

Table 685: FLOWID_TCAM_DATA2
Device 0x1F, Register 0x1EF0

Bits	Field	Mode	HW Rst	SW Rst	Description
175:160	BONUS_DATA	R/W	0x0000	0x0000	2 bytes of additional bonus data extracted from one of the custom tags.
159:156	SECOND_OUTER_PRIORITY	R/W	0x0	0x0	2nd Outermost VLAN {PCP/P bits, DE/CFI} or {1b0,EXP} for MPLS.
155:136	SECOND_OUTER_TAG_ID	R/W	0x00000	0x00000	2nd Outermost VLAN ID {8d0,VLAN_ID[11:0]}, or 20-bit MPLS label.
135:132	OUTER_PRIORITY	R/W	0x0	0x0	Outermost VLAN {PCP/P bits, DE/CFI} or {1b0,EXP} for MPLS.
131:112	OUTER_TAG_ID	R/W	0x00000	0x00000	Outermost VLAN ID {8d0,VLAN_ID[11:0]}, or 20-bit MPLS label.
111:96	ETHER_TYPE	R/W	0x0000	0x0000	First E-Type found in the packet that does not match one of the preconfigured Custom, VLAN, or MPLS values.
95:48	MAC_SA	R/W	0x0	0x0	MAC SA field extracted from the packet
47:0	MAC_DA	R/W	0x0	0x0	MAC DA field extracted from the packet

Table 686: FLOWID_TCAM_DATA3
Device 0x1F, Register 0x1F00

Bits	Field	Mode	HW Rst	SW Rst	Description
202	PORT	R/W	0x0	0x0	Port number, 0-3.
201	EXPRESS	R/W	0x0	0x0	Express packet.
200:194	NUM_TAGS	R/W	0x00	0x00	Number of VLAN tags, CUSTOM tags, or MPLS labels before the SecTAG, excluding the Rx/Tx-MCS header tags. Bit 0: no tags/labels before SecTAG Bit 1: 1 tag/label before SecTAG Bit 2: 2 tags/labels before SecTAG ... Bit 6: 6 or more tags/labels before SecTAG.
193:191	INNER_VLAN_TYPE	R/W	0x0	0x0	Encoded value indicating which VLAN TPID value matched for the second outermost VLAN Tag.
190:188	OUTER_VLAN_TYPE	R/W	0x0	0x0	Encoded value indicating which VLAN TPID value matched for the outermost VLAN Tag.

Table 686: FLOWID_TCAM_DATA3
Device 0x1F, Register 0x1F00

Bits	Field	Mode	HW Rst	SW Rst	Description
187:184	PACKET_TYPE	R/W	0x0	0x0	Encoded Packet Type from the parser: 0: No VLAN or MPLS 1: Single VLAN 2: Dual VLAN 3: MPLS 4: Single VLAN followed by MPLS 5: Dual VLAN followed by MPLS 6: Unsupported type (2 VLAN or 4 MPLS) 7-14: Reserved for future use 15: Invalid (any parsing error)
183:176	TAG_MATCH_BIT-MAP	R/W	0x00	0x00	Maps 1 to 1 with the set of configurable Etype CSRs and set when the associated E-Type (or TPID) was found in the first 6 tags of the packet.
175:160	BONUS_DATA	R/W	0x0000	0x0000	2 bytes of additional bonus data extracted from one of the custom tags.
159:156	SECOND_OUTER_ PRIORITY	R/W	0x0	0x0	2nd Outermost VLAN {PCP/P bits, DE/CFI} or {1b0,EXP} for MPLS.
155:136	SECOND_OUTER_ TAG_ID	R/W	0x00000	0x00000	2nd Outermost VLAN ID {8d0,VLAN_ID[11:0]}, or 20-bit MPLS label.
135:132	OUTER_PRIORITY	R/W	0x0	0x0	Outermost VLAN {PCP/P bits, DE/CFI} or {1b0,EXP} for MPLS.
131:112	OUTER_TAG_ID	R/W	0x00000	0x00000	Outermost VLAN ID {8d0,VLAN_ID[11:0]}, or 20-bit MPLS label.
111:96	ETHER_TYPE	R/W	0x0000	0x0000	First E-Type found in the packet that does not match one of the preconfigured Custom, VLAN, or MPLS values.
95:48	MAC_SA	R/W	0x0	0x0	MAC SA field extracted from the packet
47:0	MAC_DA	R/W	0x0	0x0	MAC DA field extracted from the packet

Table 687: FLOWID_TCAM_MASK0
Device 0x1F, Register 0x1F50

Bits	Field	Mode	HW Rst	SW Rst	Description
202	MASK_PORT	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.
201	MASK_EXPRESS	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.
200:194	MASK_NUM_TAGS	R/W	0x00	0x00	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.
193:191	MASK_INNER_VLAN_ TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.

Table 687: FLOWID_TCAM_MASK0 (Continued)
Device 0x1F, Register 0x1F50

Bits	Field	Mode	HW Rst	SW Rst	Description
190:188	MASK_OUTER_VLAN_TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
187:184	MASK_PACKET_TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
183:176	MASK_TAG_MATCH_BITMAP	R/W	0x00	0x00	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
175:160	MASK_BONUS_DATA	R/W	0x0000	0x0000	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
159:156	MASK_SECOND_OUTER_PRIORITY	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
155:136	MASK_SECOND_OUTER_TAG_ID	R/W	0x00000	0x00000	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
135:132	MASK_OUTER_PRIORITY	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
131:112	MASK_OUTER_TAG_ID	R/W	0x00000	0x00000	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
111:96	MASK_ETHER_TYPE	R/W	0x0000	0x0000	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
95:48	MASK_MAC_SA	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
47:0	MASK_MAC_DA	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.

Table 688: FLOWID_TCAM_MASK1
Device 0x1F, Register 0x1F60

Bits	Field	Mode	HW Rst	SW Rst	Description
202	MASK_PORT	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
201	MASK_EXPRESS	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
200:194	MASK_NUM_TAGS	R/W	0x00	0x00	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
193:191	MASK_INNER_VLAN_TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
190:188	MASK_OUTER_VLAN_TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
187:184	MASK_PACKET_TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.

Table 688: FLOWID_TCAM_MASK1 (Continued)
Device 0x1F, Register 0x1F60

Bits	Field	Mode	HW Rst	SW Rst	Description
183:176	MASK_TAG_MATCH_BITMAP	R/W	0x00	0x00	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
175:160	MASK_BONUS_DATA	R/W	0x0000	0x0000	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
159:156	MASK_SECOND_OUTER_PRIORITY	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
155:136	MASK_SECOND_OUTER_TAG_ID	R/W	0x00000	0x00000	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
135:132	MASK_OUTER_PRIORITY	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
131:112	MASK_OUTER_TAG_ID	R/W	0x00000	0x00000	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
111:96	MASK_ETHER_TYPE	R/W	0x0000	0x0000	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
95:48	MASK_MAC_SA	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
47:0	MASK_MAC_DA	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.

Table 689: FLOWID_TCAM_MASK2
Device 0x1F, Register 0x1F70

Bits	Field	Mode	HW Rst	SW Rst	Description
202	MASK_PORT	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
201	MASK_EXPRESS	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
200:194	MASK_NUM_TAGS	R/W	0x00	0x00	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
193:191	MASK_INNER_VLAN_TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
190:188	MASK_OUTER_VLAN_TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
187:184	MASK_PACKET_TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
183:176	MASK_TAG_MATCH_BITMAP	R/W	0x00	0x00	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.
175:160	MASK_BONUS_DATA	R/W	0x0000	0x0000	Set bits to 1 to mask/exclude corresponding flowid_tcam_data bit from compare.

Table 689: FLOWID_TCAM_MASK2 (Continued)
Device 0x1F, Register 0x1F70

Bits	Field	Mode	HW Rst	SW Rst	Description
159:156	MASK_SECOND_ OUTER_PRIORITY	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.
155:136	MASK_SECOND_ OUTER_TAG_ID	R/W	0x00000	0x00000	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.
135:132	MASK_OUTER_PRI- ORITY	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.
131:112	MASK_OUTER_TAG_ ID	R/W	0x00000	0x00000	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.
111:96	MASK_ETHER_TYPE	R/W	0x0000	0x0000	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.
95:48	MASK_MAC_SA	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.
47:0	MASK_MAC_DA	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.

Table 690: FLOWID_TCAM_MASK3
Device 0x1F, Register 0x1F80

Bits	Field	Mode	HW Rst	SW Rst	Description
202	MASK_PORT	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.
201	MASK_EXPRESS	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.
200:194	MASK_NUM_TAGS	R/W	0x00	0x00	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.
193:191	MASK_INNER_VLAN_ TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.
190:188	MASK_OUTER_ VLAN_TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.
187:184	MASK_PACKET_ TYPE	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.
183:176	MASK_TAG_MATCH_ BITMAP	R/W	0x00	0x00	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.
175:160	MASK_BONUS_DATA	R/W	0x0000	0x0000	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.
159:156	MASK_SECOND_ OUTER_PRIORITY	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.
155:136	MASK_SECOND_ OUTER_TAG_ID	R/W	0x00000	0x00000	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.

Table 690: FLOWID_TCAM_MASK3
Device 0x1F, Register 0x1F80

Bits	Field	Mode	HW Rst	SW Rst	Description
135:132	MASK_OUTER_PRI-ORITY	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.
131:112	MASK_OUTER_TAG_ ID	R/W	0x00000	0x00000	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.
111:96	MASK_ETHER_TYPE	R/W	0x0000	0x0000	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.
95:48	MASK_MAC_SA	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.
47:0	MASK_MAC_DA	R/W	0x0	0x0	Set bits to 1 to mask/exclude corresponding flowid_tcam_ data bit from compare.

Table 691: IFINCTLOCTETS0
Device 0x1F, Register 0x3300

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_CTL_OCTET_ CNT	R/W	0x0	0x0	Ingress Total MSDU and MAC-DA/SA Octets that are per-mitted by the controlled port policies of this SecY.

Table 692: IFINCTLOCTETS1
Device 0x1F, Register 0x3304

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_CTL_OCTET_ CNT	R/W	0x0	0x0	Ingress Total MSDU and MAC-DA/SA Octets that are per-mitted by the controlled port policies of this SecY.

Table 693: IFINCTLOCTETS2
Device 0x1F, Register 0x3308

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_CTL_OCTET_ CNT	R/W	0x0	0x0	Ingress Total MSDU and MAC-DA/SA Octets that are per-mitted by the controlled port policies of this SecY.

Table 694: IFINCTLOCTETS3
Device 0x1F, Register 0x330C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_CTL_OCTET_CNT	R/W	0x0	0x0	Ingress Total MSDU and MAC-DA/SA Octets that are permitted by the controlled port policies of this SecY.

Table 695: IFINCTLUCPKTS0
Device 0x1F, Register 0x3310

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_CTL_PKT_UCAST_CNT	R/W	0x0	0x0	Ingress Unicast packet count value for controlled ports of this SecY.

Table 696: IFINCTLUCPKTS1
Device 0x1F, Register 0x3314

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_CTL_PKT_UCAST_CNT	R/W	0x0	0x0	Ingress Unicast packet count value for controlled ports of this SecY.

Table 697: IFINCTLUCPKTS2
Device 0x1F, Register 0x3318

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_CTL_PKT_UCAST_CNT	R/W	0x0	0x0	Ingress Unicast packet count value for controlled ports of this SecY.

Table 698: IFINCTLUCPKTS3
Device 0x1F, Register 0x331C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_CTL_PKT_UCAST_CNT	R/W	0x0	0x0	Ingress Unicast packet count value for controlled ports of this SecY.

Table 699: IFINCTLMCPKTS0
Device 0x1F, Register 0x3320

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_CTL_PKT_ MCAST_CNT	R/W	0x0	0x0	Ingress Multicast packet count value for controlled ports of this SecY.

Table 700: IFINCTLMCPKTS1
Device 0x1F, Register 0x3324

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_CTL_PKT_ MCAST_CNT	R/W	0x0	0x0	Ingress Multicast packet count value for controlled ports of this SecY.

Table 701: IFINCTLMCPKTS2
Device 0x1F, Register 0x3328

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_CTL_PKT_ MCAST_CNT	R/W	0x0	0x0	Ingress Multicast packet count value for controlled ports of this SecY.

Table 702: IFINCTLMCPKTS3
Device 0x1F, Register 0x332C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_CTL_PKT_ MCAST_CNT	R/W	0x0	0x0	Ingress Multicast packet count value for controlled ports of this SecY.

Table 703: IFINCTLBCPKTS0
Device 0x1F, Register 0x3330

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_CTL_PKT_ BCAST_CNT	R/W	0x0	0x0	Ingress Broadcast packet count value for controlled ports of this SecY.

Table 704: IFINCTLBCPKTS1
Device 0x1F, Register 0x3334

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_CTL_PKT_BCAST_CNT	R/W	0x0	0x0	Ingress Broadcast packet count value for controlled ports of this SecY.

Table 705: IFINCTLBCPKTS2
Device 0x1F, Register 0x3338

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_CTL_PKT_BCAST_CNT	R/W	0x0	0x0	Ingress Broadcast packet count value for controlled ports of this SecY.

Table 706: IFINCTLBCPKTS3
Device 0x1F, Register 0x333C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_CTL_PKT_BCAST_CNT	R/W	0x0	0x0	Ingress Broadcast packet count value for controlled ports of this SecY.

Table 707: IFINUNCTLOCTETS0
Device 0x1F, Register 0x3340

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_UNCTL_OCTET_CNT	R/W	0x0	0x0	Ingress Total MSDU and MAC-DA/SA Octets that are permitted by the uncontrolled port policies of this SecY.

Table 708: IFINUNCTLOCTETS1
Device 0x1F, Register 0x3344

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_UNCTL_OCTET_CNT	R/W	0x0	0x0	Ingress Total MSDU and MAC-DA/SA Octets that are permitted by the uncontrolled port policies of this SecY.

Table 709: IFINUNCTLOCTETS2
Device 0x1F, Register 0x3348

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_UNCTL_OCTET_CNT	R/W	0x0	0x0	Ingress Total MSDU and MAC-DA/SA Octets that are permitted by the uncontrolled port policies of this SecY.

Table 710: IFINUNCTLOCTETS3
Device 0x1F, Register 0x334C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_UNCTL_OCTET_CNT	R/W	0x0	0x0	Ingress Total MSDU and MAC-DA/SA Octets that are permitted by the uncontrolled port policies of this SecY.

Table 711: IFINUNCTLUCPKTS0
Device 0x1F, Register 0x3350

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_UNCTL_PKT_UCAST_CNT	R/W	0x0	0x0	Ingress Unicast packet count value for uncontrolled ports of this SecY.

Table 712: IFINUNCTLUCPKTS1
Device 0x1F, Register 0x3354

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_UNCTL_PKT_UCAST_CNT	R/W	0x0	0x0	Ingress Unicast packet count value for uncontrolled ports of this SecY.

Table 713: IFINUNCTLUCPKTS2
Device 0x1F, Register 0x3358

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_UNCTL_PKT_UCAST_CNT	R/W	0x0	0x0	Ingress Unicast packet count value for uncontrolled ports of this SecY.

Table 714: IFINUNCTLUCPKTS3
Device 0x1F, Register 0x335C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_UNCTL_PKT_UCAST_CNT	R/W	0x0	0x0	Ingress Unicast packet count value for uncontrolled ports of this SecY.

Table 715: IFINUNCTLMCPKTS0
Device 0x1F, Register 0x3360

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_UNCTL_PKT_MCAST_CNT	R/W	0x0	0x0	Ingress Multicast packet count value for uncontrolled ports of this SecY.

Table 716: IFINUNCTLMCPKTS1
Device 0x1F, Register 0x3364

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_UNCTL_PKT_MCAST_CNT	R/W	0x0	0x0	Ingress Multicast packet count value for uncontrolled ports of this SecY.

Table 717: IFINUNCTLMCPKTS2
Device 0x1F, Register 0x3368

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_UNCTL_PKT_MCAST_CNT	R/W	0x0	0x0	Ingress Multicast packet count value for uncontrolled ports of this SecY.

Table 718: IFINUNCTLMCPKTS3
Device 0x1F, Register 0x336C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_UNCTL_PKT_MCAST_CNT	R/W	0x0	0x0	Ingress Multicast packet count value for uncontrolled ports of this SecY.

Table 719: IFINUNCTLBCPKTS0
Device 0x1F, Register 0x3370

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_UNCTL_PKT_BCAST_CNT	R/W	0x0	0x0	Ingress Broadcast packet count value for uncontrolled ports of this SecY.

Table 720: IFINUNCTLBCPKTS1
Device 0x1F, Register 0x3374

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_UNCTL_PKT_BCAST_CNT	R/W	0x0	0x0	Ingress Broadcast packet count value for uncontrolled ports of this SecY.

Table 721: IFINUNCTLBCPKTS2
Device 0x1F, Register 0x3378

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_UNCTL_PKT_BCAST_CNT	R/W	0x0	0x0	Ingress Broadcast packet count value for uncontrolled ports of this SecY.

Table 722: IFINUNCTLBCPKTS3
Device 0x1F, Register 0x337C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_UNCTL_PKT_BCAST_CNT	R/W	0x0	0x0	Ingress Broadcast packet count value for uncontrolled ports of this SecY.

Table 723: INPKTSSECYTAGGEDCTL0
Device 0x1F, Register 0x3380

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_TAGGED_CTL_CNT	R/W	0x0	0x0	Number of tagged control packets received by the SecY.

Table 724: INPKTSSECYTAGGEDCTL1
Device 0x1F, Register 0x3384

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_ TAGGED_CTL_CNT	R/W	0x0	0x0	Number of tagged control packets received by the SecY.

Table 725: INPKTSSECYTAGGEDCTL2
Device 0x1F, Register 0x3388

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_ TAGGED_CTL_CNT	R/W	0x0	0x0	Number of tagged control packets received by the SecY.

Table 726: INPKTSSECYTAGGEDCTL3
Device 0x1F, Register 0x338C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_ TAGGED_CTL_CNT	R/W	0x0	0x0	Number of tagged control packets received by the SecY.

Table 727: INPKTSCTRLPORTDISABLED0
Device 0x1F, Register 0x3390

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_ CTRL_PORT_DIS- ABLED_CNT	R/W	0x0	0x0	The number of packets received which are dropped on disabled SecY.

Table 728: INPKTSCTRLPORTDISABLED1
Device 0x1F, Register 0x3394

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_ CTRL_PORT_DIS- ABLED_CNT	R/W	0x0	0x0	The number of packets received which are dropped on disabled SecY.

Table 729: INPKTSCTRLPORTDISABLED2
Device 0x1F, Register 0x3398

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_CTRL_PORT_DISABLED_CNT	R/W	0x0	0x0	The number of packets received which are dropped on disabled SecY.

Table 730: INPKTSCTRLPORTDISABLED3
Device 0x1F, Register 0x339C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_CTRL_PORT_DISABLED_CNT	R/W	0x0	0x0	The number of packets received which are dropped on disabled SecY.

Table 731: INPKTSSECYUNTAGGED0
Device 0x1F, Register 0x33A0

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_UNTAGGED_CNT	R/W	0x0	0x0	The number of packets without a SecTag received while SecY.Validate_Frames was not STRICT.

Table 732: INPKTSSECYUNTAGGED1
Device 0x1F, Register 0x33A4

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_UNTAGGED_CNT	R/W	0x0	0x0	The number of packets without a SecTag received while SecY.Validate_Frames was not STRICT.

Table 733: INPKTSSECYUNTAGGED2
Device 0x1F, Register 0x33A8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_UNTAGGED_CNT	R/W	0x0	0x0	The number of packets without a SecTag received while SecY.Validate_Frames was not STRICT.

Table 734: INPKTSSECYUNTAGGED3
Device 0x1F, Register 0x33AC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_ UNTAGGED_CNT	R/W	0x0	0x0	The number of packets without a SecTag received while SecY.Validate_Frames was not STRICT.

Table 735: INPKTSSECYNOTAG0
Device 0x1F, Register 0x33B0

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_ NOTAG_CNT	R/W	0x0	0x0	The number of received packets without a SecTag discarded because SecY.Validate_Frames was STRICT.

Table 736: INPKTSSECYNOTAG1
Device 0x1F, Register 0x33B4

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_ NOTAG_CNT	R/W	0x0	0x0	The number of received packets without a SecTag discarded because SecY.Validate_Frames was STRICT.

Table 737: INPKTSSECYNOTAG2
Device 0x1F, Register 0x33B8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_ NOTAG_CNT	R/W	0x0	0x0	The number of received packets without a SecTag discarded because SecY.Validate_Frames was STRICT.

Table 738: INPKTSSECYNOTAG3
Device 0x1F, Register 0x33BC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_ NOTAG_CNT	R/W	0x0	0x0	The number of received packets without a SecTag discarded because SecY.Validate_Frames was STRICT.

Table 739: INPKTSSECYBADTAG0
Device 0x1F, Register 0x33C0

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_BAD-TAG_CNT	R/W	0x0	0x0	The number of received packets discarded with an invalid SecTag, zero value PN, or invalid ICV.

Table 740: INPKTSSECYBADTAG1
Device 0x1F, Register 0x33C4

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_BAD-TAG_CNT	R/W	0x0	0x0	The number of received packets discarded with an invalid SecTag, zero value PN, or invalid ICV.

Table 741: INPKTSSECYBADTAG2
Device 0x1F, Register 0x33C8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_BAD-TAG_CNT	R/W	0x0	0x0	The number of received packets discarded with an invalid SecTag, zero value PN, or invalid ICV.

Table 742: INPKTSSECYBADTAG3
Device 0x1F, Register 0x33CC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_BAD-TAG_CNT	R/W	0x0	0x0	The number of received packets discarded with an invalid SecTag, zero value PN, or invalid ICV.

Table 743: INPKTSSECYNOSA0
Device 0x1F, Register 0x33D0

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_ NOSA_CNT	R/W	0x0	0x0	The number of received packets with an unknown SA or an unused SA.

Table 744: INPKTSSECYNOSA1
Device 0x1F, Register 0x33D4

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_ NOSA_CNT	R/W	0x0	0x0	The number of received packets with an unknown SA or an unused SA.

Table 745: INPKTSSECYNOSA2
Device 0x1F, Register 0x33D8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_ NOSA_CNT	R/W	0x0	0x0	The number of received packets with an unknown SA or an unused SA.

Table 746: INPKTSSECYNOSA3
Device 0x1F, Register 0x33DC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_ NOSA_CNT	R/W	0x0	0x0	The number of received packets with an unknown SA or an unused SA.

Table 747: INPKTSSECYNOSAERROR0
Device 0x1F, Register 0x33E0

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_ NOSAERROR_CNT	R/W	0x0	0x0	The number of received packets discarded because the received SCI is unknown on the SA is not in use.

Table 748: INPKTSSECYNOSAERROR1
Device 0x1F, Register 0x33E4

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_ NOSAERROR_CNT	R/W	0x0	0x0	The number of received packets discarded because the received SCI is unknown on the SA is not in use.

Table 749: INPKTSSECYNOSAERROR2
Device 0x1F, Register 0x33E8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_ NOSAERROR_CNT	R/W	0x0	0x0	The number of received packets discarded because the received SCI is unknown on the SA is not in use.

Table 750: INPKTSSECYNOSAERROR3
Device 0x1F, Register 0x33EC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_PKT_ NOSAERROR_CNT	R/W	0x0	0x0	The number of received packets discarded because the received SCI is unknown on the SA is not in use.

Table 751: INOCTETSSECYVALIDATE0
Device 0x1F, Register 0x33F0

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_OCTET_ VALIDATED_CNT	R/W	0x0	0x0	The number of plaintext octets recovered from packets that were integrity protected but not encrypted.

Table 752: INOCTETSSECYVALIDATE1
Device 0x1F, Register 0x33F4

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_OCTET_ VALIDATED_CNT	R/W	0x0	0x0	The number of plaintext octets recovered from packets that were integrity protected but not encrypted.

Table 753: INOCTETSSECYVALIDATE2
Device 0x1F, Register 0x33F8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_OCTET_ VALIDATED_CNT	R/W	0x0	0x0	The number of plaintext octets recovered from packets that were integrity protected but not encrypted.

Table 754: INOCTETSSECYVALIDATE3
Device 0x1F, Register 0x33FC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_OCTET_VALIDATED_CNT	R/W	0x0	0x0	The number of plaintext octets recovered from packets that were integrity protected but not encrypted.

Table 755: INOCTETSSECYDECRYPTED0
Device 0x1F, Register 0x3400

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_OCTET_DECRYPTED_CNT	R/W	0x0	0x0	The number of plaintext octets recovered from packets that were integrity protected and encrypted.

Table 756: INOCTETSSECYDECRYPTED1
Device 0x1F, Register 0x3404

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_OCTET_DECRYPTED_CNT	R/W	0x0	0x0	The number of plaintext octets recovered from packets that were integrity protected and encrypted.

Table 757: INOCTETSSECYDECRYPTED2
Device 0x1F, Register 0x3408

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_OCTET_DECRYPTED_CNT	R/W	0x0	0x0	The number of plaintext octets recovered from packets that were integrity protected and encrypted.

Table 758: INOCTETSSECYDECRYPTED3
Device 0x1F, Register 0x340C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SECY_OCTET_DECRYPTED_CNT	R/W	0x0	0x0	The number of plaintext octets recovered from packets that were integrity protected and encrypted.

Table 759: INPKTSSCLATE0
Device 0x1F, Register 0x3420

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SC_PKT_LATE_CNT	R/W	0x0	0x0	The number of packets discarded, for this SC, because the received PN was lower than the lowest acceptable PN and with replay protect true.

Table 760: INPKTSSCLATE1
Device 0x1F, Register 0x3424

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SC_PKT_LATE_CNT	R/W	0x0	0x0	The number of packets discarded, for this SC, because the received PN was lower than the lowest acceptable PN and with replay protect true.

Table 761: INPKTSSCLATE2
Device 0x1F, Register 0x3428

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SC_PKT_LATE_CNT	R/W	0x0	0x0	The number of packets discarded, for this SC, because the received PN was lower than the lowest acceptable PN and with replay protect true.

Table 762: INPKTSSCLATE3
Device 0x1F, Register 0x342C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SC_PKT_LATE_CNT	R/W	0x0	0x0	The number of packets discarded, for this SC, because the received PN was lower than the lowest acceptable PN and with replay protect true.

Table 763: INPKTSSCNOTVALID0
Device 0x1F, Register 0x3430

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SC_PKT_NOT-VALID_CNT	R/W	0x0	0x0	The number of packets discarded for this SC because validation failed and SecY.Validate_Frames is STRICT or the data was encrypted so the original frame could not be recovered.

Table 764: INPKTSSCNOTVALID1
Device 0x1F, Register 0x3434

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SC_PKT_NOT-VALID_CNT	R/W	0x0	0x0	The number of packets discarded for this SC because validation failed and SecY.Validate_Frames is STRICT or the data was encrypted so the original frame could not be recovered.

Table 765: INPKTSSCNOTVALID2
Device 0x1F, Register 0x3438

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SC_PKT_NOT-VALID_CNT	R/W	0x0	0x0	The number of packets discarded for this SC because validation failed and SecY.Validate_Frames is STRICT or the data was encrypted so the original frame could not be recovered.

Table 766: INPKTSSCNOTVALID3
Device 0x1F, Register 0x343C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SC_PKT_NOT-VALID_CNT	R/W	0x0	0x0	The number of packets discarded for this SC because validation failed and SecY.Validate_Frames is STRICT' or the data was encrypted so the original frame could not be recovered.

Table 767: INPKTSSCINVALID0
Device 0x1F, Register 0x3440

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SC_PKT_ INVALID_CNT	R/W	0x0	0x0	The number of packets for this SC that failed validation but could be received because SecY.Validate_Frames was CHECK and the data was not encrypted so the original frame could be recovered.

Table 768: INPKTSSCINVALID1
Device 0x1F, Register 0x3444

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SC_PKT_ INVALID_CNT	R/W	0x0	0x0	The number of packets for this SC that failed validation but could be received because SecY.Validate_Frames was CHECK' and the data was not encrypted so the original frame could be recovered.

Table 769: INPKTSSCINVALID2
Device 0x1F, Register 0x3448

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SC_PKT_ INVALID_CNT	R/W	0x0	0x0	The number of packets for this SC that failed validation but could be received because SecY.Validate_Frames was CHECK and the data was not encrypted, so the original frame could be recovered.

Table 770: INPKTSSCINVALID3
Device 0x1F, Register 0x344C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SC_PKT_ INVALID_CNT	R/W	0x0	0x0	The number of packets, for this SC, that failed validation but could be received because SecY.Validate_Frames was CHECK' and the data was not encrypted so the original frame could be recovered.

Table 771: INPKTSSCDELAYED0
Device 0x1F, Register 0x3450

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SC_PKT_ DELAYED_CNT	R/W	0x0	0x0	The number of received packets, for this SC, with PN lower than the lowest acceptable PN and replay protect is false.

Table 772: INPKTSSCDELAYED1
Device 0x1F, Register 0x3454

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SC_PKT_ DELAYED_CNT	R/W	0x0	0x0	The number of received packets, for this SC, with PN lower than the lowest acceptable PN and replay protect is false.

Table 773: INPKTSSCDELAYED2
Device 0x1F, Register 0x3458

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SC_PKT_ DELAYED_CNT	R/W	0x0	0x0	The number of received packets, for this SC, with PN lower than the lowest acceptable PN and replay protect is false.

Table 774: INPKTSSCDELAYED3
Device 0x1F, Register 0x345C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SC_PKT_ DELAYED_CNT	R/W	0x0	0x0	The number of received packets, for this SC, with PN lower than the lowest acceptable PN and replay protect is false.

Table 775: INPKTSSCUNCHECKED0
Device 0x1F, Register 0x3460

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SC_PKT_ UNCHECKED_CNT	R/W	0x0	0x0	The number of packets received for this SC, while Validate_Frames was disabled.

Table 776: INPKTSSCUNCHECKED1
Device 0x1F, Register 0x3464

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SC_PKT_ UNCHECKED_CNT	R/W	0x0	0x0	The number of packets received for this SC, while Validate_Frames was disabled.

Table 777: INPKTSSCUNCHECKED2
Device 0x1F, Register 0x3468

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SC_PKT_ UNCHECKED_CNT	R/W	0x0	0x0	The number of packets received for this SC, while Validate_Frames was disabled.

Table 778: INPKTSSCUNCHECKED3
Device 0x1F, Register 0x346C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SC_PKT_ UNCHECKED_CNT	R/W	0x0	0x0	The number of packets received for this SC, while Validate_Frames was disabled.

Table 779: INPKTSSCOK0
Device 0x1F, Register 0x3470

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SC_PKT_OK_ CNT	R/W	0x0	0x0	The number of packets received for this SC successfully validated and within the replay window.

Table 780: INPKTSSCOK1
Device 0x1F, Register 0x3474

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SC_PKT_OK_ CNT	R/W	0x0	0x0	The number of packets received for this SC successfully validated and within the replay window.

Table 781: INPKTSSCOK2
Device 0x1F, Register 0x3478

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SC_PKT_OK_ CNT	R/W	0x0	0x0	The number of packets received for this SC successfully validated and within the replay window.

Table 782: INPKTSSCOK3
Device 0x1F, Register 0x347C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_SC_PKT_OK_ CNT	R/W	0x0	0x0	The number of packets received for this SC successfully validated and within the replay window.

Table 783: INPKTSPARSEERR
Device 0x1F, Register 0x3480

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_PORT_PKT_PARSE_ERR_CNT	R/W	0x0	0x0	The number of packets that have a parse error as indicated by PEX per port.

Table 784: INPKTSFLOWIDTCAMMISS
Device 0x1F, Register 0x3484

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_PORT_PKT_FLOWID_TCAM_MISS_CNT	R/W	0x0	0x0	The number of Flow ID TCAM misses per port.

Table 785: INPKTSEARLYPREEMPTERR
Device 0x1F, Register 0x3488

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_PORT_PKT_EARLY_PREEMPT_ERR_CNT	R/W	0x0	0x0	The number of packets with Early Preemption violations detected per port.

Table 786: INPKTSFLOWIDTCAMHIT0
Device 0x1F, Register 0x348C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_FLOWID_PKT_FLOWID_TCAM_HIT_CNT	R/W	0x0	0x0	The number of Packets which hit an entry in the Flow-ID TCAM. Only 1 counter increments per packet.

Table 787: INPKTSFLOWIDTCAMHIT1
Device 0x1F, Register 0x3490

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_FLOWID_PKT_FLOWID_TCAM_HIT_CNT	R/W	0x0	0x0	The number of Packets which hit an entry in the Flow-ID TCAM. Only 1 counter increments per packet.

Table 788: INPKTSFLOWIDTCAMHIT2
Device 0x1F, Register 0x3494

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_FLOWID_PKT_FLOWID_TCAM_HIT_CNT	R/W	0x0	0x0	The number of Packets which hit an entry in the Flow-ID TCAM. Only 1 counter increments per packet.

Table 789: INPKTSFLOWIDTCAMHIT3
Device 0x1F, Register 0x3498

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	RX_FLOWID_PKT_FLOWID_TCAM_HIT_CNT	R/W	0x0	0x0	The number of Packets which hit an entry in the Flow-ID TCAM. Only 1 counter increments per packet.

Table 790: IFOUTCTLOCTETS0
Device 0x1F, Register 0x34A0

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_CTL_OCTET_CNT	R/W	0x0	0x0	Egress Total MSDU and MAC-DA/SA Octets that are permitted by the controlled port policies of this SecY.

Table 791: IFOUTCTLOCTETS1
Device 0x1F, Register 0x34A4

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_CTL_OCTET_CNT	R/W	0x0	0x0	Egress Total MSDU and MAC-DA/SA Octets that are permitted by the controlled port policies of this SecY.

Table 792: IFOUTCTLOCTETS2
Device 0x1F, Register 0x34A8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_CTL_OCTET_CNT	R/W	0x0	0x0	Egress Total MSDU and MAC-DA/SA Octets that are permitted by the controlled port policies of this SecY.

Table 793: IFOUTCTLOCTETS3
Device 0x1F, Register 0x34AC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_CTL_OCTET_CNT	R/W	0x0	0x0	Egress Total MSDU and MAC-DA/SA Octets that are permitted by the controlled port policies of this SecY.

Table 794: IFOUTCTLUCPKTS0
Device 0x1F, Register 0x34B0

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_CTL_PKT_UCAST_CNT	R/W	0x0	0x0	Egress Unicast packet count value for controlled ports of this SecY.

Table 795: IFOUTCTLUCPKTS1
Device 0x1F, Register 0x34B4

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_CTL_PKT_UCAST_CNT	R/W	0x0	0x0	Egress Unicast packet count value for controlled ports of this SecY.

Table 796: IFOUTCTLUCPKTS2
Device 0x1F, Register 0x34B8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_CTL_PKT_UCAST_CNT	R/W	0x0	0x0	Egress Unicast packet count value for controlled ports of this SecY.

Table 797: IFOUTCTLUCPKTS3
Device 0x1F, Register 0x34BC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_CTL_PKT_UCAST_CNT	R/W	0x0	0x0	Egress Unicast packet count value for controlled ports of this SecY.

Table 798: IFOUTCTLMCPKTS0
Device 0x1F, Register 0x34C0

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_CTL_PKT_ MCAST_CNT	R/W	0x0	0x0	Egress Multicast packet count value for controlled ports of this SecY.

Table 799: IFOUTCTLMCPKTS1
Device 0x1F, Register 0x34C4

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_CTL_PKT_ MCAST_CNT	R/W	0x0	0x0	Egress Multicast packet count value for controlled ports of this SecY.

Table 800: IFOUTCTLMCPKTS2
Device 0x1F, Register 0x34C8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_CTL_PKT_ MCAST_CNT	R/W	0x0	0x0	Egress Multicast packet count value for controlled ports of this SecY.

Table 801: IFOUTCTLMCPKTS3
Device 0x1F, Register 0x34CC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_CTL_PKT_ MCAST_CNT	R/W	0x0	0x0	Egress Multicast packet count value for controlled ports of this SecY.

Table 802: IFOUTCTLBCPKTS0
Device 0x1F, Register 0x34D0

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_CTL_PKT_ BCAST_CNT	R/W	0x0	0x0	Egress Broadcast packet count value for controlled ports of this SecY.

Table 803: IFOUTCTLBCPKTS1
Device 0x1F, Register 0x34D4

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_CTL_PKT_BCAST_CNT	R/W	0x0	0x0	Egress Broadcast packet count value for controlled ports of this SecY.

Table 804: IFOUTCTLBCPKTS2
Device 0x1F, Register 0x34D8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_CTL_PKT_BCAST_CNT	R/W	0x0	0x0	Egress Broadcast packet count value for controlled ports of this SecY.

Table 805: IFOUTCTLBCPKTS3
Device 0x1F, Register 0x34DC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_CTL_PKT_BCAST_CNT	R/W	0x0	0x0	Egress Broadcast packet count value for controlled ports of this SecY.

Table 806: IFOUTUNCTLOCTETS0
Device 0x1F, Register 0x34E0

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_UNCTL_OCTET_CNT	R/W	0x0	0x0	Egress Total MSDU and MAC-DA/SA Octets that are permitted by the uncontrolled port policies of this SecY.

Table 807: IFOUTUNCTLOCTETS1
Device 0x1F, Register 0x34E4

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_UNCTL_OCTET_CNT	R/W	0x0	0x0	Egress Total MSDU and MAC-DA/SA Octets that are permitted by the uncontrolled port policies of this SecY.

Table 808: IFOUTUNCTLOCTETS2
Device 0x1F, Register 0x34E8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_UNCTL_OCTET_CNT	R/W	0x0	0x0	Egress Total MSDU and MAC-DA/SA Octets that are permitted by the uncontrolled port policies of this SecY.

Table 809: IFOUTUNCTLOCTETS3
Device 0x1F, Register 0x34EC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_UNCTL_OCTET_CNT	R/W	0x0	0x0	Egress Total MSDU and MAC-DA/SA Octets that are permitted by the uncontrolled port policies of this SecY.

Table 810: IFOUTUNCTLUCPKTS0
Device 0x1F, Register 0x34F0

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_UNCTL_PKT_UCAST_CNT	R/W	0x0	0x0	Egress Unicast packet count value for uncontrolled ports of this SecY.

Table 811: IFOUTUNCTLUCPKTS1
Device 0x1F, Register 0x34F4

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_UNCTL_PKT_UCAST_CNT	R/W	0x0	0x0	Egress Unicast packet count value for uncontrolled ports of this SecY.

Table 812: IFOUTUNCTLUCPKTS2
Device 0x1F, Register 0x34F8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_UNCTL_PKT_UCAST_CNT	R/W	0x0	0x0	Egress Unicast packet count value for uncontrolled ports of this SecY.

Table 813: IFOUTUNCTLUCPKTS3
Device 0x1F, Register 0x34FC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_UNCTL_PKT_UCAST_CNT	R/W	0x0	0x0	Egress Unicast packet count value for uncontrolled ports of this SecY.

Table 814: IFOUTUNCTLMCPKTS0
Device 0x1F, Register 0x3500

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_UNCTL_PKT_MCAST_CNT	R/W	0x0	0x0	Egress Multicast packet count value for uncontrolled ports of this SecY.

Table 815: IFOUTUNCTLMCPKTS1
Device 0x1F, Register 0x3504

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_UNCTL_PKT_MCAST_CNT	R/W	0x0	0x0	Egress Multicast packet count value for uncontrolled ports of this SecY.

Table 816: IFOUTUNCTLMCPKTS2
Device 0x1F, Register 0x3508

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_UNCTL_PKT_MCAST_CNT	R/W	0x0	0x0	Egress Multicast packet count value for uncontrolled ports of this SecY.

Table 817: IFOUTUNCTLMCPKTS3
Device 0x1F, Register 0x350C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_UNCTL_PKT_MCAST_CNT	R/W	0x0	0x0	Egress Multicast packet count value for uncontrolled ports of this SecY.

Table 818: IFOUTUNCTLBCPKTS0
Device 0x1F, Register 0x3510

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_UNCTL_PKT_BCAST_CNT	R/W	0x0	0x0	Egress Broadcast packet count value for uncontrolled ports of this SecY.

Table 819: IFOUTUNCTLBCPKTS1
Device 0x1F, Register 0x3514

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_UNCTL_PKT_BCAST_CNT	R/W	0x0	0x0	Egress Broadcast packet count value for uncontrolled ports of this SecY.

Table 820: IFOUTUNCTLBCPKTS2
Device 0x1F, Register 0x3518

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_UNCTL_PKT_BCAST_CNT	R/W	0x0	0x0	Egress Broadcast packet count value for uncontrolled ports of this SecY.

Table 821: IFOUTUNCTLBCPKTS3
Device 0x1F, Register 0x351C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_UNCTL_PKT_BCAST_CNT	R/W	0x0	0x0	Egress Broadcast packet count value for uncontrolled ports of this SecY.

Table 822: OUTPKTSCTRLPORTDISABLED0
Device 0x1F, Register 0x3520

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SECY_PKT_CTRL_PORT_DISABLED_CNT	R/W	0x0	0x0	The number of packets received on disabled SecY.

Table 823: OUTPKTSCTRLPORTDISABLED1
Device 0x1F, Register 0x3524

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SECY_PKT_CTRL_PORT_DISABLED_CNT	R/W	0x0	0x0	The number of packets received on disabled SecY.

Table 824: OUTPKTSCTRLPORTDISABLED2
Device 0x1F, Register 0x3528

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SECY_PKT_CTRL_PORT_DISABLED_CNT	R/W	0x0	0x0	The number of packets received on disabled SecY.

Table 825: OUTPKTSCTRLPORTDISABLED3
Device 0x1F, Register 0x352C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SECY_PKT_CTRL_PORT_DISABLED_CNT	R/W	0x0	0x0	The number of packets received on disabled SecY.

Table 826: OUTPKTSSECYUNTAGGED0
Device 0x1F, Register 0x3530

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SECY_PKT_UNTAGGED_CNT	R/W	0x0	0x0	The number of data packets (excluding control packets) transmitted without a SecTag because Protect Frames is false.

Table 827: OUTPKTSSECYUNTAGGED1
Device 0x1F, Register 0x3534

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SECY_PKT_UNTAGGED_CNT	R/W	0x0	0x0	The number of data packets (excluding control packets) transmitted without a SecTag because Protect Frames is false.

Table 828: OUTPKTSSECYUNTAGGED2
Device 0x1F, Register 0x3538

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SECY_PKT_ UNTAGGED_CNT	R/W	0x0	0x0	The number of data packets (excluding control packets) transmitted without a SecTag because Protect Frames is false.

Table 829: OUTPKTSSECYUNTAGGED3
Device 0x1F, Register 0x353C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SECY_PKT_ UNTAGGED_CNT	R/W	0x0	0x0	The number of data packets (excluding control packets) transmitted without a SecTag because Protect Frames is false.

Table 830: OUTPKTSSECYNOACTIVESA0
Device 0x1F, Register 0x3540

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SECY_PKT_ NOACTIVESA_CNT	R/W	0x0	0x0	The number of data packets with SA value not matching any active SA value configured.

Table 831: OUTPKTSSECYNOACTIVESA1
Device 0x1F, Register 0x3544

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SECY_PKT_ NOACTIVESA_CNT	R/W	0x0	0x0	The number of data packets with SA value not matching any active SA value configured.

Table 832: OUTPKTSSECYNOACTIVESA2
Device 0x1F, Register 0x3548

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SECY_PKT_ NOACTIVESA_CNT	R/W	0x0	0x0	The number of data packets with SA value not matching any active SA value configured.

Table 833: OUTPKTSSECYNOACTIVESA3
Device 0x1F, Register 0x354C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SECY_PKT_ NOACTIVESA_CNT	R/W	0x0	0x0	The number of data packets with SA value not matching any active SA value configured.

Table 834: OUTPKTSSECYTOOLONG0
Device 0x1F, Register 0x3550

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SECY_PKT_ TOOLONG_CNT	R/W	0x0	0x0	The number of transmit packets discarded because their length is greater than the configured MTU after SecTag/ICV insertion.

Table 835: OUTPKTSSECYTOOLONG1
Device 0x1F, Register 0x3554

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SECY_PKT_ TOOLONG_CNT	R/W	0x0	0x0	The number of transmit packets discarded because their length is greater than the configured MTU after SecTag/ICV insertion.

Table 836: OUTPKTSSECYTOOLONG2
Device 0x1F, Register 0x3558

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SECY_PKT_ TOOLONG_CNT	R/W	0x0	0x0	The number of transmit packets discarded because their length is greater than the configured MTU after SecTag/ICV insertion.

Table 837: OUTPKTSSECYTOOLONG3
Device 0x1F, Register 0x355C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SECY_PKT_ TOOLONG_CNT	R/W	0x0	0x0	The number of transmit packets discarded because their length is greater than the configured MTU after SecTag/ICV insertion.

Table 838: OUTOCTETSSECYPROTECTED0
Device 0x1F, Register 0x3560

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SECY_OCTET_PROTECTED_CNT	R/W	0x0	0x0	The number of plain text octets integrity protected, but not encrypted in transmitted frames.

Table 839: OUTOCTETSSECYPROTECTED1
Device 0x1F, Register 0x3564

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SECY_OCTET_PROTECTED_CNT	R/W	0x0	0x0	The number of plain text octets integrity protected, but not encrypted in transmitted frames.

Table 840: OUTOCTETSSECYPROTECTED2
Device 0x1F, Register 0x3568

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SECY_OCTET_PROTECTED_CNT	R/W	0x0	0x0	The number of plain text octets integrity protected, but not encrypted in transmitted frames.

Table 841: OUTOCTETSSECYPROTECTED3
Device 0x1F, Register 0x356C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SECY_OCTET_PROTECTED_CNT	R/W	0x0	0x0	The number of plain text octets integrity protected, but not encrypted in transmitted frames.

Table 842: OUTOCTETSSECYENCRYPTED0
Device 0x1F, Register 0x3570

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SECY_OCTET_ENCRYPTED_CNT	R/W	0x0	0x0	The number of plain text octets integrity protected and encrypted in transmitted frames.

Table 843: OUTOCTETSSECYENCRYPTED1
Device 0x1F, Register 0x3574

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SECY_OCTET_ENCRYPTED_CNT	R/W	0x0	0x0	The number of plain text octets integrity protected and encrypted in transmitted frames.

Table 844: OUTOCTETSSECYENCRYPTED2
Device 0x1F, Register 0x3578

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SECY_OCTET_ENCRYPTED_CNT	R/W	0x0	0x0	The number of plain text octets integrity protected and encrypted in transmitted frames.

Table 845: OUTOCTETSSECYENCRYPTED3
Device 0x1F, Register 0x357C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SECY_OCTET_ENCRYPTED_CNT	R/W	0x0	0x0	The number of plain text octets integrity protected and encrypted in transmitted frames.

Table 846: OUTPKTSSCPROTECTED0
Device 0x1F, Register 0x3580

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SC_PKT_PROTECTED_CNT	R/W	0x0	0x0	The number of integrity protected, but not encrypted packets for this transmit SC.

Table 847: OUTPKTSSCPROTECTED1
Device 0x1F, Register 0x3584

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SC_PKT_PROTECTED_CNT	R/W	0x0	0x0	The number of integrity protected, but not encrypted packets for this transmit SC.

Table 848: OUTPKTSSCPROTECTED2
Device 0x1F, Register 0x3588

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SC_PKT_PRO-TECTED_CNT	R/W	0x0	0x0	The number of integrity protected, but not encrypted packets for this transmit SC.

Table 849: OUTPKTSSCPROTECTED3
Device 0x1F, Register 0x358C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SC_PKT_PRO-TECTED_CNT	R/W	0x0	0x0	The number of integrity protected, but not encrypted packets for this transmit SC.

Table 850: OUTPKTSSCENCRYPTED0
Device 0x1F, Register 0x3590

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SC_PKT_ ENCRYPTED_CNT	R/W	0x0	0x0	The number of integrity protected and encrypted packets for this transmit SC.

Table 851: OUTPKTSSCENCRYPTED1
Device 0x1F, Register 0x3594

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SC_PKT_ ENCRYPTED_CNT	R/W	0x0	0x0	The number of integrity protected and encrypted packets for this transmit SC.

Table 852: OUTPKTSSCENCRYPTED2
Device 0x1F, Register 0x3598

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SC_PKT_ ENCRYPTED_CNT	R/W	0x0	0x0	The number of integrity protected and encrypted packets for this transmit SC.

Table 853: OUTPKTSSCENCRYPTED3
Device 0x1F, Register 0x359C

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_SC_PKT_ ENCRYPTED_CNT	R/W	0x0	0x0	The number of integrity protected and encrypted packets for this transmit SC.

Table 854: OUTPKTSPARSEERR
Device 0x1F, Register 0x35A0

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_PORT_PKT_ PARSE_ERR_CNT	R/W	0x0	0x0	The number of packets that have a parse error as indicated by PEX per port.

Table 855: OUTPKTSFLOWIDTCAMMISS
Device 0x1F, Register 0x35A4

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_PORT_PKT_ FLOWID_TCAM_ MISS_CNT	R/W	0x0	0x0	The number of Flow ID TCAM misses per port.

Table 856: OUTPKTSEARLYPREEMPTERR
Device 0x1F, Register 0x35A8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_PORT_PKT_EAR-LY_PREEMPT_ERR_ CNT	R/W	0x0	0x0	The number of packets with Early Preemption violations detected per port.

Table 857: OUTPKTSFLOWIDTCAMHIT0
Device 0x1F, Register 0x35AC

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_FLOWID_PKT_ FLOWID_TCAM_HIT_ CNT	R/W	0x0	0x0	The number of Flow ID TCAM hits per flow id entry.

Table 858: OUTPKTSFLOWIDTCAMHIT1
Device 0x1F, Register 0x35B0

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_FLOWID_PKT_FLOWID_TCAM_HIT_CNT	R/W	0x0	0x0	The number of Flow ID TCAM hits per flow id entry.

Table 859: OUTPKTSFLOWIDTCAMHIT2
Device 0x1F, Register 0x35B4

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_FLOWID_PKT_FLOWID_TCAM_HIT_CNT	R/W	0x0	0x0	The number of Flow ID TCAM hits per flow id entry.

Table 860: OUTPKTSFLOWIDTCAMHIT3
Device 0x1F, Register 0x35B8

Bits	Field	Mode	HW Rst	SW Rst	Description
47:0	TX_FLOWID_PKT_FLOWID_TCAM_HIT_CNT	R/W	0x0	0x0	The number of Flow ID TCAM hits per flow ID entry.

Table 861: MPTP_CFG
Device 0x1F, Register 0xA008

Bits	Field	Mode	HW Rst	SW Rst	Description
15	CSR_SYNC_LINK	rw	0x0	0x0	Set to force ptp sync_link input to be 1. Otherwise, sync_link is
14	UNUSED_14	ro	0x0	0x0	UNUSED
13	MCS_MPLS_DIS	rw	0x1	0x1	Drives msc_mpls_disable input
12	MCS_VLAN_DIS	rw	0x0	0x0	Drives MMAC mcs_vlan_disable input
11	TUNO_EEE_CAP	rw	0x1	0x1	Drives MMAC tuno_eee_capable_a input
10	CUNO_HOLD_LPI	rw	0x0	0x0	Drives MMAC cuno_hold_lpi_s input.
9	MMAC_MEM_PWDN	rw	0x0	0x0	Set to power down MMAC internal memory
8	PTP_EXT_IGR_SFD	rw	0x0	0x0	Set to select external Rx sfd to drive ptp ptp_rxframe pin.
7	PTP_EXT_EGR_SFD	rw	0x0	0x0	Set to select external Tx sfd to drive ptp ptp_txframe pin.
6	MMAC_DISABLE	rw	0x1	0x1	When MMAC_DISABLE_OW is set, this bit defines mmac to be disabled

Table 861: MPTP_CFG (Continued)
Device 0x1F, Register 0xA008

Bits	Field	Mode	HW Rst	SW Rst	Description
5	MMAC_DISABLE_OW	rw	0x1	0x1	Set 1 to override mmac_disable input from EFUSE read-out.
4	MMAC_LOW_ LATENCY	rw	0x0	0x0	This bit defines mmac_low_latency input to mmac.
3	PTP_CLK_EN	rw	0x0	0x0	Set 1 to enable PTP clocks.
2	MMAC_CORE_CLK-SEL	rw	0x0	0x0	0: use recovered clk, same as mac clk. 1: use reference clk, asynchronous
1:0	MPTP_SEL	rw	0x00	0x00	mmac_ptp_sel[1:0]: 00 -- bypass mmac, bypass ptp 01 -- bypass

Table 862: MPTP_RSTN
Device 0x1F, Register 0xA00A

Bits	Field	Mode	HW Rst	SW Rst	Description
15:14	UNUSED_15_14	ro	0x0	0x0	UNUSED
13	EN_SELF_RST_ TRAFFIC_STUCK	rw	0x0	0x0	Set 1 to enable MMAC self-reset if MMAC traffic is stuck
12	EN_SELF_RST_DP_ BUF_FULL	rw	0x0	0x0	Set 1 to enable MMAC self-reset if any buffer in MMAC datapath is full.
11	MMAC_EXT_SRST_ DIS	rw	0x0	0x0	Set 1 to disable external soft reset to MMAC.
10	PTP_EXT_SRST_DIS	rw	0x0	0x0	Set 1 to disable external soft reset to PTP.
9	MMAC_SRESETN	rw	0x1	0x1	Active low mmac soft reset
8	PTP_SRESETN	rw	0x1	0x1	active low all PTP soft resets
7:6	UNUSED_7_6	rw	0x1	0x1	UNUSED
5	PTP_TS_HS_RSTN	rw	0x1	0x1	Active low ptp TAI hard&soft reset
4	PTP_TS_H_RSTN	rw	0x1	0x1	Active low ptp TAI hard reset
3	PTP_TX_HS_RSTN	rw	0x1	0x1	Active low ptp tx path hard&soft reset
2	PTP_RX_HS_RSTN	rw	0x1	0x1	Active low ptp rx path hard&soft reset
1	PTP_SYS_HS_RSTN	rw	0x1	0x1	Active low ptp sysclk hard&soft reset
0	PTP_SYS_H_RSTN	rw	0x1	0x1	Active low ptp sysclk hard reset

4 Electrical Specifications

4.1 Absolute Maximum Ratings

Table 863: Absolute Maximum Ratings

Stresses above those listed in Absolute Maximum Ratings may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Symbol	Parameter	Min	Typ	Max	Unit
V_{DDA}	Power Supply Voltage on AVDDL with respect to VSS	-0.40	–	1.32	V
V_{DDAR}	Power Supply Voltage on AVDD33 with respect to VSS	-0.40	–	3.63	V
V_{REG_IN}	Power Supply Voltage on REG_IN (VDD33) with respect to VSS	-0.40	–	3.63	V
V_{DD}	Power Supply Voltage on DVDD with respect to VSS	-0.40	–	0.88	V
V_{DDO}	Power Supply Voltage on VDDO with respect to VSS (@1.8V)	–	–	1.98	V
V_{DDO}	Power Supply Voltage on VDDO with respect to VSS (@2.5V)	–	–	2.75	V
V_{DDO}	Power Supply Voltage on VDDO with respect to VSS (@3.3V)	–	–	3.63	V
V_{PIN}	Voltage Applied to Any Digital Input Pin	–	–	3.63 or VDDO+0.4, whichever is less	V
T_J	Junction Temperature	–	–	150	^oC

4.2 Recommended Operating Conditions

Table 864: Recommended Operating Conditions

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}[1, 2]	AVDDL Supply	For AVDDL	1.14	1.2	1.26	V
V_{DDAR}[1]	AVDD33 Supply	For AVDD33	3.135	3.3	3.465	V
V_{DD}[1, 2]	DVDD Supply	DVDD for Rev B0/B1	0.7125	0.75	0.7875	V
		DVDD for Rev B2 (without TC10)	0.7125	0.80	0.84	V
		DVDD for Rev B2 (with TC10)	0.76	0.80	0.84	V
V_{DDO}[1]	VDDO Supply	For VDDO at 1.8V	1.71	1.8	1.89	V
		For VDDO at 2.5V	2.375	2.5	2.625	V
		For VDDO at 3.3V	3.135	3.3	3.465	V
RSET	Internal Bias Reference	Resistor connected to V_{SS}	–	4990 ±1% Tolerance	–	
T_A	Ambient Operating Temperature	AEC-Q100 Grade 1	-40	–	125	°C
T_A	Ambient Operating Temperature	AEC-Q100 Grade 2	-40	–	105	°C
T_J	Junction Temperature[3, 4]		-40	–	140	°C

1. Maximum noise allowed on supplies is 50 mV peak-peak.
2. The recommended operating conditions mentioned here for AVDDL and DVDD are applicable only when using external supplies. They are not applicable when using internal regulators.
3. Operation beyond 125°C for extended periods of time may impact long-term reliability. Care should be taken to ensure that the maximum junction temperature of 140°C is not exceeded in the system design. Thermal mitigation measures should be taken if necessary.
4. Electrical parameters and power consumption are characterized over this junction temperature range.

4.3 Package Thermal Information

Table 865: Thermal Conditions for BRIGHTLANE™ 88Q2220/88Q2220M/88Q2221/88Q2221M/88Q1200M/88Q1201M 40-pin QFN Package

Symbol	Parameter[1]	Condition	Min	Typ	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance $\theta_{JA} = (T_J - T_A)/P$ P = Total Power Dissipation	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow	–	40.49	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow	–	37.43	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow	–	36.48	–	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance $\theta_{JB} = (T_J - T_B)/P_{bottom}$ P_{bottom} = Power Dissipation from the Bottom of the Package to the PCB Surface	JEDEC with no air flow	–	25.63	–	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance $\theta_{JC} = (T_J - T_C)/P_{top}$ P_{top} = Power Dissipation from the Top of the Package	JEDEC with no air flow	–	19.02	–	°C/W
ψ_{JB}	Junction-to-Board Thermal Characterization Parameter $\psi_{JB} = (T_J - T_{bottom})/P$ P = Total Power Dissipation T_{bottom} = Temperature on the Bottom of the Package	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow	–	25.62	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow	–	25.54	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow	–	25.47	–	°C/W
ψ_{JT}	Junction-to-Top-Center Thermal Characterization Parameter $\psi_{JT} = (T_J - T_{top})/P$ P = Total Power Dissipation T_{top} = Temperature on the Top Center of the Package	JEDEC 3 in. x 4.5 in. 4-layer PCB with no air flow	–	1.04	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 1 meter/sec air flow	–	1.31	–	°C/W
		JEDEC 3 in. x 4.5 in. 4-layer PCB with 2 meter/sec air flow	–	1.51	–	°C/W

1. Refer to the white paper on T_J Thermal Calculations for detailed information.

4.4 Current Consumption

4.4.1 Current Consumption when Using External Regulators

Note

Table 866, Table 867, Table 868, and Table 869 provide electrical data for the Max setting of fast corner devices at 140°C temperature and supply for DVDD running at 12% above 0.75V[1], and 5% above nominal values for rest of supplies. The Typical setting is for typical devices at room temperature of 25°C with external supplies at nominal values. The data was extracted from devices running with an external power supply.

4.4.1.1 Current Consumption AVDDL

Table 866: Current Consumption AVDDL

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition		Min	Typ	Max	Unit
I_{AVDD}	1.2V Power to Analog Core	AVDDL	RGMII with traffic	1000BASE-T1	–	71	84	mA
			RGMII with traffic	100BASE-T1	–	53	62	mA
			SGMII with traffic	1000BASE-T1	–	84	106	mA
			SGMII with traffic	100BASE-T1	–	68	83	mA
			RGMII with MACsec traffic	1000BASE-T1	–	76	90	mA
			RGMII with MACsec traffic	100BASE-T1	–	54	63	mA
			SGMII with MACsec traffic	1000BASE-T1	–	90	111	mA
			SGMII with MACsec traffic	100BASE-T1	–	69	85	mA

1. 0.75V applies for Rev B0/B1. 0.80V applies for Rev B2.

4.4.1.2 Current Consumption AVDD33

Table 867: Current Consumption AVDD33
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition		Min	Typ	Max	Unit
I_{AVDDR}	Analog 3.3V Supply	AVDD33	RGMII with traffic	1000BASE-T1	–	14	15	mA
			RGMII with traffic	100BASE-T1	–	17	20	mA
			SGMII with traffic	1000BASE-T1	–	14	15	mA
			SGMII with traffic	100BASE-T1	–	17	20	mA
			RGMII with MACsec traffic	1000BASE-T1	–	16	18	mA
			RGMII with MACsec traffic	100BASE-T1	–	18	21	mA
			SGMII with MACsec traffic	1000BASE-T1	–	16	17	mA
			SGMII with MACsec traffic	100BASE-T1	–	17	21	mA

4.4.1.3 Current Consumption DVDD

Table 868: Current Consumption DVDD
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition		Min	Typ	Max	Unit
I_{VDD}	0.75V[1] Power to Digital Core	DVDD	RGMII with traffic	1000BASE-T1	–	83	199	mA
			RGMII with traffic	100BASE-T1	–	47	158	mA
			SGMII with traffic	1000BASE-T1	–	87	193	mA
			SGMII with traffic	100BASE-T1	–	51	147	mA
			RGMII with MACsec traffic	1000BASE-T1	–	131	266	mA
			RGMII with MACsec traffic	100BASE-T1	–	55	172	mA
			SGMII with MACsec traffic	1000BASE-T1	–	135	252	mA
			SGMII with MACsec traffic	100BASE-T1	–	59	160	mA

1. 0.75V applies for Rev B0/B1. 0.80V applies for Rev B2.

4.4.1.4 Current Consumption VDDO

Table 869: Current Consumption VDDO

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Pins	Condition			Min	Typ	Max	Unit
I_{VDDO}	Power to the Digital I/Os	VDDO	RGMII with traffic	1000BASE-T1	VDDO = 3.3V	–	30	32	mA
					VDDO = 2.5V	–	23	25	mA
					VDDO = 1.8V	–	14	17	mA
			RGMII with traffic	100BASE-T1	VDDO = 3.3V	–	14	14	mA
					VDDO = 2.5V	–	10	10	mA
					VDDO = 1.8V	–	5	6	mA
			SGMII with traffic	1000BASE-T1	VDDO = 3.3V	–	3	4	mA
					VDDO = 2.5V	–	2	3	mA
					VDDO = 1.8V	–	1	2	mA
			SGMII with traffic	100BASE-T1	VDDO = 3.3V	–	3	4	mA
					VDDO = 2.5V	–	2	3	mA
					VDDO = 1.8V	–	1	2	mA
			RGMII with MACsec traffic	1000BASE-T1	VDDO = 3.3V	–	30	32	mA
					VDDO = 2.5V	–	23	25	mA
					VDDO = 1.8V	–	14	17	mA
			RGMII with MACsec traffic	100BASE-T1	VDDO = 3.3V	–	14	14	mA
					VDDO = 2.5V	–	10	10	mA
					VDDO = 1.8V	–	5	6	mA
			SGMII with MACsec traffic	1000BASE-T1	VDDO = 3.3V	–	3	4	mA
					VDDO = 2.5V	–	2	3	mA
					VDDO = 1.8V	–	1	2	mA
			SGMII with MACsec traffic	100BASE-T1	VDDO = 3.3V	–	3	4	mA
					VDDO = 2.5V	–	2	3	mA
					VDDO = 1.8V	–	1	2	mA

4.5 ESD Ratings

Table 870: ESD Ratings

Parameter	I/O Pins	Value	Unit
Human Body Model (HBM)[1]	MDI pins	+/-6	kV
	WAKE_IN pins	+/-5	kV
	All other pins	+/-2	kV
Charged Device Model (CDM)[2]	Corner pins	+/-750	V
	All other pins	+/-500	V

1. Reference Standard - AEC-Q100, AEC-Q100-002.
2. Reference Standard - AEC-Q100, AEC-Q100-011.

4.6 DC Operating Conditions

4.6.1 Digital Pin Grouping

Table 871: Digital Pin Grouping

Group	Operating Conditions	Pin Name
Group 1 RGMII Input/Output	1.8V/2.5V/3.3V	RXD[3:0], RXC, RCLK
Group 2 RGMI Input	1.8V/2.5V/3.3V	TXD[3:0],TXD,TCLK
Group 3 MISC Input/Output	1.8V/2.5V/3.3V	INTN, GPIO, MDIO
Group 4 MISC Input	1.8V/2.5V/3.3V	RESETN
Group 5 High Speed Input/Output	1.8V/2.5V/3.3V	TX_ENABLE

4.6.2 Digital Pin Operating Conditions

Table 872: Digital Pin Operating Conditions

Symbol	Parameter	Pins	Voltage Rail	Min	Typ	Max	Unit
VDDO	Power Supply Voltage	All Pins	3.3	3.135	3.3	3.465	V
			2.5	2.375	2.5	2.625	V
			1.8	1.71	1.8	1.89	V
VIL	Input Low Voltage	Group 1, 2	3.3	-0.3		0.8	V
			2.5	-0.3	-	VDDO*30%	V
			1.8	-0.3	-	VDDO*30%	V
		Group 3, 4, 5	3.3	-0.3	-	VDDO*30%	V
			2.5	-0.3	-	VDDO*30%	V
			1.8	-0.3	-	VDDO*30%	V
VIH	Input High Voltage	Group 1, 2, 3, 4, 5	3.3	VDDO*70%			V
			2.5	VDDO*70%	-	-	V
			1.8	VDDO*70%	-	-	V
VHYS	Voltage Hysteresis	All Pins	-	150	-	-	mV

Table 872: Digital Pin Operating Conditions (Continued)

Symbol	Parameter	Pins	Voltage Rail	Min	Typ	Max	Unit
VOL	Output Low Voltage	Group 1	3.3V (I_{OL} = 6.8 mA)	-	-	0.4	V
			2.5V (I_{OL} = 6.8 mA)	-	-	0.4	V
			1.8V (I_{OL} = 6.4 mA)	-	-	0.4	V
		Group 3	3.3V (I_{OL} = 6.8 mA)	-	-	0.4	V
			2.5V (I_{OL} = 6.8 mA)	-	-	0.4	V
			1.8V (I_{OL} = 6.8 mA)	-	-	0.4	V
		Group 5	3.3V (I_{OL} = 8 mA)	-	-	0.4	V
			2.5V (I_{OL} = 8 mA)	-	-	0.4	V
			1.8V (I_{OL} = 8 mA)	-	-	0.4	V
VOH	Output High Voltage	Group 1	3.3V (I_{OH} = 6.8 mA)	VDDO-0.4	-	-	V
			2.5V (I_{OH} = 6.8 mA)	VDDO-0.4	-	-	V
			1.8V (I_{OH} = 6.4 mA)	VDDO-0.4	-	-	V
		Group 3	3.3V (I_{OH} = 6.8 mA)	VDDO-0.4	-	-	V
			2.5V (I_{OH} = 6.8 mA)	VDDO-0.4	-	-	V
			1.8V (I_{OH} = 6.8 mA)	VDDO-0.4	-	-	V
		Group 5	3.3V (I_{OH} = 8 mA)	VDDO-0.4	-	-	V
			2.5V (I_{OH} = 8 mA)	VDDO-0.4	-	-	V
			1.8V (I_{OH} = 8 mA)	VDDO-0.4	-	-	V

Table 872: Digital Pin Operating Conditions (Continued)

Symbol	Parameter	Pins	Voltage Rail	Min	Typ	Max	Unit
IILK	Input Leakage Current	Group 1, 2, 3, 4 w/ pull-up resistor	0 < Vin < VDDO	-	-	+10 -90	µA
		Group 1, 2, 3, 4 w/ pull-down resistor		-	-	90 -10	µA
		Group 5 w/pull-up resistor		-	-	+20 -90	µA
		Group 5 w/pull-down resistor		-	-	+90 -20	µA
		Group 1, 2, 3, 4		-	-	+10 -10	µA
		Group 5		-	-	+20 -20	µA
CIN	Input Capacitance	XTAL_I N	-	-	5	-	pF
		Group 1, 2, 3, 4		-	-	5	pF
		Group 5		-	-	10	pF

4.7 Internal Resistors

These values are based on pad specifications.

Table 873: Internal Resistors

Symbol	Parameter	Min	Typ	Max	Unit
$R_{Pull-Up}$	Pull-Up Resistance	40	–	100	k
$R_{Pull-Down}$	Pull-Down Resistance	40	–	100	k

4.7.1 IEEE Transceiver Parameters

IEEE tests are typically based on templates and cannot simply be specified by a number. For an exact description of the template and the test conditions, refer to the IEEE specifications:

- 1000BASE-T1

Table 874: PMA Electrical Specifications (IEEE Std 802bp-2016)

Tests	Min	Max	Unit
Maximum Output Droop Negative	–	10	%

Table 874: PMA Electrical Specifications (IEEE Std 802bp-2016) (Continued)

Tests	Min	Max	Unit
Transmitter Distortion	–	15	mV
Transmitter Timing Jitter Master	–	RMS <5, Peak-to-Peak <50	ps
Transmitter Timing Jitter Slave	–	RMS <10, Peak-to-Peak <100	ps
Transmitter Timing Jitter MDI	–	RMS <5, Peak-to-Peak <50	ps
Transmit Power Level	–	5	dBm
Transmitter Power Spectral Density	Fit template		
Transmitter Peak Differential Output	–	1.3	V peak-peak
Transmitter Clock Frequency	–	±100	ppm

4.7.2 SGMII Interface

SGMII specification is a de-facto standard proposed by Cisco. It is available at the Cisco website (ftp://ftp-eng.cisco/smii/sgmii.pdf). It uses a modified LVDS specification based on the IEEE standard 1596.3: refer to that standard for the exact definition of the terminology used in Table 875. The device adds flexibility by allowing programmable output voltage swing and supply voltage option.

4.7.2.1 Transmitter DC Characteristics

Table 875: Transmitter DC Characteristics
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

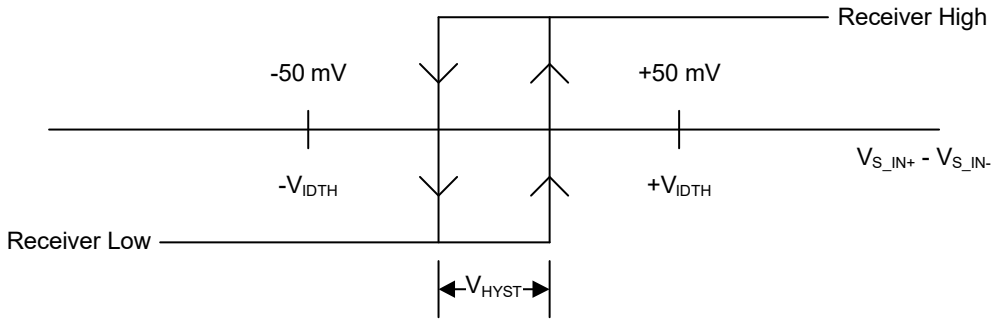
Symbol	Parameter	Min	Typ	Max	Unit
VOH	Output Voltage High	–	–	350	mV
VOL	Output Voltage Low	40	–	–	mV
VRING	Output Ringing	–	–	10	%
|VOD|	Output Voltage Swing (differential peak)	150	–	400	mV peak
VOS	Output Offset Voltage (also called Common Mode Voltage)	100	–	200	mV
RO	Output Impedance (Single-ended) (50Ω Termination)	40	–	60	Ω
Delta R_O	Mismatch in a Pair	–	–	10	%
Delta V_{OD}	Change in V_{OD} between 0 and 1	–	–	25	mV
Delta V_{OS}	Change in V_{OS} between 0 and 1	–	–	25	mV
IS+, IS-	Output Current on Short to VSS	–	–	40	mA
IS+-	Output Current when S_OUT+ and S_OUT- are Shorted	–	–	12	mA
IX+, IX-	Power Off Leakage Current	–	–	10	mA

4.7.2.2 Receiver DC Characteristics

Table 876: Receiver DC Characteristics
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
V_{IDTH}	Input Differential Threshold	-50	–	50	mV
V_{HYST}	Input Differential Hysteresis	25	–	–	mV
R_{IN}	Receiver 100Ω Differential Input Impedance	80	–	120	Ω

Figure 42: Input Differential Hysteresis



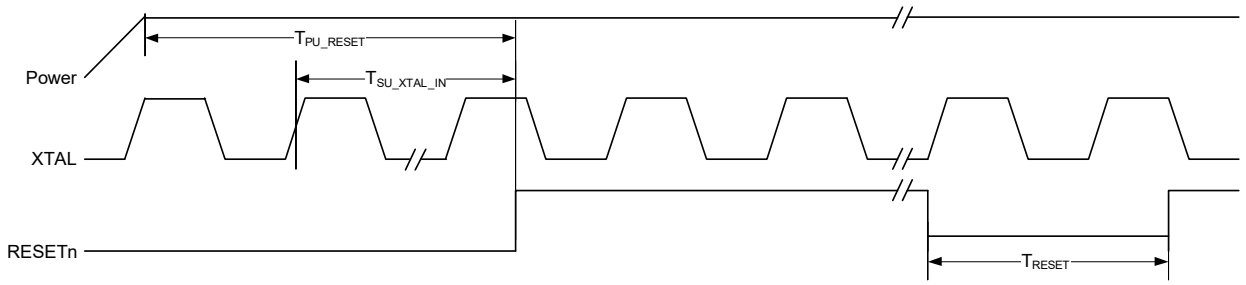
4.8 AC Electrical Specifications

4.8.1 Reset Timing

Table 877: Reset Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified.)

Symbol	Parameter	Min	Typ	Max	Unit
T_{PU_RESET}	Valid Power to RESETn De-asserted	1	–	–	ms
$T_{SU\_XTAL\_IN}$	Number of Valid XTAL_IN Cycles Prior to RESETn De-asserted	10	–	–	clocks
T_{RESET}	Minimum Reset Pulse Width during Normal Operation	1	–	–	ms
T_{RESET_MDIO}	Minimum Wait Time from RESET De-assertion to First MDIO Access	1	–	–	ms

Figure 43: Reset Timing



4.8.2 XTAL_IN/XTAL_OUT Timing

Table 878: 25 MHz Oscillator Requirements
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_T	Target Frequency	–	–	25.0	–	MHz
	Frequency Tolerance	–	-100	–	+100	ppm
$T_{P\_XTAL\_IN}$	XTAL_IN Period	–	–	40	–	ns
$V_{SWING\_XTAL\_IN}$	XTAL_IN Swing	See the *Oscillator Shifting Application Note* (MV-S301630-00). (Note: Must be AC coupled with a 0.1 nF capacitor.)	0.8	–	1.8	Vpp
$T_{H\_XTAL\_IN}$	XTAL_IN High Time	–	13	20	27	ns
$T_{L\_XTAL\_IN}$	XTAL_IN Low Time	–	13	20	27	ns
$T_{R\_XTAL\_IN}$	XTAL_IN Rise Time	10 to 90%	–	3.0	5.0	ns

Table 878: 25 MHz Oscillator Requirements (Continued)

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$T_{F\_XTAL\_IN}$	XTAL_IN Fall Time	10 to 90%	–	3.0	–	ns
$T_{J\_XTAL\_IN}$	XTAL_IN Total Jitter[1]	12 kHz to 20 MHz	–	–	1.0 (SGMII)	ps RMS
					4.0 (RGMII)	
$C_{J\_XTAL\_OUT}$	Capacitor value from XTAL_OUT to ground	Ceramic	–	0.1	–	µF

1. PLL-generated clocks are not recommended as input to XTAL_IN since they can have excessive jitter. Zero delay buffers are also not recommended for the same reason.

Figure 44: XTAL_IN/XTAL_OUT Timing

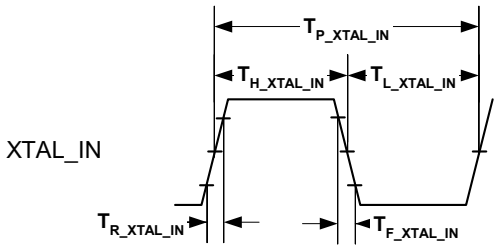


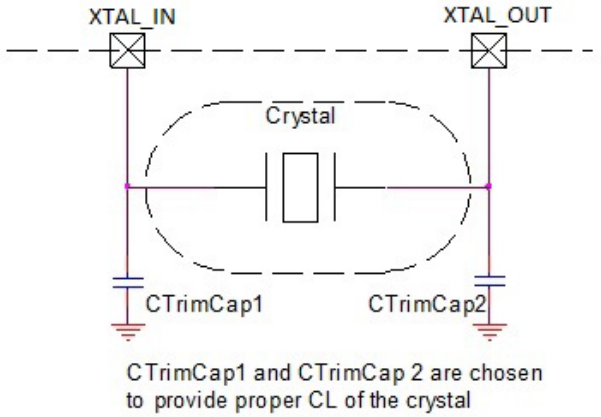
Table 879: 25 MHz Crystal Requirements[1]

(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
F_T	Target Frequency	–	–	25.0	–	MHz
	Frequency Tolerance	–	-100	–	100	ppm
C_L	Load Capacitance	User Specified	–	6	12	pF
C_S	Shunt Capacitance	–	–	–	CL/6	pF
RL or ESR	Equivalent Series Resistance	–	–	100	150	Ω
D_L	Drive Level	–	100	–	–	µW

1. See *How to Use Crystals as Clock Sources Application Note* (MV-S300626-00) for details.

Figure 45: Crystal Reference Schematic

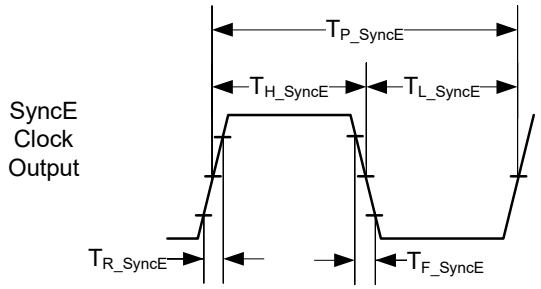


4.8.3 SyncE Recovered Clock Output Timing

Table 880: SyncE Recovered Clock Output Timing

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{P_SyncE}	Period	125 MHz	–	8.0002	–	ns
T_{H_SyncE}	High Time	125 MHz	–	3.0833	–	ns
T_{L_SyncE}	Low Time	125 MHz	–	3.6349	–	ns
T_{R_SyncE}	Rise Time	125 MHz	–	0.472	–	ns
T_{F_SyncE}	Fall Time	125 MHz	–	0.445	–	ns
T	Duty Cycle	125 MHz	48.7	49	49.3	%

Figure 46: SyncE Clock Output Timing



4.9 MAC Interface Timing

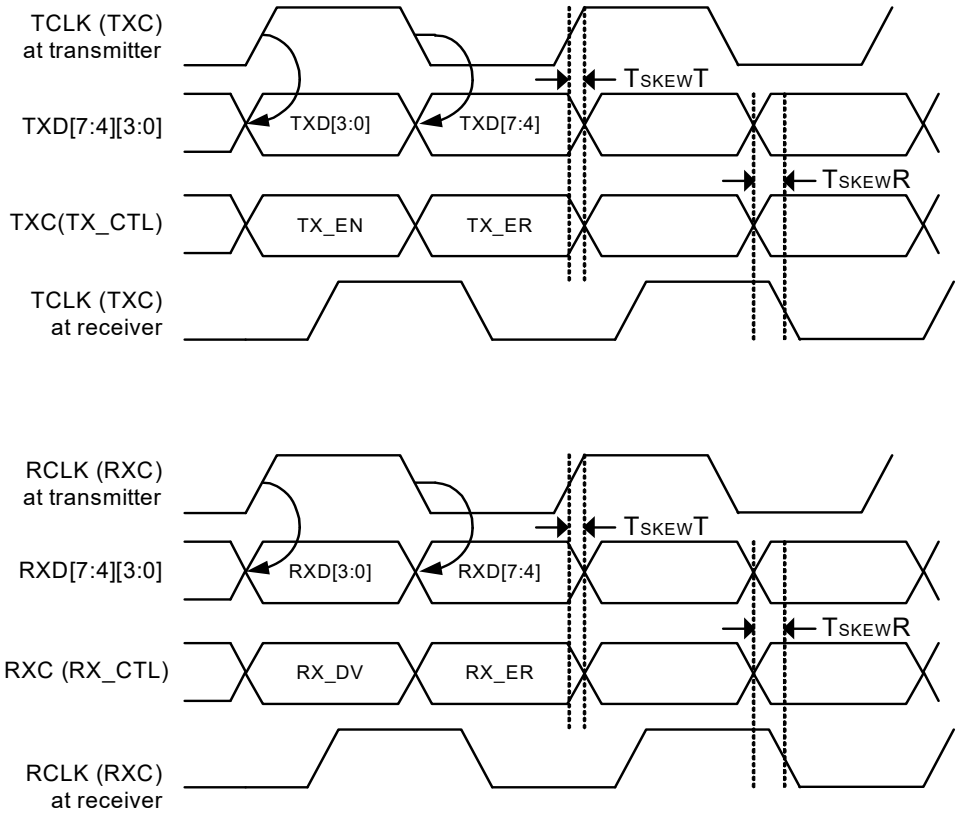
4.9.1 RGMII AC Characteristics

Table 881: RGMII AC Characteristics

(This table is copied from the RGMII Specification. See the four timing modes discussed in Section 4.9.2, RGMII Delay Timing for Different RGMII Modes, on page 472).

Symbol	Parameter	Min	Typ	Max	Unit
TskewT	Data to Clock Output Skew (at Transmitter)	-500	0	500	ps
TskewR	Data to Clock Input Skew (at Receiver)	1.0	–	2.8	ns
T_{CYCLE}	Clock Cycle Duration	7.2	8.0	8.8	ns
$T_{CYCLE\_HIGH100}$	High Time for 1000BASE-T	3.6	4.0	4.4	ns
T_{RISE}/T_{FALL}	Rise/Fall Time (20 to 80%)	–	–	0.75	ns

Figure 47: RGMII Multiplexing and Timing



This figure is copied from the RGMII Specification. See the four timing modes discussed in Section 4.9.2, RGMII Delay Timing for Different RGMII Modes, on page 472.

4.9.2 RGMII Delay Timing for Different RGMII Modes

4.9.2.1 PHY Input — TCLK Delay

Table 882: PHY Input — TCLK No Delay when Register 4.A001.15 = 0
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{setup}	Setup Time	Register 4.A001.15 = 0	1.0	–	–	ns
T_{hold}	Hold Time		0.8	–	–	ns

Figure 48: TCLK No Delay Timing — Register 4.A001.15 = 0

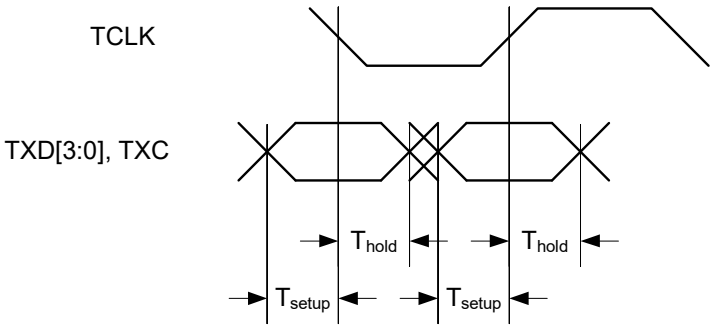
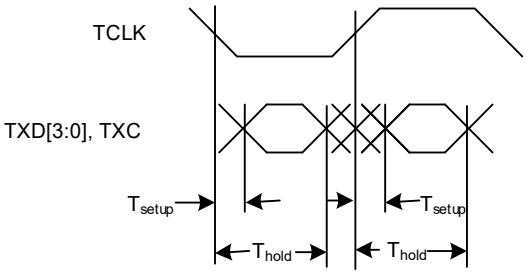


Table 883: PHY Input — TCLK Delay when Register 4.A001.15 = 1
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{setup}	Setup Time	Register 4.A001.15 = 1	-0.9	–	–	ns
T_{hold}	Hold Time		2.7	–	–	ns

Figure 49: TCLK Delay Timing — Register 4.A001.15 = 1



4.9.2.2 PHY Output — RCLK Delay

Table 884: PHY Output — RCLK No Delay when Register 4.A001.14 = 0
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{skew}	Skew Time	Register 4.A001.14 = 0	- 0.5	–	0.5	ns

Figure 50: RGMII RCLK No Delay Timing — Register 4.A001.14 = 0

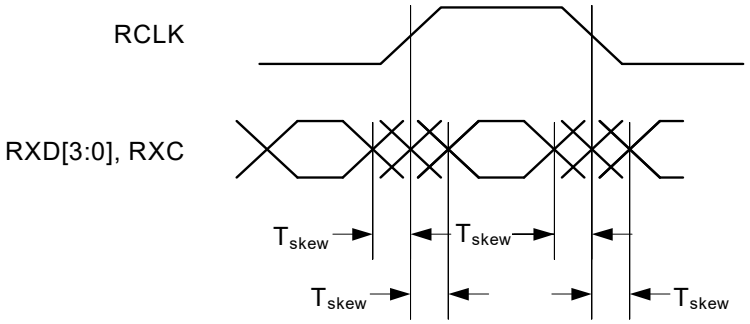
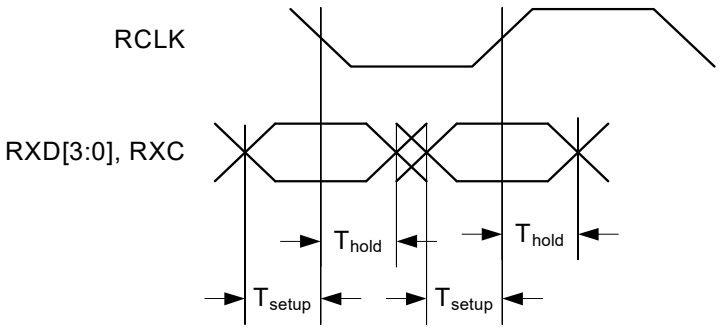


Table 885: PHY Output — RCLK Delay when Register A.8001.14 = 1
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_{setup}	Setup Time	Register 4.A001.14 = 1 (add delay)	1.2	–	–	ns
T_{hold}	Hold Time		1.2	–	–	ns

Figure 51: RGMII RCLK Delay Timing — Register 4.A001.14 = 1



4.9.3 SGMII Interface Timing

Table 886: SGMII Timing

Symbol	Parameter	Min	Typ	Max	Unit
T_{FALL}	V_{OD} Fall Time (20 to 80%)	100	–	200	ps
T_{RISE}	V_{OD} Rise Time (20 to 80%)	100	–	200	ps
T_{SKEW1}[1]	Skew between Two Members of a Differential Pair	–	–	20	ps
$T_{OutputJitter}$	Total Output Jitter Tolerance (Deterministic + 14 × rms Random)	–	127	–	ps

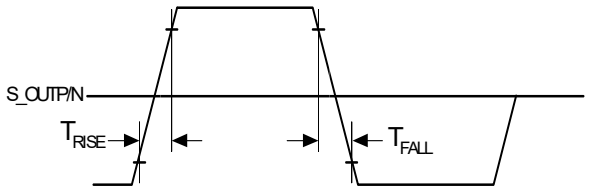
1. Skew measured at 50% of the transition.

4.9.4 SGMII Input AC Characteristics

Table 887: SGMII Input AC Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$T_{InputJitter}$	Total Input Jitter Tolerance (Deterministic + 14 × rms Random)	–	–	599	ps

Figure 52: Serial Interface Rise and Fall Time



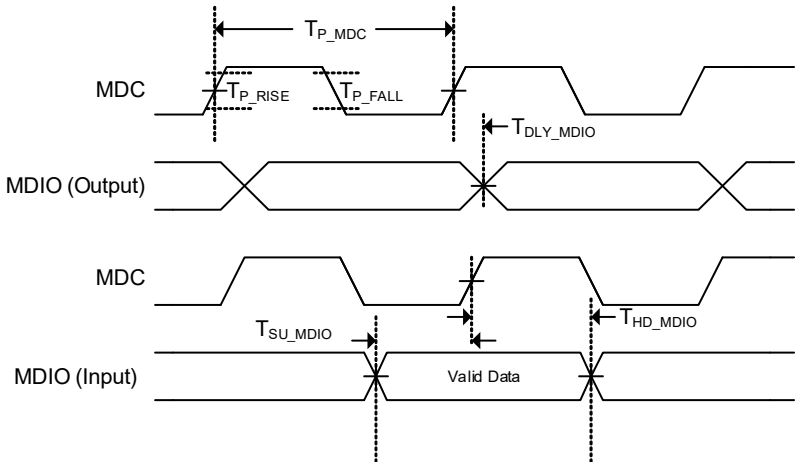
4.10 MDC/MDIO Timing

Table 888: MDC/MDIO Timing
(Over full range of values listed in the Recommended Operating Conditions unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit
T_{P_RISE}/T_{P_FALL}	Rise Time/Fall Time (20 to 80%)	0	–	10	ns
T_{DLY_MDIO}	MDC to MDIO (Output) Delay Time	0	–	20	ns
T_{SU_MDIO}	MDIO (Input) to MDC Setup Time	10	–	–	ns
T_{HD_MDIO}	MDIO (Input) to MDC Hold Time	10	–	–	ns
T_{P_MDC}	MDC Period	80	–	–	ns[1]

1. Maximum frequency = 12.5 MHz.

Figure 53: MDC/MDIO Timing



4.11 Latency Timing

Table 889 lists the transmit and receive latency values. Note that 1000BASE-T1: SGMII MACsec updated based on correlated delay to be released to customer.

Table 889: Latency Timing

MAC Interface	MACsec Mode	Min	Typ	Max	Units
1000BASE-T1					
1000BASE-T1 Tx					
RGMII	Disabled	0.211	0.40082	0.521	µs
SGMII	Disabled	0.44	0.60963	0.768	µs
RGMII	Authority Only	2.425	2.60668	2.804	µs
SGMII	Authority Only	2.654	2.81549	3.051	µs
1000BASE-T1 Rx					
RGMII	Disabled	4.125	4.30474	4.498	µs
SGMII	Disabled	4.281	4.43126	4.625	µs
RGMII	Authority Only	6.407	6.57543	6.716	µs
SGMII	Authority Only	6.563	6.70195	6.843	µs
100BASE-T1					
100BASE-T1 Tx					
RGMII	Disabled	0.749	0.78437	0.845	µs
SGMII	Disabled	0.981	1.01225	1.048	µs
RGMII	Authority Only	22.322	22.41222	22.485	µs
SGMII	Authority Only	22.554	22.6401	22.688	µs
100BASE-T1 Rx					
RGMII	Disabled	0.881	0.91029	0.948	µs
SGMII	Disabled	1.397	1.43234	1.466	µs
RGMII	Authority Only	22.763	22.88094	23.015	µs
SGMII	Authority Only	23.279	23.40299	23.533	µs

Note Authority Only means that first enable MACsec and set to “Cut through” and “Low latency”, then set PAB_RX.DELAY_CFG (0x1F.0288)/ PAB_TX.DELAY_CFG (0x1F.0308) = 0x10000085, MPTP_CFG(0x1F.A008) = 0x1E.

5 Package Mechanical Dimensions

5.1 40-pin QFN Package

Figure 54: 40-pin QFN Package Mechanical Drawing

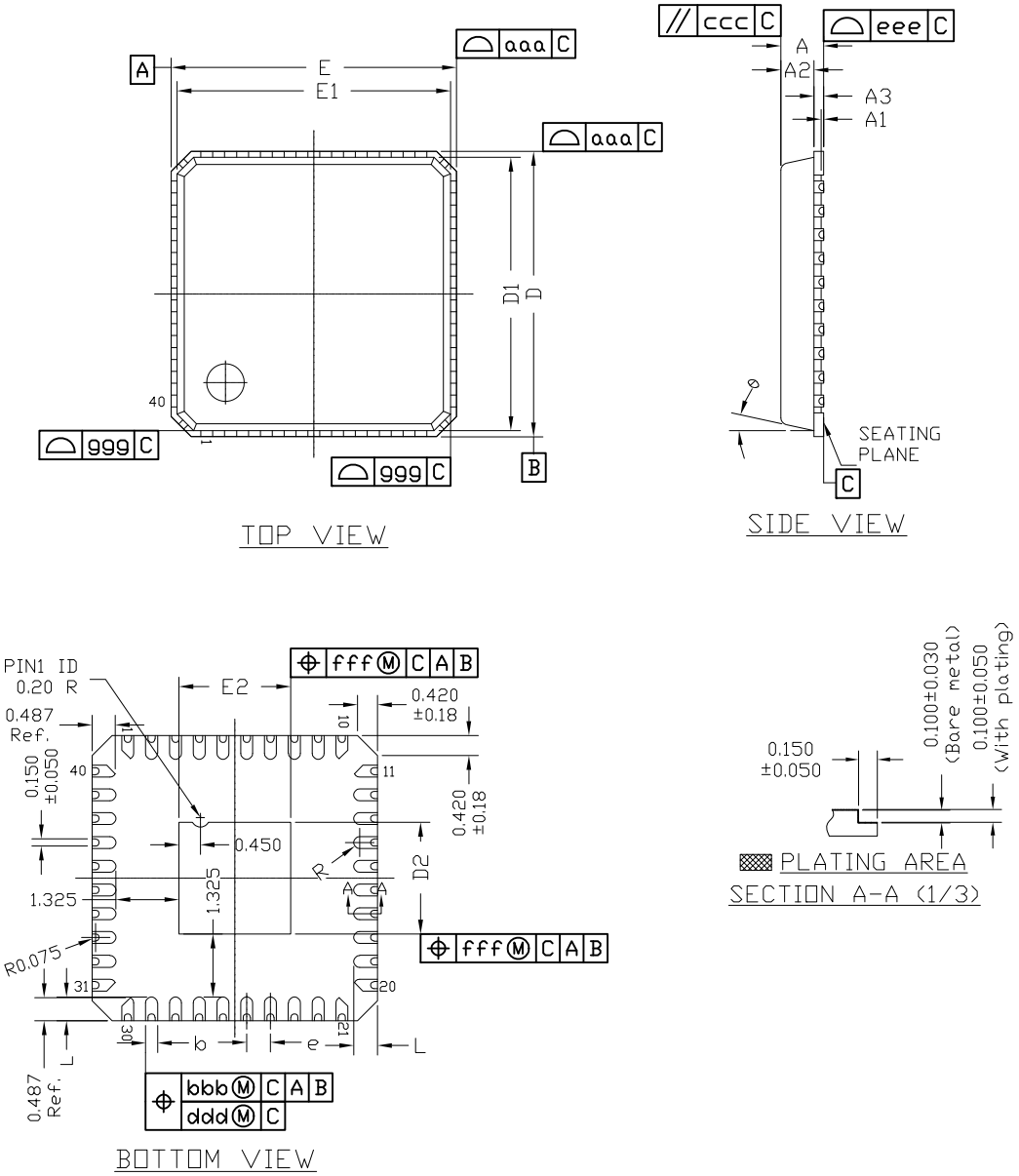


Table 890: 40-pin QFN Package Dimensions

Symbol	Dimension in mm		
	Min	Nom	Max
A	0.800	0.850	0.900
A1	0.000	0.020	0.050
A2	0.600	0.650	0.700
A3		0.203 REF.	
b	0.180	0.250	0.300
D		6 BSC	
D1		5.750 BSC	
D2	2.25	2.35	2.45
E		6 BSC	
E1		5.750 BSC	
E2	2.25	2.35	2.45
L	0.400	0.500	0.600
e		0.500 BSC	
Θ	0°	–	14°
R	0.090	–	–
Tolerances of Form and Position			
aaa		0.150	
bbb		0.100	
ccc		0.100	
ddd		0.050	
eee		0.080	
fff		0.100	
ggg		0.200	

5.2 40-pin QFN (6 mm x 6 mm) Package Information

Table 891: 40-pin QFN (6 mm x 6 mm) Package Information

Symbol	Parameter	Min	Typ	Max	Unit
$P_{PRESSURE}$	Maximum pressure on the package	–	–	20	N
$T_{STORAGE}$[1]	Storage temperature	-55	–	+125[2]	°C

1. The conditions for storing unpowered and unmounted devices are as follows:
   - Packed inside a vacuum-sealed moisture barrier bag with desiccant and humidity indicator card (HIC)
   - Stored at <40°C and <90% relative humidity (RH)

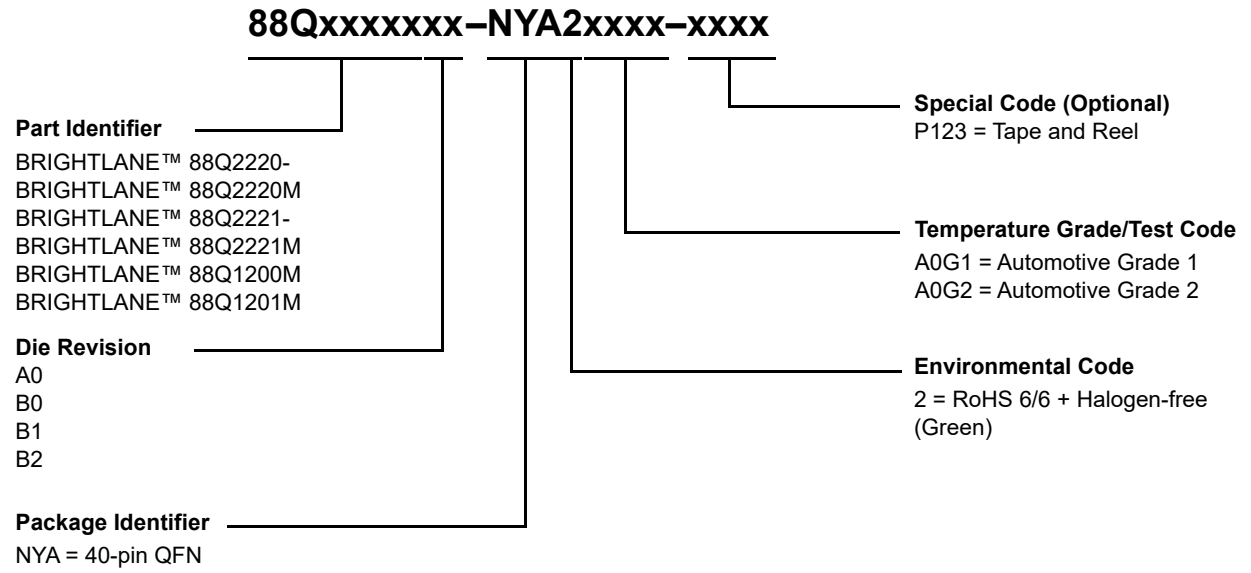
2. 125°C is only used as bake temperature for not more than 24 hours. Long-term storage (for example, weeks or longer) must be kept at 85°C or lower.

6 Part Order Numbering/Package Marking

6.1 Part Order Numbering

Figure 55 shows the ordering part numbering scheme for the device. Refer to the relevant release notes on the Infineon customer portal for the latest revision and complete part ordering information.

Figure 55: Sample Part Number



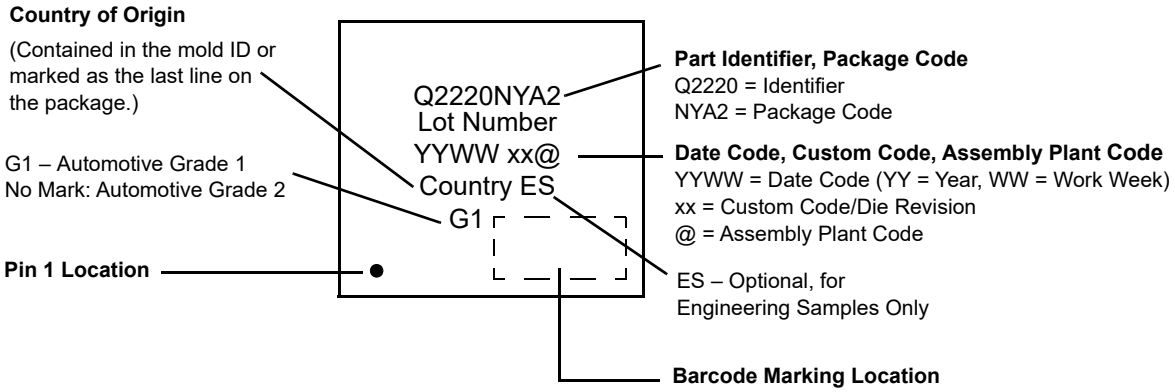
Note

Refer to the release notes associated with a specific device for revision details.

6.2 Package Marking

Figure 56 shows a sample package marking and pin 1 location for the BRIGHTLANE™ 88Q2220 40-pin QFN package (Automotive, Green).

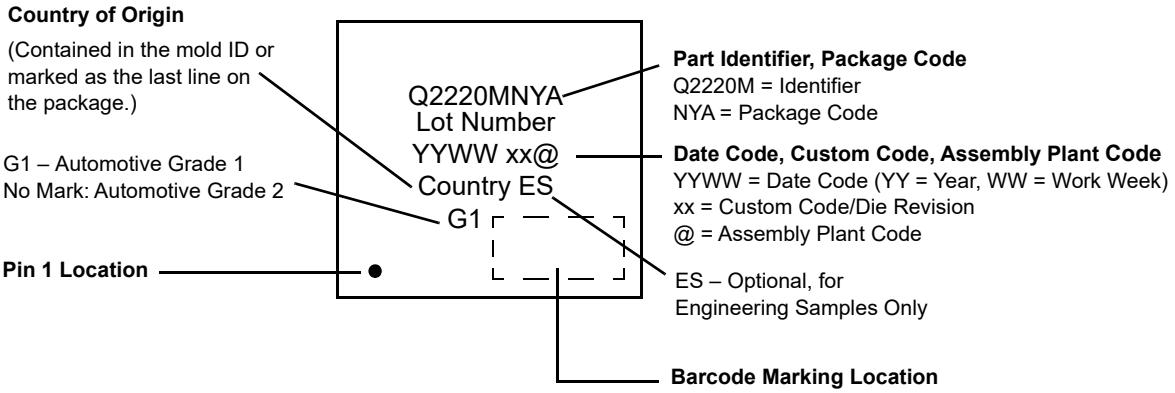
Figure 56: BRIGHTLANE™ 88Q2220 40-pin QFN Sample Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. The location of the markings is approximate.

Figure 57 shows a sample package marking and pin 1 location for the BRIGHTLANE™ 88Q2220M 40-pin QFN package (Automotive, Green).

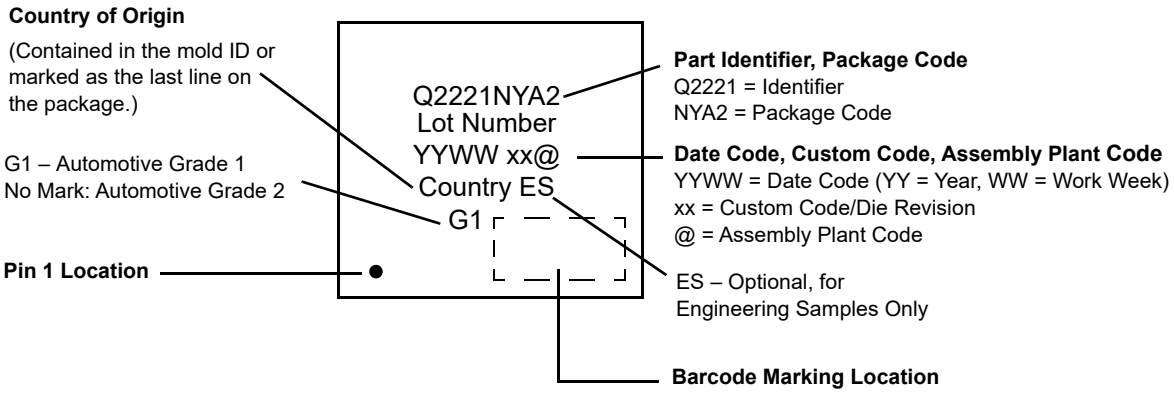
Figure 57: BRIGHTLANE™ 88Q2220M 40-pin QFN Sample Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. The location of the markings is approximate.

Figure 58 shows a sample package marking and pin 1 location for the BRIGHTLANE™ 88Q2221 40-pin QFN package (Automotive, Green).

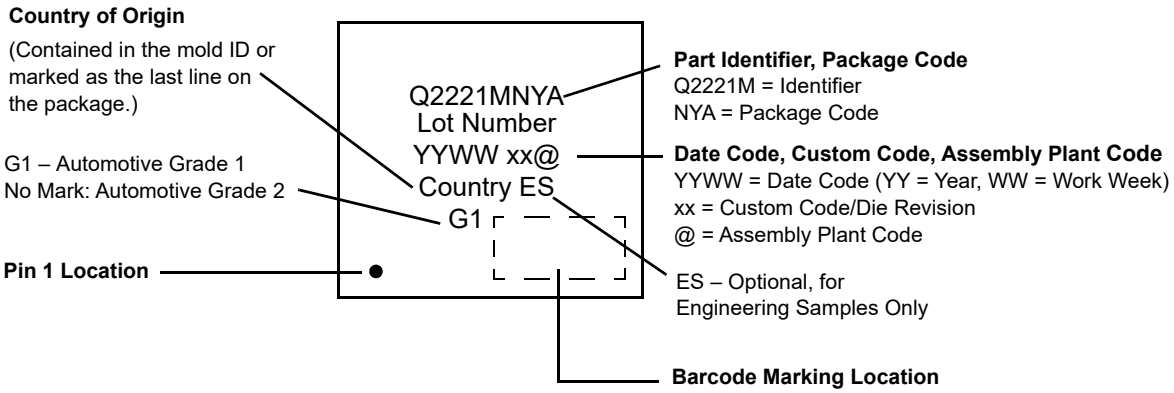
Figure 58: BRIGHTLANE™ 88Q2221 40-pin QFN Sample Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. The location of the markings is approximate.

Figure 59 shows a sample package marking and pin 1 location for the BRIGHTLANE™ 88Q2221M 40-pin QFN package (Automotive, Green).

Figure 59: BRIGHTLANE™ 88Q2221M 40-pin QFN Sample Package Marking and Pin 1 Location

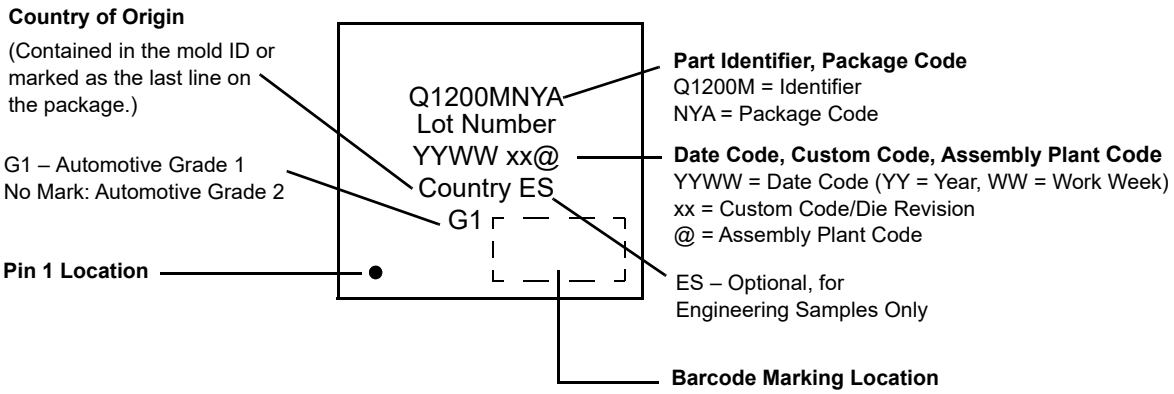


Note: The above example is not drawn to scale. The location of the markings is approximate.

Part Order Numbering/Package Marking

Figure 60 shows a sample package marking and pin 1 location for the BRIGHTLANE™ 88Q1200M 40-pin QFN package (Automotive, Green).

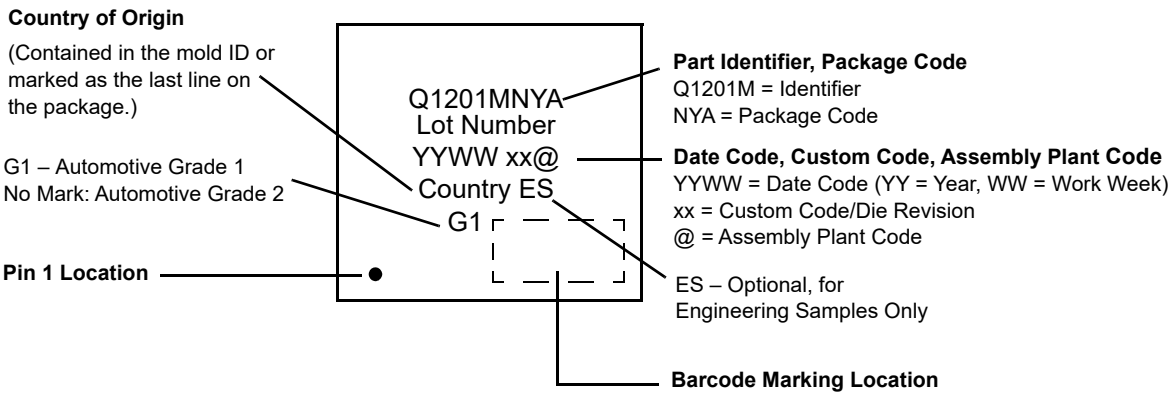
Figure 60: BRIGHTLANE™ 88Q1200M 40-pin QFN Sample Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. The location of the markings is approximate.

Figure 61 shows a sample package marking and pin 1 location for the BRIGHTLANE™ 88Q1201M 40-pin QFN package (Automotive, Green).

Figure 61: BRIGHTLANE™ 88Q1201M 40-pin QFN Sample Package Marking and Pin 1 Location



Note: The above example is not drawn to scale. The location of the markings is approximate.

A Revision History

Table 892: Revision History

Revision	Description	Date
Rev. 16	Migrated to Infineon template. • Updated AVDDLS to AVDDL in Table 22, Table 23. Table 44, and Table 45.	October 30, 2025
Rev. 15 v15.00f	***Rev. 15 release.*** ***Section 3, Registers*** • Table 110, Interrupt Enable Register, on page 145 updated. • Table 156, LPSD Data Sleep Restore, on page 165 updated. • Table 222, Receiver Status Register, on page 194 updated.	June 23, 2025
Rev. 14 v14.00c	***Rev. 14 release.*** ***Section 6, Part Order Numbering/Package Marking*** • Figure 58, BRIGHTLANE™ 88Q2221 40-pin QFN Sample Package Marking and Pin 1 Location, on page 481 updated. • Figure 59, BRIGHTLANE™ 88Q2221M 40-pin QFN Sample Package Marking and Pin 1 Location, on page 481 updated.	April 22, 2025

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 13 v13.00f	***Rev. 13 release.*** ***Section 2, PHY Functional Specifications*** • Table 51, LPSD Electrical Characteristics, on page 77 updated. • Section 2.21.1, AVDDL updated. • Section 2.21.2, AVDD33 updated. • Section 2.21.4, REG_IN updated. ***Section 3, Registers*** • Table 101, MCS_TOP_SLAVE.DBG_MUX_SEL, on page 142 added. • Table 102, BBE_SLAVE0.DBG_MUX_SEL, on page 142 added. • Table 103, BBE_SLAVE1.DBG_MUX_SEL, on page 143 added. • Table 101, SLC_INTR_SET, on page 140 added. • Table 102, MEM_ECC_ERR_CNT, on page 141 added. • Table 103, MMAC_ALERT_CFG, on page 141 added. • Table 124, PCS Interrupt Status Register, on page 152 added. • Table 125, PCS Interrupt Mask Register, on page 152 added. • Table 127, Enable PLL Clock Check, on page 153 added. • Table 128, Configure Frequency Offset Check PLL, on page 154 added. • Table 129, Enable 125 MHz Reference Clock Check, on page 154 added. • Table 130, Configure Frequency Offset Check of 125 MHz Ref Clock, on page 154 added. • Table 146, PHY Safety Detection Enable Register, on page 158 added. • Table 147, PHY Safety Detection Status Register, on page 159 added. • Table 149, Under-voltage Detection Config 2, on page 161 updated. • Table 165, 1000BASE-T1 PCS Status Register 1, on page 172 updated. ***Section 4, Electrical Specifications*** • Table 863, Absolute Maximum Ratings, on page 454 updated. • Table 878, 25 MHz Oscillator Requirements, on page 467 updated. ***Section 6, Part Order Numbering/Package Marking*** • Figure 56, BRIGHTLANE™ 88Q2220 40-pin QFN Sample Package Marking and Pin 1 Location, on page 480 updated. • Figure 59, BRIGHTLANE™ 88Q2221M 40-pin QFN Sample Package Marking and Pin 1 Location, on page 481 updated.	March 13, 2025

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 12 v12.00g	***Rev. 12 release.***	October 30, 2024
	Section 2, PHY Functional Specifications • Section 2.7.4, WAKE_OUT to WAKE_IN Pin or INH Pin updated. • Section 2.7.2.2, Enter Sleep Modes updated. • Figure 22, LPSD Block Diagram — Option 1, on page 76 updated. • Figure 23, LPSD Block Diagram — Option 2 (only Applicable in Rev. B2), on page 77 updated. ***Section 3, Registers*** • Table 114, LPSD Control Register 2, on page 148 updated. ***Section 6, Part Order Numbering/Package Marking*** • Figure 55, Sample Part Number, on page 479 updated. • Figure 56, BRIGHTLANE™ 88Q2220 40-pin QFN Sample Package Marking and Pin 1 Location, on page 480 updated. • Figure 57, BRIGHTLANE™ 88Q2220M 40-pin QFN Sample Package Marking and Pin 1 Location, on page 480 updated. • Figure 58, BRIGHTLANE™ 88Q2221 40-pin QFN Sample Package Marking and Pin 1 Location, on page 481 updated. • Figure 59, BRIGHTLANE™ 88Q2221M 40-pin QFN Sample Package Marking and Pin 1 Location, on page 481 updated. • Figure 60, BRIGHTLANE™ 88Q1200M 40-pin QFN Sample Package Marking and Pin 1 Location, on page 482 updated. • Figure 61, BRIGHTLANE™ 88Q1201M 40-pin QFN Sample Package Marking and Pin 1 Location, on page 482 updated.	

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 11 v11.00h	***Rev. 11 release.***	June 14, 2024
	Section 1, Signal Description • Table 7, BRIGHTLANE™ 88Q2220/88Q2220M Clock/Configuration/Reset/I/O, on page 34 updated. • Table 10, BRIGHTLANE™ 88Q2220/88Q2220M Low Power Signal Detect, on page 35 updated. • Table 18, BRIGHTLANE™ 88Q2221/88Q2221M Clock/Configuration/Reset/I/O, on page 41 updated. • Table 21, BRIGHTLANE™ 88Q2221/88Q2221M Low Power Signal Detect, on page 42 updated. • Table 29, BRIGHTLANE™ 88Q1200M Clock/Configuration/Reset/I/O, on page 48 updated. • Table 32, BRIGHTLANE™ 88Q1200M Low Power Signal Detect, on page 49 updated. • Table 40, BRIGHTLANE™ 88Q1201M Clock/Configuration/Reset/I/O, on page 55 updated. • Table 43, BRIGHTLANE™ 88Q1201M Low Power Signal Detect, on page 56 updated. • Figure 9, BRIGHTLANE™ 88Q2220M/88Q2221M Functional Block Diagram, on page 59 restored from version 9. ***Section 2, PHY Functional Specifications*** • Table 51, LPSD Electrical Characteristics, on page 77 updated. • Table 52, Status of Functional Block in Each Mode, on page 79 updated. • Figure 12, BRIGHTLANE™ 88Q1201 Functional Block Diagram, on page 62 updated. • Figure 23, LPSD Block Diagram — Option 2 (only Applicable in Rev. B2), on page 77 updated. • Section 2.7.5.3, LPSD Application Notes updated. • Figure 32, Regulator-generated 1.2V for AVDDL, on page 94 updated. • Figure 33, Regulator-generated for DVDD, on page 95 updated.	

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 11 v11.00h (continued)	***Section 2, PHY Functional Specifications*** • Table 51, LPSD Electrical Characteristics, on page 77 updated. • Table 52, Status of Functional Block in Each Mode, on page 79 updated. • Section 2.7.4, WAKE_OUT to WAKE_IN Pin or INH Pin updated. • WAKE_OUT Widths table removed. • Section 2.10.1, VCT Configuration updated. • Section 2.16.1, Hardware Reset State updated. • Section 2.21, Regulators and Power Supplies updated. • Section 2.21.7, Power Supply Sequencing updated. • Section 2.21.8, Under-voltage (UV) detection updated. • Section 2.22.3.3, Trigger Pulse Generate Function updated. ***Section 3, Registers*** • Table 111, GPIO Interrupt Status Register, on page 146 updated. • Table 112, Common LPSD Control Register 1, on page 146 updated. • Table 136, TDR Reset Register, on page 156 updated. • Table 145, Under Voltage Interrupt Mask Register, on page 158 updated. • Table 150, Under Voltage Interrupt Status Register, on page 162 updated. • Table 156, LPSD Data Sleep Restore, on page 165 updated. • Transition Safe State Enable table removed. • Table 165, 1000BASE-T1 PCS Status Register 1, on page 172 updated. • Table 327, PTP Port Config Register 3, on page 250 updated. • Table 349, TAI Global Config 22, on page 266 updated. • Table 355, TAI Global Config 28, on page 276 updated. • Table 378, PTP Status 5, on page 290 updated. • Table 394, PTP Global Time Array 21, on page 297 updated. • Some MMAC/PTP registers designated and internal and were removed. • Table 782 to Table 852 and Table 984, removed [internal registers]. ***Section 4, Electrical Specifications*** • Table 864, Recommended Operating Conditions, on page 455 updated. • Table 870, ESD Ratings, on page 460 updated. • Table 872, Digital Pin Operating Conditions, on page 461 updated. • Table 878, 25 MHz Oscillator Requirements, on page 467 updated.	June 14, 2024

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 10	***Rev. 10 release.***	April 12, 2024
Rev. 10 v10.00g	***Section 1, Signal Description*** • Table 11, BRIGHTLANE™ 88Q2220/88Q2220M Power, Ground, and Internal Regulators, on page 36 updated. • Table 22, BRIGHTLANE™ 88Q2221/88Q2221M Power, Ground, and Internal Regulators, on page 43 updated. • Table 33, BRIGHTLANE™ 88Q1200M Power, Ground, and Internal Regulators, on page 50 updated. • Table 33, BRIGHTLANE™ 88Q1200M Power, Ground, and Internal Regulators, on page 50 updated. ***Section 2, PHY Functional Specifications*** • Figure 9, BRIGHTLANE™ 88Q2220M/88Q2221M Functional Block Diagram, on page 59 updated. • Table 52, Status of Functional Block in Each Mode, on page 79 updated. • Figure 33, Regulator-generated for DVDD, on page 95 updated. • Section 2.21, Regulators and Power Supplies updated. ***Section 3, Registers*** • Table 108, Tx Disable Status Register, on page 144 updated. • Table 149, Under-voltage Detection Config 2, on page 161 updated. • Table 153, Secondary ID Register, on page 163 updated. • Table 268, 1000BT1 Sleep/Wakeup Interrupt Enable, on page 215 updated. • Table 286, 1000BASE-T1 Link Training Time, on page 220 updated. • Table 287, 1000BASE-T1 Local Receiver Time, on page 221 updated. • Table 288, 1000BASE-T1 Remote Receiver Time, on page 221 updated. • Table 465, MACsec Summary Register Map, on page 318 updated. • Table 662, SA_MAP_MEM0, on page 403 updated. • Table 663, SA_MAP_MEM1, on page 403 updated. • Table 664, SA_MAP_MEM2, on page 404 updated. • Table 665, SA_MAP_MEM3, on page 404 updated.	

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 10 v10.00g (continued)	***Section 4, Electrical Specifications*** • Table 863, Absolute Maximum Ratings, on page 454 updated. • Table 864, Recommended Operating Conditions, on page 455 updated. • Section 4.4.1, Current Consumption when Using External Regulators updated. • Table 868, Current Consumption DVDD, on page 458 updated. • Section 4.6.1, Digital Pin Grouping updated. • Table 871, Digital Pin Grouping, on page 461 updated. • Section 4.6.2, Digital Pin Operating Conditions updated. • Table 872, Digital Pin Operating Conditions, on page 461 updated. • Table 873, Internal Resistors, on page 463 updated. • Table 875, Transmitter DC Characteristics, on page 465 updated. • Table 876, Receiver DC Characteristics, on page 465 updated. • Table 889, Latency Timing, on page 476 updated.	April 12, 2024
Rev. 9	***Rev. 9 release.***	November 10, 2023
Rev. 9 v9.00c	***Section 3, Registers*** • Table 148, Under-voltage Detection Config 1, on page 160 reordered to a new section. • Under-voltage Detection Config 2 Device 4, Register 0x8701 removed. • Table 149, Under-voltage Detection Config 2, on page 161 renamed and reordered to a new section. • Section 3.13 Under-voltage Registers removed ***Section 4, Electrical Specifications*** • Table 863, Absolute Maximum Ratings, on page 454 updated.	

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 8	***Rev. 8 release.***	October 30, 2023
Rev. 8 v8.00j	***Section 1, Signal Description*** • Table 43, BRIGHTLANE™ 88Q1201M Low Power Signal Detect, on page 56 updated. ***Section 2, PHY Functional Specifications*** • Section 2.2.2.1, 1.25 GHz SERDES Interface updated. • Section 2.6.1, IEEE Power Down Mode updated. • In-band Wake/Sleep Embedded IDLES removed. • RGMII Coding – For Legacy in-band Status and the New Sleep/Wake Command Mapping for the PHY table removed. • RGMII Coding – For Legacy in-band Status and the New Sleep/Wake Command Mapping for the Switch table removed. • Commands Passed through SGMII Code Group (8-bit) table removed. • Section 2.7.2.2, Enter Sleep Modes reordered. • Sleep Handshake removed. • Section 2.7.2.2.1, Low Power Sleep reordered. • Section 2.7.2.3, Sleep/Wake Forward Through Host Interface By Command Idle Codegroup (CIC) added. • In-band WUP, WUR, and LPS Commands removed. • Figure 21, In-band Communication Transaction, on page 74 reordered. • Section 2.7.2.3.1, Messages in CIC added. • Section 2.7.4, WAKE_OUT to WAKE_IN Pin or INH Pin updated. • Figure 22, LPSD Block Diagram — Option 1, on page 76 updated. • Figure 23, LPSD Block Diagram — Option 2 (only Applicable in Rev. B2), on page 77 updated. • Section 2.7.5.1, LPSD Option updated. • Section 2.12, Automatic Polarity Detection and Correction updated. • Section 2.19.1, Hardware Configuration updated. • Section 2.21.7, Power Supply Sequencing updated. • Section 2.21.8, Under-voltage (UV) detection added. ***Section 3, Registers*** • Table 113, Common Sleep/Wakeup Configuration, on page 148 updated. • Table 114, LPSD Control Register 2, on page 148 updated. • Table 156, LPSD Data Sleep Restore, on page 165 added.	

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 8 v8.00j (continued)	***Section 3, Registers*** • Table 157, LPSD Data Sleep Control, on page 169 added. • Table 219, Bad SSD Counter Register, on page 193 updated. • Table 220, Bad ESD Counter Register, on page 193 updated. • Table 222, Receiver Status Register, on page 194 updated. • Table 247, 100BASE-T1 LPSD Status Register, on page 203 updated. • Table 252, 100BASE-T1 Sleep/Wakeup Interrupt Enable, on page 206 updated. • Table 263, 1000BT LPSD Status Register, on page 213 updated. • Table 267, 1000BT1 Sleep/Wakeup Interrupt Status, on page 214 updated. • Table 268, 1000BT1 Sleep/Wakeup Interrupt Enable, on page 215 updated. • Table 271, Signal Quality Index, on page 216 updated. • Table 294, RGMII_IO Control Register, on page 224 updated. • Table 314, SGMII Specific Control Register 2, on page 239 updated. • Table 372, TAI Global Config 12, on page 286 updated. • Table 693, RX_ETYPE, on page 397 updated. • Table 591, SA_MAP_MEM1, on page 376 updated. • Table 592, SA_MAP_MEM2, on page 376 updated. • Table 593, SA_MAP_MEM3, on page 376 updated. • Table 594, SA_MAP_MEM4, on page 377 updated. • Table 595, SA_MAP_MEM5, on page 377 updated. • Table 596, SA_MAP_MEM6, on page 377 updated. • Table 597, SA_MAP_MEM7, on page 377 updated. • Table 598, SA_MAP_MEM8, on page 378 updated. • Table 599, SA_MAP_MEM9, on page 378 updated. • Table 600, SA_MAP_MEM10, on page 378 updated. • Table 601, SA_MAP_MEM11, on page 378 updated. • Table 602, SA_MAP_MEM12, on page 379 updated. • Table 603, SA_MAP_MEM13, on page 379 updated. • Table 604, SA_MAP_MEM14, on page 379 updated. • Section 3.13, Under-voltage Registers added. ***Section 4, Electrical Specifications*** • Section 4.2, Recommended Operating Conditions updated. • Figure 49, TCLK Delay Timing — Register 4.A001.15 = 1, on page 472 updated. • Figure 53, MDC/MDIO Timing, on page 475 updated. • Table 864, Recommended Operating Conditions, on page 455 updated. • Table 869, Current Consumption VDDO, on page 459 updated.	October 30, 2023

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 8 v8.00j (continued)	***Section 4, Electrical Specifications*** • Table 870, ESD Ratings, on page 460 added. • Table 883, PHY Input — TCLK Delay when Register 4.A001.15 = 1, on page 472 updated • Table 888, MDC/MDIO Timing, on page 475 updated • Table 889, Latency Timing, on page 476 added. ***Section 6, Part Order Numbering/Package Marking*** • Figure 56, BRIGHTLANE™ 88Q2220 40-pin QFN Sample Package Marking and Pin 1 Location, on page 480 updated.	October 30, 2023

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 7	***Rev. 7 release.***	April 27, 2023
Rev. 7 v7.00n	***Final*** ***Product Overview*** section updated. ***Section 1, Signal Description*** • Table 43, BRIGHTLANE™ 88Q1201M Low Power Signal Detect, on page 56 updated. ***Section 2, PHY Functional Specifications*** • Section 2.6, Power Management updated. • Section 2.6.1, IEEE Power Down Mode updated. • Figure 22, LPSD Block Diagram — Option 1, on page 76 updated. • Figure 23, LPSD Block Diagram - VBAT Option 2, on page 73 removed. • Table 51, LPSD Electrical Characteristics, on page 77 updated. • Section 2.6.2, Passive Mode removed. • Section 2.12, Automatic Polarity Detection and Correction updated. • Section 2.13, DME Pages Exchange Complete with No Link updated. • Section 2.23, MMAC: MAC and MACsec updated. • Section 2.23.1, Overview updated. ***Section 3, Registers*** • Table 106, Config Register, on page 143 updated. • Table 107, MDIO Broadcast Mode Register, on page 144 added. • Table 111, MDIO Write Signature, on page 148 added. • Table 112, MDIO Read Signature, on page 148 added. • Table 110, Interrupt Enable Register, on page 145 updated. • Table 111, GPIO Interrupt Status Register, on page 146 updated. • Table 112, Common LPSD Control Register 1, on page 146 updated. • Table 114, LPSD Control Register 2, on page 148 added. • Table 115, Temperature Sensor Register 1, on page 148 updated. • Table 118, TDR Status Register 1 Device 3, Register 0xFEDB removed. • Table 116, Temperature Sensor Register 2, on page 149 updated. • Table 119 1000BT Sleep/Wake Request Device 3, Register 0x8022 removed. • Table 119, TDR Status Register 2 Device 3, Register 0xFEDC removed. • Table 117, FailSafe Control Register 1, on page 150 added.	

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 7 v7.00n (continued)	• Table 118, FailSafe Control Register 2, on page 150 added. • Table 119, FailSafe Status Register, on page 150 added. • Table 120, Remote GPIO Command Register, on page 150 added. • Table 121, Remote GPIO Status Register, on page 151 added. • Table 122, Temperature Sensor Register 3, on page 151 • Table 132, TDR Offset Cutoff, on page 155 added. • Table 133, TDR Offset Shortcable, on page 155 added. • Table 134, TDR Status, on page 155 added. • Table 135, TDR Offset Longcable, on page 155 added. • Table 136, TDR Reset Register, on page 156 added. • Table 141, SQI Register Device 3, Register 0xFC4 removed. • Table 150, Under Voltage Interrupt Status Register, on page 162 updated. • Table 151, Critical Failure Interrupt Register, on page 162 updated. • Table 145, Transition Safe State Enable, on page 164 added. • Table 231: BIST Control Register Device 3, Register 0x8617 removed. • Table 232: BIST Status Register Device 3, Register 0x8618 removed. • Table 233: BIST Counters Register Device 3, Register 0x8619 removed. • Table 247, 100BASE-T1 LPSD Status Register, on page 203 updated. • Table 247, 100BASE-T1 LPSD Status Register, on page 203 added. • Table 253, 100BT1 Sleep/Wakeup Interrupt Status 2, on page 206 added. • Table 254, 100BT1 Sleep/Wakeup Interrupt Enable 2, on page 207 updated. • Table 257, GPIO Function and Interrupt Tri-state Control Register, on page 209 updated. • Table 259, Open Drain Control Register, on page 211 updated. • Table 260, LED Function Control Register, on page 211 updated. • Table 269, 1000BT1 Sleep/Wakeup Interrupt Status 2, on page 216 added. • Table 270, 1000BT1 Sleep/Wakeup Interrupt Enable 2, on page 216 added. • Table 271, Signal Quality Index, on page 216 added. • Table 272, Mean Square Error, on page 216 added. • Table 273, Worst Case Mean Square Error, on page 217 added. • Table 280, LinkUp Status Count, on page 219 added. • Table 281, LinkDown Status Count, on page 219 added.	4/27/2023

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 7 v7.00n (continued)	• Table 282, Enable Code Word Count, on page 220 added. • Table 283, Retain Code Word Count, on page 220 added. • Table 284, Clear Code Word Count, on page 220 added. • Table 274, 1000BT1 LTT_TIMER, on page 216 removed. • Table 285, Correctable Code Word Count, on page 220 added. • Table 275, 1000BT1 LRT_TIMER, on page 216 removed. • Table 276, 1000BT1 RRT_TIMER, on page 216 removed. • Table 299, PTP Control Register 5 other fields, Device 0x1F, Register 0xA005 removed. ***Section 4, Electrical Specifications*** • Section 4.4.1, Current Consumption when Using External Regulators updated. • Table 866, Current Consumption AVDDL, on page 457 updated. • Table 867, Current Consumption AVDD33, on page 458 updated. • Table 868, Current Consumption DVDD, on page 458 updated. • Table 869, Current Consumption VDDO, on page 459 updated. • Table 875, Transmitter DC Characteristics, on page 465 updated. • Table 876, Receiver DC Characteristics, on page 465 updated. • Section 4.9.2, RGMII Delay Timing for Different RGMII Modes updated. ***Section 6, Part Order Numbering/Package Marking*** • Figure 56, BRIGHTLANE™ 88Q2220 40-pin QFN Sample Package Marking and Pin 1 Location, on page 480 updated. • Figure 57, BRIGHTLANE™ 88Q2220M 40-pin QFN Sample Package Marking and Pin 1 Location, on page 480 updated. • Figure 58, BRIGHTLANE™ 88Q2221 40-pin QFN Sample Package Marking and Pin 1 Location, on page 481 updated. • Figure 59, BRIGHTLANE™ 88Q2221M 40-pin QFN Sample Package Marking and Pin 1 Location, on page 481 updated. • Figure 60, BRIGHTLANE™ 88Q1200M 40-pin QFN Sample Package Marking and Pin 1 Location, on page 482 updated. • Figure 61, BRIGHTLANE™ 88Q1201M 40-pin QFN Sample Package Marking and Pin 1 Location, on page 482 updated.	4/27/2023

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 6	***Rev. 6 release.***	1/31/2023
Rev. 6 v6.00m	***Cover title*** updated. ***Product Overview*** section updated. ***Section 1, Signal Description*** • Table 9, BRIGHTLANE™ 88Q2220/88Q2220M Test, on page 35 updated. • Table 10, BRIGHTLANE™ 88Q2220/88Q2220M Low Power Signal Detect, on page 35 updated. • Table 12, BRIGHTLANE™ 88Q2220/88Q2220M 40-pin QFN Pin Assignment List — Alphabetical by Signal Name, on page 37 updated. • Table 20, BRIGHTLANE™ 88Q2221/88Q2221M Test, on page 41 updated. • Table 21, BRIGHTLANE™ 88Q2221/88Q2221M Low Power Signal Detect, on page 42 updated. • Table 31, BRIGHTLANE™ 88Q1200M Test, on page 48 updated. • Table 32, BRIGHTLANE™ 88Q1200M Low Power Signal Detect, on page 49 updated. • Table 42, BRIGHTLANE™ 88Q1201M Test, on page 55 updated. • Table 43, BRIGHTLANE™ 88Q1201M Low Power Signal Detect, on page 56 updated. ***Section 2, PHY Functional Specifications*** • Section 2.6.2, Passive Mode added. • Figure 32, Regulator-generated 1.2V for AVDDL, on page 94 updated. • Table 51, LPSD Electrical Characteristics, on page 77 updated.	

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 6 v6.00m (continued)	• Table 58, Sampled Values, on page 89 updated. • Section 2.21.7, Power Supply Sequencing updated. • Section 2.22.1.1, PTP Event Request updated. • Section 2.22.1.2, PTP Trigger Generate updated. • Section 2.22.1.3, PTP Control Register updated. • Section 2.22.4, ReadPlus Command updated. ***Section 3, Registers*** • Table 86, PMA/PMD Device Identifier Register 1, on page 135 updated. • Table 87, PMA/PMD Device Identifier Register 2, on page 135 updated. • Table 91, PMA/PMD Package Identifier Register 1, on page 137 updated. • Table 92, PMA/PMD Package Identifier Register 2, on page 137 updated. • Table 161, PCS Device Identifier Register 1, on page 171 updated. • Table 162, PCS Device Identifier Register 2, on page 171 updated. • Table 166, PCS Package Identifier Register 1, on page 173 updated. • Table 167, PCS Package Identifier Register 2, on page 173 updated. • Table 183, Auto-Negotiation Device Identifier Register 1, on page 178 updated. • Table 184, Auto-Negotiation Device Identifier Register 2, on page 179 updated. • Table 187, Auto-Negotiation Package Identifier Register 1, on page 180 updated. • Table 188, Auto-Negotiation Package Identifier Register 2, on page 180 updated. • Table 205, 100BASE-T1 Status Register, on page 188 updated. • Table 247, 100BASE-T1 LPSD Status Register, on page 203 updated. • Table 264, 1000BT1 Sleep/Wake Request, on page 213 updated. • Table 299, PHY Identifier Register 1, on page 228 updated. • Table 269, 1000BT1 Sleep/Wakeup Interrupt Status 2, on page 216 added. • Table 270, 1000BT1 Sleep/Wakeup Interrupt Enable 2, on page 216 added. • Section 3.10, PTP Registers added. • Section 3.11, MMAC Registers added. • Section 3.12, MACsec Registers added. ***Section 4, Electrical Specifications*** • Table 864, Recommended Operating Conditions, on page 455 updated. • Table 877, Reset Timing, on page 467 updated.	1/31/2023

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 5	***Rev. 5 release.***	December 21, 2021
Rev. 5 v5.03	***Section 6, Part Order Numbering/Package Marking*** • Part Order Numbering Options table removed. • Figure 56, BRIGHTLANE™ 88Q2220 40-pin QFN Sample Package Marking and Pin 1 Location, on page 480 updated. • Figure 57, BRIGHTLANE™ 88Q2220M 40-pin QFN Sample Package Marking and Pin 1 Location, on page 480 updated. • Figure 58, BRIGHTLANE™ 88Q2221 40-pin QFN Sample Package Marking and Pin 1 Location, on page 481 updated. • Figure 59, BRIGHTLANE™ 88Q2221M 40-pin QFN Sample Package Marking and Pin 1 Location, on page 481 updated. • Figure 60, BRIGHTLANE™ 88Q1200M 40-pin QFN Sample Package Marking and Pin 1 Location, on page 482 updated. • Figure 61, BRIGHTLANE™ 88Q1201M 40-pin QFN Sample Package Marking and Pin 1 Location, on page 482 updated.	
Rev. 5 v5.02	***Section 4, Electrical Specifications*** • Table 865, Thermal Conditions for BRIGHTLANE™ 88Q2220/88Q2220M/88Q2221/88Q2221M/88Q1200M/88Q1201M 40-pin QFN Package, on page 456 updated.	December 14, 2021
Rev. 5 v5.01	***Product Overview*** • Product Overview, on page 2 updated. ***Section 2, PHY Functional Specifications*** • Section 2.21.7, Power Supply Sequencing updated. ***Section 4, Electrical Specifications*** • Table 865, Thermal Conditions for BRIGHTLANE™ 88Q2220/88Q2220M/88Q2221/88Q2221M/88Q1200M/88Q1201M 40-pin QFN Package, on page 456 updated. ***Section 5, Package Mechanical Dimensions*** • Table 890, 40-pin QFN Package Dimensions, on page 478 updated. ***Section 6, Part Order Numbering/Package Marking*** • Figure 55, Sample Part Number, on page 479 updated.	December 13, 2021

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 5 v5.00	***Product Overview*** • Product Overview, on page 2 updated. ***Section 2, PHY Functional Specifications*** • Section 2.15.1, LED Polarity updated. ***Section 3, Registers*** • Table 108, Tx Disable Status Register, on page 144 updated. • Table 110, Interrupt Enable Register, on page 145 updated. • Table 111, GPIO Interrupt Status Register, on page 146 updated. • Table 112, Common LPSD Control Register 1, on page 146 updated. • Table I/O Voltage Control Register Device 4, Register 0x8214 removed. • Table 152, Critical Failure Interrupt Mask Register, on page 163 updated. • Table 159, PCS Control Register 1, on page 170 updated. • Table 160, PCS Status Register 1, on page 171 updated. • Table 161, PCS Device Identifier Register 1, on page 171 updated. • Table 169, PCS Control Register, on page 173 updated. • Table 170, PCS 1000BASE-T1 Status Register 1, on page 174 updated. • Table 213, MAC Specific Control Register, on page 191 updated. • Table 261, LED [1:0] Polarity Control Register, on page 211 updated. • Table 268, 1000BT1 Sleep/Wakeup Interrupt Enable, on page 215 updated. • Table 275, Packet Generator Control Register, on page 218 updated. • Table 274, 1000BT1 LTT_TIMER, on page 216 updated. • Table 275, 1000BT1 LRT_TIMER, on page 216 updated. • Table 276, 1000BT1 RRT_TIMER, on page 216 updated. • Table 296, SGMII Registers — Register Map, on page 225 updated. ***Section 5, Package Mechanical Dimensions*** • Figure 54, 40-pin QFN Package Mechanical Drawing, on page 477 updated. ***Section 6, Part Order Numbering/Package Marking*** • Table 302, Part Order Numbering Options, on page 210 updated.	December 12, 2021

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 4	***Rev. 4 release.***	January 15, 2021
Rev. 4 v4.06	***Section 4, Electrical Specifications*** • Table 278, Current Consumption AVDDL, on page 197 updated. • Table 280, Current Consumption DVDD, on page 198 updated. • Table 281, Current Consumption VDDO, on page 198 updated. • Table 284, Internal Resistors, on page 200 added.	
Rev. 4 v4.05	***Section 4, Electrical Specifications*** • Table 278, Current Consumption AVDDL, on page 197 updated. • Table 279, Current Consumption AVDD33, on page 197 updated. • Table 280, Current Consumption DVDD, on page 198 updated. • Table 281, Current Consumption VDDO, on page 198 updated.	January 8, 2021
Rev. 4 v4.04	***Section 1, Signal Description*** • Table 10, 88Q2220/88Q2220M Power, Ground, and Internal Regulators, on page 30 updated. • Table 21, 88Q2221/88Q2221M Power, Ground, and Internal Regulators, on page 37 updated. • Table 32, 88Q1200M Power, Ground, and Internal Regulators, on page 44 updated. • Table 43, 88Q1201M Power, Ground, and Internal Regulators, on page 51 updated. ***Section 4, Electrical Specifications*** • Section 4.4.1, Current Consumption when Using External Regulators updated. • Table 278, Current Consumption AVDDL, on page 197 updated. • Table 279, Current Consumption AVDD33, on page 197 updated. • Table 280, Current Consumption DVDD, on page 198 updated. • Table 281, Current Consumption VDDO, on page 198 updated.	January 6, 2021
Rev. 4 v4.03	***Product Overview*** • Product Overview, on page 3 updated. ***Section 1, Signal Description*** • Table 10, 88Q2220/88Q2220M Power, Ground, and Internal Regulators, on page 30 updated. ***Section 5, Package Mechanical Dimensions*** • Table 302, Part Order Options, on page 214 updated.	December 7, 2020

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 4 v4.02	***Product Overview*** • Figure 4, 88Q1201M Block Diagram, on page 6 updated. ***Section 1, Signal Description*** • Table 10, 88Q2220/88Q2220M Power, Ground, and Internal Regulators, on page 30 updated. • Table 21, 88Q2221/88Q2221M Power, Ground, and Internal Regulators, on page 37 updated. • Table 32, 88Q1200M Power, Ground, and Internal Regulators, on page 44 updated. • Table 43, 88Q1201M Power, Ground, and Internal Regulators, on page 51 updated. ***Section 2, PHY Functional Specifications*** • Table 65, Power Supply Options — Integrated Regulator (REG_IN), on page 89 updated. • Table 66, Power Supply Options — External Supplies, on page 90 updated. ***Section 4, Electrical Specifications*** • Table 275, Absolute Maximum Ratings, on page 194 updated.	December 4, 2020
Rev. 4 v4.01	***Product Overview*** • Figure 4, 88Q1201M Block Diagram, on page 6 updated. ***Section 1, Signal Description*** • Table 10, 88Q2220/88Q2220M Power, Ground, and Internal Regulators, on page 30 updated. • Table 21, 88Q2221/88Q2221M Power, Ground, and Internal Regulators, on page 37 updated. • Table 24, 88Q1200M Media Dependent Interface, on page 40 updated. • Table 25, 88Q1200M Host Interfaces, on page 40 updated. • Table 35, 88Q1201M Media Dependent Interface, on page 47 updated. ***Section 2, PHY Functional Specifications*** • Figure 5, 88Q2220M/88Q2221M Functional Block Diagram, on page 53 updated. • Figure 6, 88Q2220/88Q2221 Functional Block Diagram, on page 54 updated. • Figure 7, 88Q1200M Functional Block Diagram, on page 55 updated. • Figure 8, 88Q1201M Functional Block Diagram, on page 56 updated. • Figure 10, MAC Interface Loopback Diagram — Copper Media Interface, on page 62 updated. • Figure 11, Copper Line Loopback Data Path, on page 63 updated. • Figure 12, FIFO Locations, on page 64 updated. • Figure 17, In-band Communication Transaction, on page 69 updated. • Figure 18, LPSD Block Diagram - VBAT Option 1, on page 73 updated. • Figure 19, LPSD Block Diagram - VBAT Option 2, on page 73 updated. ***Section 4, Electrical Specifications*** • Table 282, Digital Pins, on page 199 updated.	December 1, 2020

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 4 v4.00	***Cover*** • Title updated. ***Product Overview*** • Product Overview, on page 3 updated. • Table 1, Features, on page 4 updated. • Figure 3, 88Q1200M Block Diagram, on page 5 updated. • Figure 4, 88Q1201M Block Diagram, on page 6 updated. ***Section 2, PHY Functional Specifications*** • Figure 7, 88Q1200M Functional Block Diagram, on page 55 added. • Figure 8, 88Q1201M Functional Block Diagram, on page 56 added. • Figure 11, Copper Line Loopback Data Path, on page 63 added. • Figure 12, FIFO Locations, on page 64 added. • Figure 14, 88Q120xM TC10 Sleep/Wake, on page 66 added. • Figure 15, In-band TC10 Relay to MAC (Switch) Interface, on page 66 added. • Figure 16, MAC (Switch) Interface In-band TC10 Relay, on page 67 added. • Figure 17, In-band Communication Transaction, on page 69 added. • Figure 18, LPSD Block Diagram - VBAT Option 1, on page 73 added. • Figure 19, LPSD Block Diagram - VBAT Option 2, on page 73 added. • Figure 31, MMAC Location in 88Q2221/88Q2221M/88Q1201M Data Path, on page 94 added. ***Section 5, Package Mechanical Dimensions*** • Table 302, Part Order Options, on page 214 updated. • Figure 53, 88Q1200M 40-pin QFN Sample Package Marking and Pin 1 Location, on page 219 added. • Figure 54, 88Q1201M 40-pin QFN Sample Package Marking and Pin 1 Location, on page 219 added.	October 28, 2020

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 3	***Rev. 3 release.***	September 15, 2020
Rev. 3 v3.09	***Product Overview*** • Features, on page 4 updated. ***Section 2, PHY Functional Specifications*** • Section 2.2.1.2, Slew Rate Control and Waveshaping updated. • Section 2.2.2.1, 100/1000BASE-T1 updated. • Section 2.2.3.6, Link Monitor updated. • Section 2.2.4.1, 100/1000BASE-T1 updated. • Table 48, Power Down Control Bits, on page 65 updated. • Enter Sleep Modes, on page 70 updated. • Sleep Handshake, on page 70 updated. • Table 53, Status of Functional Block in Each Mode, on page 75 updated. • Section 2.14, GPIO updated. ***Section 3, Registers*** • Table 99, Common LPSD Status, on page 115 updated. ***Section 4, Electrical Specifications*** • Table 275, Absolute Maximum Ratings, on page 194 updated. • Table 276, Recommended Operating Conditions, on page 195 updated.	
Rev. 3 v3.08	***Product Overview*** • Features, on page 4 updated. ***Section 1, Signal Description*** • Table 6, 88Q2220/88Q2220M Clock/Configuration/Reset/I/O, on page 28 updated. • Table 17, 88Q2221/88Q2221M Clock/Configuration/Reset/I/O, on page 35 updated. ***Section 2, PHY Functional Specifications*** • Figure 5, 88Q2220M/88Q2221M Functional Block Diagram, on page 53 updated. • Figure 6, 88Q2220/88Q2221 Functional Block Diagram, on page 54 updated. • Table 45, RGMII Signal Mapping, on page 59 updated. • Section 2.23.2, Data Flow updated. ***Section 4, Electrical Specifications*** • Table 276, Recommended Operating Conditions, on page 195 updated. • Table 282, Digital Pins, on page 199 updated. • Section 4.5.2, TX_ENABLE/LED Pin updated. • Table 283, TX_ENABLE/LED Pin, on page 199 updated. • Table 288, Reset Timing, on page 203 updated.	September 9, 2020

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 3 v3.07	***Section 2, PHY Functional Specifications*** • Figure 31, MMAC Location in 88Q2221/88Q2221M/88Q1201M Data Path, on page 94 updated. ***Section 3, Registers*** • Table 97, Interrupt Enable Register, on page 114 updated. • Table 98, GPIO Interrupt Status Register, on page 115 updated. • Table 99, Common LPSD Status, on page 115 updated. • Table 112, WOL Interrupt Mask Register, on page 120 updated. • Table 113, WOL Interrupt Status Register, on page 120 updated. • Table 114, I/O Voltage Control Register, on page 120 updated. • Table 125, Secondary ID Register, on page 124 updated. • Table 135, PCS Package Identifier Register 2, on page 128 updated. • Table 196, Mean Square Error, on page 151 updated. • Table 197, Worst Case Mean Square Error, on page 151 updated. • Table 225, GPIO Function and Interrupt Tri-state Control Register, on page 162 updated. • Table 226, GPIO Interrupt Register, on page 163 updated. • Table 227, Open Drain Control Register, on page 163 updated. • Table 228, Function Control Register, on page 164 updated. • Table 229, LED [1:0] Polarity Control Register, on page 164 updated. ***Section 4, Electrical Specifications*** • Table 281, Current Consumption VDDO, on page 198 updated. • IEEE Transceiver Parameters removed.	August 31, 2020

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 3 v3.06	***Section 3, Registers*** • Table 102, Temperature Sensor Register 2, on page 117 updated. • Table 103, Temperature Sensor Register 3, on page 117 updated. • Table 104, Temperature Sensor Register 4, on page 118 updated. • Table 112, WOL Interrupt Mask Register, on page 120 updated. • Table 113, WOL Interrupt Status Register, on page 120 updated. • Table 114, I/O Voltage Control Register, on page 120 updated. • Table 115, WOL Control Register, on page 120 updated. • Table 116, WOL Status Register, on page 121 updated. • Table 117, WOL Packet Destination Register 0, on page 121 updated. • Table 118, WOL Packet Destination Register 1, on page 121 updated. • Table 119, WOL Packet Destination Register 2, on page 121 updated. • Table 120, Under Voltage Interrupt Mask Register, on page 121 updated. • Table 121, Under Voltage Interrupt Status Register, on page 122 updated. • Table 122, Critical Failure Interrupt Register, on page 123 updated. • Table 123, Critical Failure Interrupt Mask Register, on page 123 updated. • Table 124, Failure Power Down Mask Register H, on page 123 updated. • Table 125, Secondary ID Register, on page 124 updated. • Table 137, PCS Control Register, on page 128 updated. • Table 138, PCS 1000BASE-T1 Status Register 1, on page 128 updated. • Table 177, 100BASE-T1 Specific Interrupt Enable Register, on page 144 updated. • Table 178, Copper Interrupt Status Register, on page 145 updated. • Table 190, Receiver Status Register, on page 148 updated.	August 29, 2020

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 3 v3.05	***Section 2, PHY Functional Specifications*** • Table 23, Modes, on page 33 removed. • Section 2.3.1, RGMII Interface updated. • Table 46, Modes, on page 59 updated. • Figure 25, Signal Reflections, on page 85 updated. • Figure 26, Clean Signal after Manual Calibration, on page 85 updated. • Table 59, Sampled Values, on page 86 updated. • Figure 29, Regulator-generated 1.2V for AVDDL, on page 91 updated. • Figure 30, Regulator-generated 0.75 for DVDD, on page 92 updated. ***Section 3, Registers*** • Table 231, 1000BT1 Sleep/Wake Request, on page 165 updated. • Table 232, 1000BT1 Sleep Status, on page 166 updated. • Table 233, 1000BT1 Wakeup Status, on page 166 updated. • Table 234, 1000BT1 Sleep/Wakeup Interrupt Status, on page 166 updated. • Table 235, 1000BT1 Sleep/Wakeup Interrupt Enable, on page 166 updated. ***Section 4, Electrical Specifications*** • Table 293, PHY Input — TCLK No Delay when Register 4.A001.15 = 0, on page 208 updated. • Table 294, PHY Input — TCLK Delay when Register 4.A001.15 = 1, on page 208 updated. • Table 295, PHY Output — RCLK No Delay when Register 4.A001.14 = 0, on page 209 updated. • Table 296, PHY Output — RCLK Delay when Register A.8001.14 = 1, on page 209 updated.	August 27, 2020

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 3 v3.04	***Section 2, PHY Functional Specifications*** • Section 2.18, Manual Impedance Calibration updated. ***Section 3, Registers*** • Table 80, PMA/PMD Speed Ability Register, on page 107 updated. • Table 95, Tx Disable Status Register, on page 113 updated. • Table 105, Interrupt Enable Register, on page 118 updated. • Table 106, Interrupt Status Register, on page 118 updated. • Table 135, PCS Package Identifier Register 2, on page 128 updated. • Table 231, 1000BT1 Sleep/Wake Request, on page 165 updated. • Table 232, 1000BT1 Sleep Status, on page 166 updated. • Table 233, 1000BT1 Wakeup Status, on page 166 updated. • Table 234, 1000BT1 Sleep/Wakeup Interrupt Status, on page 166 updated. • Table 235, 1000BT1 Sleep/Wakeup Interrupt Enable, on page 166 updated. • Table 250, RGMII_IO Control Register, on page 172 added. • PHY Identifier Register 2, Device 4, Register 0x8003 removed. • PTP registers removed. ***Section 4, Electrical Specifications*** • Table 276, Recommended Operating Conditions, on page 195 updated. • Table 278, Current Consumption AVDDL, on page 197 updated. ***Section 6, Part Order Numbering/Package Marking*** • Figure 49, 88Q2220 40-pin QFN Sample Package Marking and Pin 1 Location, on page 216 updated. • Figure 50, 88Q2220M 40-pin QFN Sample Package Marking and Pin 1 Location, on page 216 updated. • Figure 51, 88Q2221 40-pin QFN Sample Package Marking and Pin 1 Location, on page 217 updated. • Figure 52, 88Q2221M 40-pin QFN Sample Package Marking and Pin 1 Location, on page 218 updated.	August 27, 2020

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 3 v3.03	***Section 1, Signal Description*** • Table 2, 88Q2220/88Q2220M Media Dependent Interface, on page 26 updated. • Table 3, 88Q2220/88Q2220M Host Interfaces, on page 26 updated. • Table 4, 88Q2220/88Q2220M Management Interface, on page 27 updated. • Table 5, 88Q2220/88Q2220M TX_ENABLE/GPIO/Interrupt Interface, on page 27 updated. • Table 6, 88Q2220/88Q2220M Clock/Configuration/Reset/I/O, on page 28 updated. • Table 7, 88Q2220/88Q2220M Control and Reference, on page 28 updated. • Table 8, 88Q2220/88Q2220M Test, on page 28 updated. • Table 9, 88Q2220/88Q2220M Low Power Signal Detect, on page 29 updated. • Table 10, 88Q2220/88Q2220M Power, Ground, and Internal Regulators, on page 30 updated. • Table 13, 88Q2221/88Q2221M Media Dependent Interface, on page 33 updated. • Table 14, 88Q2221/88Q2221M Host Interfaces, on page 33 updated. • Table 15, 88Q2221/88Q2221M Management Interface, on page 34 updated. • Table 16, 88Q2221/88Q2221M TX_ ENABLE/GPIO/Interrupt Interface, on page 34 updated. • Table 17, 88Q2221/88Q2221M Clock/Configuration/Reset/I/O, on page 35 updated. • Table 18, 88Q2221/88Q2221M Control and Reference, on page 35 updated. • Table 19, 88Q2221/88Q2221M Test, on page 35 updated. • Table 20, 88Q2221/88Q2221M Low Power Signal Detect, on page 36 updated. • Table 21, 88Q2221/88Q2221M Power, Ground, and Internal Regulators, on page 37 updated.	August 11, 2020

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 3 v3.02	***Section 2, PHY Functional Specifications*** • Section 2.21.7, Power Supply Sequencing updated. • Table 59, Sampled Values, on page 86 updated. ***Section 3, Registers*** • Table 77, PMA/PMD Control Register 1, on page 106 updated. • Table 78, PMA/PMD Device Identifier Register 1, on page 107 updated. • Table 83, PMA/PMD Package Identifier Register 1, on page 108 updated. • Table 84, PMA/PMD Package Identifier Register 2, on page 108updated. • Table 97, Interrupt Enable Register, on page 114 updated. • Table 111, I/O Voltage Control Register, on page 120 added. • Table 105, Interrupt Enable Register, on page 118 added. • Table 106, Interrupt Status Register, on page 118 added. • Table 84, 100BASE-T1 LPSD Control Register, on page 105 added. • Table 87, 100BASE-T1 Sleep Status, on page 107 added. • Table 88, 100BASE-T1 Wakeup Status, on page 107added. • Table 89, 100BASE-T1 Sleep/Wakeup Interrupt Status, on page 107 added. • Table 90, 100BASE-T1 Sleep/Wakeup Interrupt Enable, on page 107 added. • Table 152, Auto-Negotiation Device Identifier Register 2, on page 134 updated. • Table 175, PHY Status, on page 143 added. • Table 176, PHY REM/LOC Counters, on page 144 added. • Table 188, PTP Control Register 1, on page 147 updated. ***Section 4, Electrical Specifications*** • Table 277, Thermal Conditions for 88Q2220/88Q2220M/88Q2221/88Q2221M/88Q1200M/88Q1201M 40-pin QFN Package, on page 196 updated.	August 10, 2020

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 3 v3.01	***Product Overview*** • Features updated. ***Section 2, PHY Functional Specifications*** • Figure 5, 88Q2220M/88Q2221M Functional Block Diagram, on page 32 updated. • Figure 6, 88Q2220/88Q2221 Functional Block Diagram, on page 33 updated. • Section 2.23, MMAC updated.	August 9, 2020
Rev. 3 v3.00	***Section 1, Signal Description*** • Table 4, 88Q2220/88Q2220M Management Interface, on page 21 updated. • Table 5, 88Q2220/88Q2220M TX_ENABLE/GPIO/Interrupt Interface, on page 21 updated. • Table 10, 88Q2220/88Q2220M Power, Ground, and Internal Regulators, on page 24 updated. ***Section 2, PHY Functional Specifications*** • Figure 5, 88Q2220M/88Q2221M Functional Block Diagram, on page 32 updated. ***Section 5, MMAC*** • Added. ***Section 5, Package Mechanical Dimensions*** • Figure 47, 40-pin QFN Package Mechanical Drawing, on page 212 updated. ***Section 6, Part Order Numbering/Package Marking*** • Figure 50, 88Q2220M 40-pin QFN Sample Package Marking and Pin 1 Location, on page 216 updated. • Figure 51, 88Q2221 40-pin QFN Sample Package Marking and Pin 1 Location, on page 217 updated. • Figure 52, 88Q2221M 40-pin QFN Sample Package Marking and Pin 1 Location, on page 218 updated.	August 8, 2020

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 2	***Rev. 2 release.***	August 7, 2020
Rev. 2 v2.00	***Section 6, Part Order Numbering/Package Marking*** • Figure 50, 88Q2220M 40-pin QFN Sample Package Marking and Pin 1 Location, on page 216 updated. • Figure 51, 88Q2221 40-pin QFN Sample Package Marking and Pin 1 Location, on page 217 updated. • Figure 52, 88Q2221M 40-pin QFN Sample Package Marking and Pin 1 Location, on page 218 updated.	August 7, 2020
Rev. 1	***Rev.1/Initial release.***	June 2, 2020
Rev. 1 v1.10	***Entire document*** • 100BASE-T1/1000BASE-T1 references updated. ***Section 3, Registers*** • Table 54, Register Types, on page 91 updated. ***Section 6, Part Order Numbering/Package Marking*** • Table 304, 88Q2220/88Q2220M/88Q2221/88Q2221M Part Order Options, on page 226 updated. • Figure 46, 88Q2220 40-pin QFN Sample Package Marking and Pin 1 Location, on page 228 updated.	June 2, 2020
Rev. 1 v1.09	***Section 2, PHY Functional Specifications*** • Figure 13, LPSD Block Diagram - VBAT Option 1, on page 53 added. • Figure 14, LPSD Block Diagram - VBAT Option 2, on page 53 added. • Application Notes updated. • Section 2.8, Status of Functional Blocks in Each Device Mode added. ***Section 5, Package Mechanical Dimensions*** • Figure 44, 88Q2220/88Q2220M/88Q2221/88Q2221M 40-pin QFN Package Mechanical Drawing, on page 224 updated. ***Section 6, Part Order Numbering/Package Marking*** • Figure 45, Sample Part Number, on page 226 updated. • Figure 46, 88Q2220 40-pin QFN Sample Package Marking and Pin 1 Location, on page 228 updated. • Figure 47, 88Q2220M 40-pin QFN Sample Package Marking and Pin 1 Location, on page 228 updated. • Figure 48, 88Q2221 40-pin QFN Sample Package Marking and Pin 1 Location, on page 229 updated. • Figure 49, 88Q2221M 40-pin QFN Sample Package Marking and Pin 1 Location, on page 230 updated.	June 1, 2020

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 1 v1.08	***Product Overview*** • Table 1, Features, on page 4 updated. • Feature Comparison table removed. ***Section 1, Signal Description*** • Table 9, 88Q2220/88Q2220M Low Power Signal Detect, on page 22 updated. • Table 13, 88Q2221/88Q2221M Media Dependent Interface, on page 27 updated. ***Section 2, PHY Functional Specifications*** • Figure 5, 88Q2220M/88Q2221M Functional Block Diagram, on page 32 added. • Figure 6, 88Q2220/88Q2221 Functional Block Diagram, on page 33 added. • Section 2.11.1, CRC Error Counter and Frame Counter added. • Section 2.18, Manual Impedance Calibration updated. ***Section 3, Registers*** • Table 74, Tx Disable Status Register, on page 100 updated.	May 28, 2020
Rev. 1 v1.07	***Product Overview*** • Table 1, Features, on page 4 updated. • Table 2, Feature Comparison, on page 4 updated. ***Section 1, Signal Description*** • Figure 3, 88Q2220/88Q2220M Device 40-pin RGMII Package (Top View), on page 19 updated. • Figure 4, 88Q2221/88Q2221M Device 40-pin SGMII Package (Top View), on page 26 updated. ***Section 2, PHY Functional Specifications*** • Section 2.1, System Interfaces updated. • Section 2.21.6, Regulator Configuration added. • Section 2.21.7, Power Supply Sequencing updated. ***Section 4, Electrical Specifications*** • Table 276, Recommended Operating Conditions, on page 195 updated.	May 18, 2020

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 1 v1.06	***Product Overview*** • Table 1, Features, on page 4 added. • Feature Comparison table removed. ***Section 1, Signal Description*** • Figure 3, 88Q2220/88Q2220M Device 40-pin RGMII Package (Top View), on page 25 updated. • Figure 4, 88Q2221/88Q2221M Device 40-pin SGMII Package (Top View), on page 32 updated. • Table 9, 88Q2220/88Q2220M Low Power Signal Detect, on page 29 updated. • Table 11, 88Q2220/88Q2220M 40-pin QFN Pin Assignment List — Alphabetical by Signal Name, on page 31 updated. • Table 20, 88Q2221/88Q2221M Low Power Signal Detect, on page 36 updated. • Table 22, 88Q2221/88Q2221M 40-pin QFN Pin Assignment List — Alphabetical by Signal Name, on page 38 updated. ***Section 2, PHY Functional Specifications*** • Table 38, Sampled Values, on page 69 updated. • Section 2.21, Regulators and Power Supplies updated. • Table 46, Power Supply Options — External 0.75V, Integrated Regulator (REG_IN) Supplies Only 1.2V, on page 73 updated. • Table 47, Power Supply Options — External 1.2V to AVDDL, Integrated Regulator (REG_IN) Supplies DVDD 0.75V Only, on page 73 updated. • Section 2.21.5, VDDO updated. ***Section 4, Electrical Specifications*** • Table 279, Recommended Operating Conditions, on page 206 updated. • Table 297, PHY Output — RCLK No Delay when Register 31.8001.14 = 0, on page 220 updated. ***Section 5, Package Mechanical Dimensions*** • Figure 44, 88Q2220/88Q2220M/88Q2221/88Q2221M 40-pin QFN Package Mechanical Drawing, on page 224 updated. • Table 302, 88Q2220/88Q2220M/88Q2221/88Q2221M 40-pin QFN Package Dimensions, on page 225 updated.	May 12, 2020

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 1 v1.05	***Product Overview*** • Figure 2, 88Q2220/88Q2220M Block Diagram, on page 5 added. ***Section 1, Signal Description*** • Figure 3, 88Q2220/88Q2220M Device 40-pin RGMII Package (Top View), on page 19 updated. • Table 5, 88Q2220/88Q2220M TX_ENABLE/GPIO/Interrupt Interface, on page 21 updated. • Table 7, 88Q2220/88Q2220M Control and Reference, on page 22 updated. • Table 8, 88Q2220/88Q2220M Test, on page 22 updated. • Table 9, 88Q2220/88Q2220M Low Power Signal Detect, on page 22 updated. • Table 10, 88Q2220/88Q2220M Power, Ground, and Internal Regulators, on page 24 updated. • Table 14, 88Q2221/88Q2221M Host Interfaces, on page 27 updated. • Table 16, 88Q2221/88Q2221M TX_ ENABLE/GPIO/Interrupt Interface, on page 28 updated. • Table 20, 88Q2221/88Q2221M Low Power Signal Detect, on page 29 updated. • Table 21, 88Q2221/88Q2221M Power, Ground, and Internal Regulators, on page 30 updated. ***Section 2, PHY Functional Specifications*** • Section 2.7.1, Low Power Modes updated. • In-band Wake/Sleep Embedded IDLES, on page 46 updated. • Section 2.7.1.3, Wake from Sleep updated. ***Section 4, Electrical Specifications*** • *Precision Time Protocol (PTP) Timestamping Support* removed. • *Current Consumption when Using Internal Regulators* removed.	May 8, 2020

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 1 v1.04	***Section 1, Signal Description*** • Section 1.1, 88Q2220/88Q2220M Pinout updated. • Section 1.2, 88Q2220/88Q2220M Pin Descriptions updated. • Section 1.3, 88Q2220/88Q2220M Pin Assignment List — Alphabetical by Signal Name updated. • Section 1.4, 88Q2221/88Q2221M Pinout updated. • Section 1.5, 88Q2221/88Q2221M Pin Descriptions updated. • Section 1.6, 88Q2221/88Q2221M Pin Assignment List — Alphabetical by Signal Name updated. ***Section 2, PHY Functional Specifications*** • Section 2.7.1, Low Power Modes updated. ***Section 3, Registers*** • Table 57, PMA/PMD Device Identifier Register 1, on page 96 updated. • Table 58, PMA/PMD Device Identifier Register 2, on page 96 updated. • Table 63, PMA/PMD Package Identifier Register 2, on page 97 updated. • Table 73, Tx Disable Status Register, on page 102 updated. • Table 75, Interrupt Enable Register, on page 102 updated. • Table 76, GPIO Interrupt Status Register, on page 103 updated. • Table 77, Temperature Sensor Register 2, on page 104 updated. • Table 98, PCS Device Identifier Register 2, on page 112 updated. • Table 103, PCS Package Identifier Register 2, on page 114 updated. • Table 104, 1000BASE-T1 PCS Status Register 2, on page 114 updated.	May 6, 2020
Rev. 1 v1.03	***Section 1, Signal Description*** • Section 1.1, 88Q2220/88Q2220M Pinout updated. • Section 1.2, 88Q2220/88Q2220M Pin Descriptions updated. • Section 1.3, 88Q2220/88Q2220M Pin Assignment List — Alphabetical by Signal Name updated. • Section 1.4, 88Q2221/88Q2221M Pinout updated. • Section 1.5, 88Q2221/88Q2221M Pin Descriptions updated. • Section 1.6, 88Q2221/88Q2221M Pin Assignment List — Alphabetical by Signal Name updated. ***Section 2, PHY Functional Specifications*** • Section 2.19.1, Hardware Configuration updated.	April 30, 2020

Table 892: Revision History (Continued)

Revision	Description	Date
Rev. 1 v1.02	***Product Overview*** • Applications, on page 4 updated. • Table 2, Feature Comparison, on page 4 added. • Figure 1, 88Q2221/88Q2221M Block Diagram, on page 4 added. • Figure 2, 88Q2220/88Q2220M Block Diagram, on page 5 added. ***Section 1, Signal Description*** • Section 1.1, 88Q2220/88Q2220M Pinout updated. • Section 1.2, 88Q2220/88Q2220M Pin Descriptions updated. • Section 1.3, 88Q2220/88Q2220M Pin Assignment List — Alphabetical by Signal Name updated. • Section 1.4, 88Q2221/88Q2221M Pinout updated. • Section 1.5, 88Q2221/88Q2221M Pin Descriptions updated. • Section 1.6, 88Q2221/88Q2221M Pin Assignment List — Alphabetical by Signal Name updated. ***Section 2, PHY Functional Specifications*** • Table 44, Power Supply Options — Integrated Regulator (REG_IN), on page 71 updated. • Table 44, Power Supply Options — Integrated Regulator (REG_IN), on page 71 updated. • Table 46, Power Supply Options — External 0.75V, Integrated Regulator (REG_IN) Supplies Only 1.2V, on page 72 updated • Table 47, Power Supply Options — External 1.2V to AVDDL, Integrated Regulator (REG_IN) Supplies DVDD 0.75V Only, on page 72 updated. • Figure 16, Supply and Regulator Connection Options removed. • Section 2.21.1, AVDDL updated. • Section 2.21.3, DVDD updated. • Section 2.21.4, REG_IN updated. • Section 2.20.6 VDD18_OUT removed. • Section 2.20.7 DVDD_OUT removed. • Section 2.21.7, Power Supply Sequencing updated.	April 30, 2020
Rev. 1 v1.01	***Product Overview*** • Features, on page 4 updated. ***Section 1, Signal Description*** • Section 1.1, 88Q2220/88Q2220M Pinout updated. • Section 1.2, 88Q2220/88Q2220M Pin Descriptions updated. • Section 1.3, 88Q2220/88Q2220M Pin Assignment List — Alphabetical by Signal Name	April 24, 2020

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